Com Block

COM-8003
SIGNAL DIVERSITY COMBINING

Key Features

- Signal diversity combiner for receiver applications. Combines up to 4 signal replicas.

- Large (256 MB) memory for very large time-diversity.

- Post-detection combining (after demodulation). 4-bit soft-quantized samples from multiple demodulators are re-synchronized to compensate for differential delays and summed coherently to improve signal-to-noise ratio.

COM-8003 Signal Diversity Combiner

- Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com8003.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Typical Application

When used in conjunction with other ComBlocks, the COM-8003 is capable of implementing time-diversity, frequency-diversity, space-diversity and modulation-diversity schemes. In all cases, the combining is implemented at post detection, that is after the demodulation.

The COM-8003 is **not** compatible with phased-array type, pre-detection combining techniques.

A typical setup to demonstrate multiple signal diversity combining techniques is shown below.

At the transmitter, the COM-8004 module splits an FEC encoded input data stream into two streams. Each stream is subject to a fixed independently programmable delay (for time diversity). In addition, periodic synchronization markers are inserted in each stream. Each stream replica is then modulated and transmitted at a distinct frequency (for frequency diversity). Two antenna can be used for space diversity.

At the receiver, two receivers/demodulator chains are used to recover two replica of the transmitted data stream(s). The COM-8003 recovers the frame synchronization for each stream, re-aligns the replicas in time by creating differential delays, then sums the two replicas to improve the signal to ratio. The resulting combined streams is then forwarded to a FEC decoder.
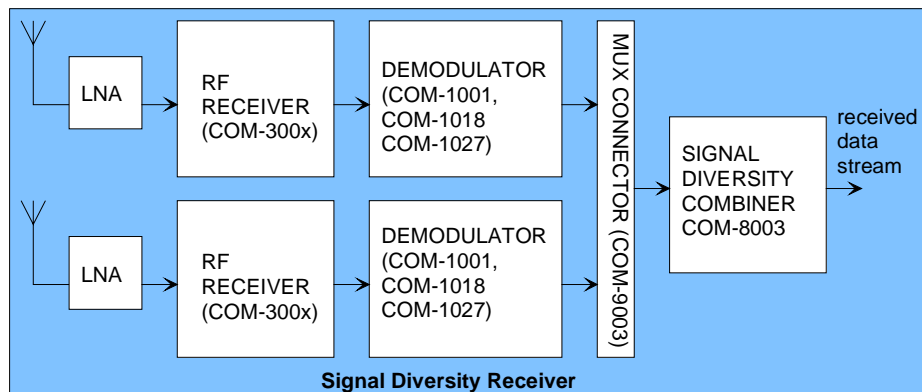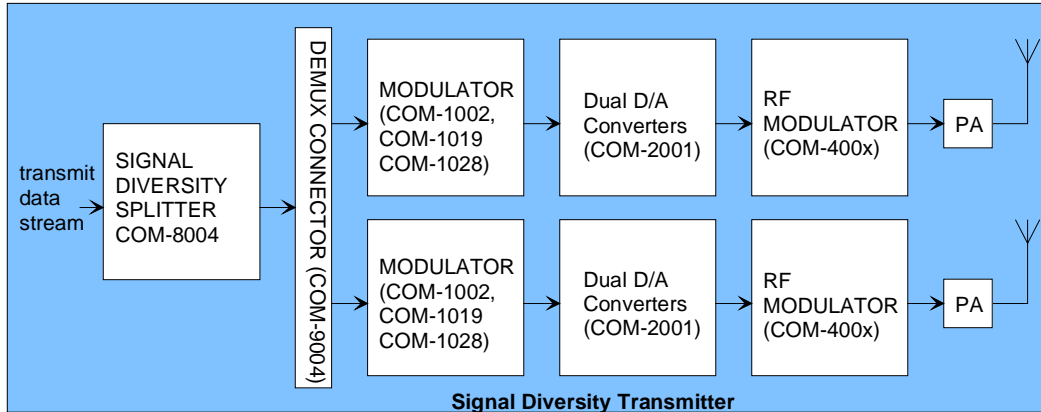
Signal Diversity Setup: 2-streams example

This generic assembly can be modified to implement a variety of other diversity techniques such as

- Single Input Multiple Output (SIMO) space diversity: one transmit chain only.
- modulation diversity: use different modulations for each replica.

Signal Diversity Combining

Principle

Signal diversity combining is a method whereby a signal is transmitted over several media (satellite links for example) to improve the quality of service.

The receiver is a multi-channel receiver. It is designed to process multiple signals from the antenna(e) to the baseband demodulators.

Receiver block diagram (2-stream signal diversity example)
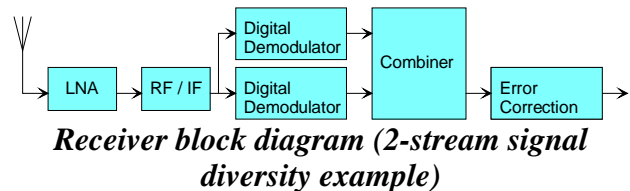
The COM-8003 combiner processes these demodulated signal replicas by removing the differential delay and summing the signals to yield the best signal to noise ratio.

How does summing the received signals coherently improve the signal to noise ratio?
Let us consider the simplified case of two received signals of equal amplitude S and equal noise amplitude N. After summing in amplitude (coherently), the resulting signal has an amplitude $S_{sum} = 2S$ and noise amplitude $N_{sum} = sqrt(2).N$ (summing two independent random variables). The signal to noise ratio improvement is thus 3 dB.

2

sync. sequence	data	sync. sequence	data

*A frame structure with synchronization marker is used to synchronize all received signals.*

Because of the propagation time difference, the received signals are offset in time. They must be re-aligned prior to combining. In order to help with the synchronization, a unique short synchronization marker is inserted periodically in the transmitted data stream. A 32-bit synchronization marker is typically a good tradeoff between probability of acquisition in extreme noise conditions and minimum overhead.

Combiner Implementation

The COM-8003 combiner comprises three distinct circuits:

(a) a synchronization circuit, whereby the start of frame and start of superframe are detected for each input signal.

(b) An elastic buffer, whereby the differential delay among the various replica is removed.

(c) An intelligent combiner, whereby the synchronized replicas are summed with adaptively controlled coefficients for best quality of service.
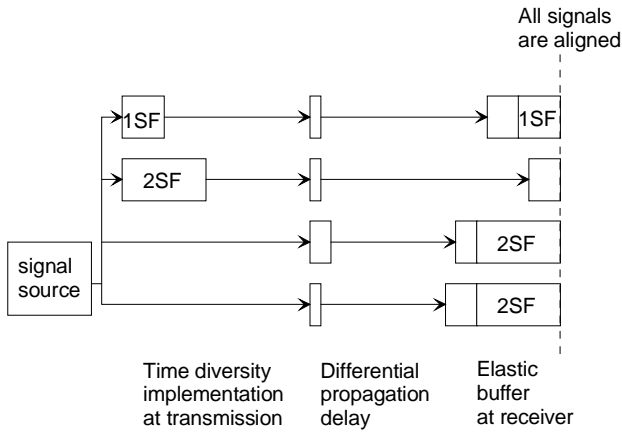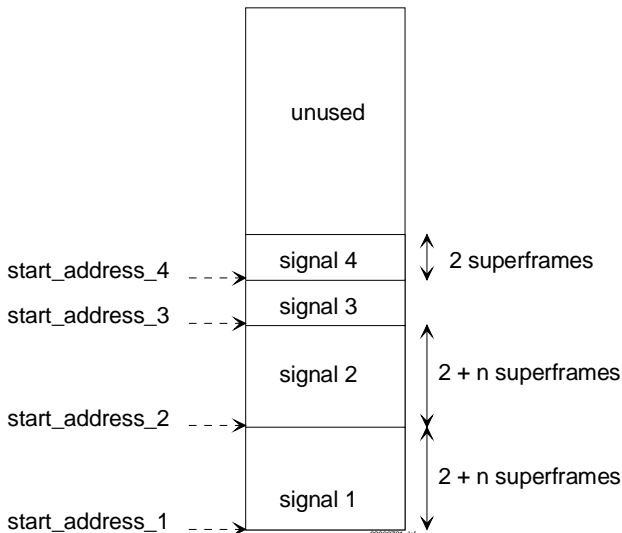
Elastic buffering is used to re-align in time all the signal replicas after they experience differential delays during propagation and at the transmitter.


Signal Diversity Combiner

3
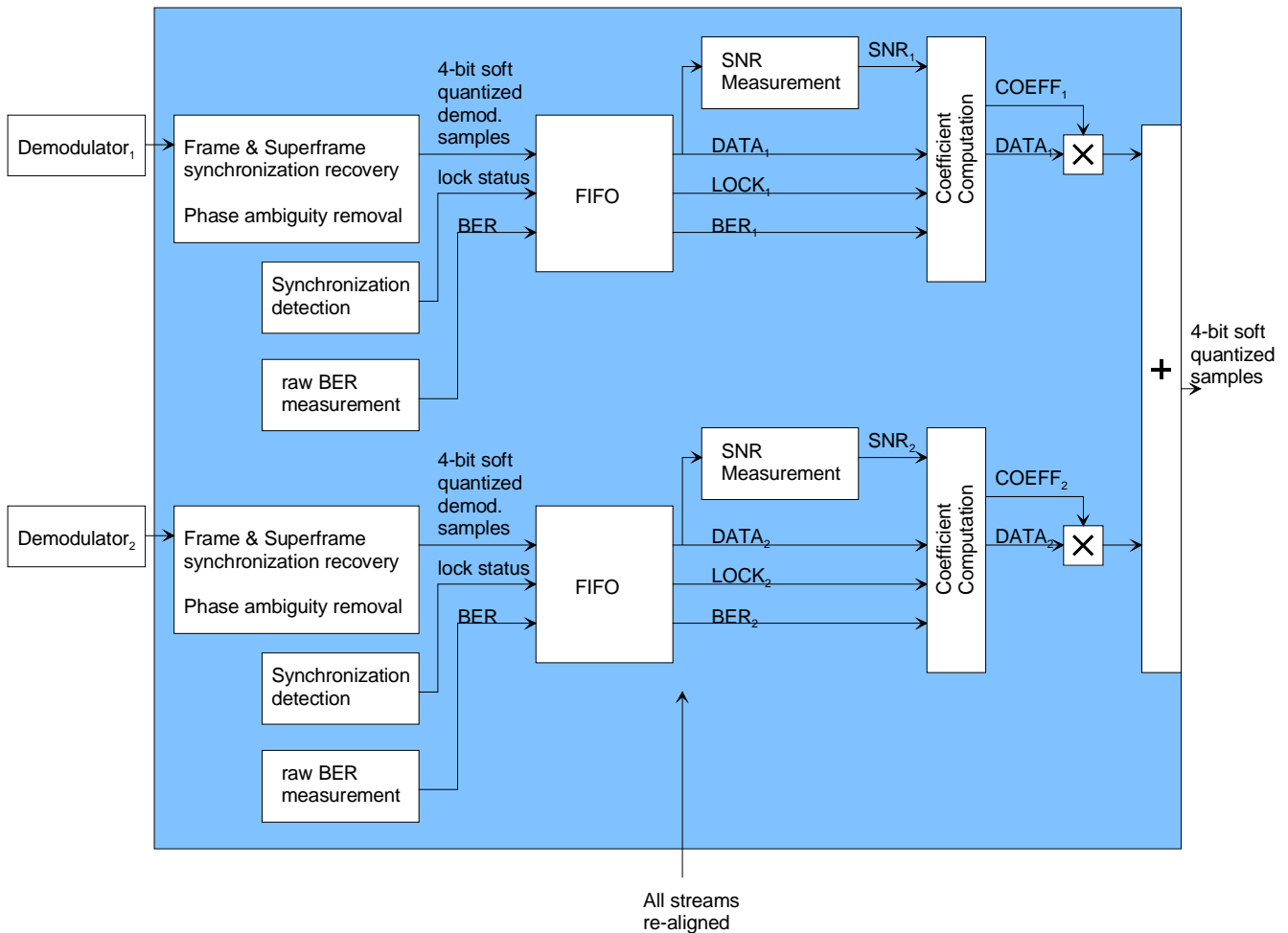
A single SDRAM is shared among all streams to implement elastic buffering. Circular buffers are memory-mapped in the SDRAM as illustrated below for a 4-stream combiner.

SDRAM Memory Map (at combiner)

Delay considerations: there is no intrinsic processing delay associated with signal diversity combining. Received signals are only stored until the trailing replica is received (maximum one-way propagation time difference for GEO constellation is 40 ms).
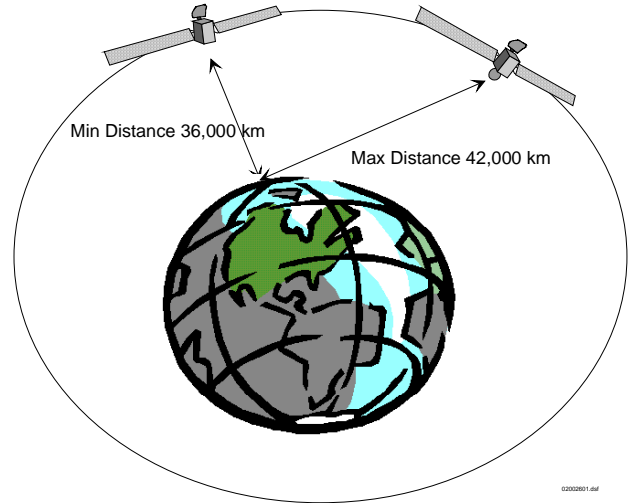
maximum differential propagation delay is
12,000 km / 3 x 10^8 m/s = 40 ms (GEO)

Each signal is structured with a short frame and a longer superframe. The frame size is fixed at 4128 bits (4096 data bits plus 32 frame synchronization bits) to minimize the sync pattern overhead (less than 1% overhead). A superframe structure comprising an integer number of frames is required to eliminate any time-of-arrival ambiguity.

The superframe size is defined by 2*(maximum differential propagation delay among replicas), rounded up to an integer number of frames. By consequence, the superframe size depends on the data rate.
Example:

- Data rate: 5 Kbps
- Maximum differential propagation delay among replicas: 4ms (12,000 km/c)
- Equivalent number of bits in differential delay: 20 bits
- Minimum superframe size = 1 frame = 4128 bits

There are, however, operational cases whereby a signal is transmitted n superframes earlier than the other replicas. This method can be used to provide time diversity in a broadcast network for example. In such a case, the SDRAM section for a given signal can be increased from 2 to n+2.

Combiner Algorithm

The weights used for combining multiple received streams are computed on the basis of the individual streams quality measurements, namely:

- Synchronization lock status, based on the detection of periodic start-of-frame synchronization markers.

- Bit Error Rate (BER) measurements based on the detection of bit errors within the 32-bit periodic (and known) frame synchronization markers. The BER computation is performed over 1024 bits spanning 32 consecutive frames. It is thus updated infrequently and detected with a noticeable delay.

- Noise-to-Signal Ratio (NSR = 1/SNR), obtained by computing the standard deviation of the noise on 4-bit soft-quantized input samples obtained from the demodulator. A key assumption is that the soft-quantized samples are normalized by some AGC. The NSR is computed continuously by running a continuous average over 4096 samples.

The two quality measurements performed prior to the elastic buffer (synchronization lock status and BER) are subjected to the same delay through the buffer as the associated data stream. Therefore, the combiner algorithm can use either or both the current and delayed (signal aligned) versions of these two quality measurements.

The baseline combining algorithm (-A option) uses the following rules for combining:

- immediately disqualify a stream if the synchronization status becomes 'unlocked'.

- if all streams are disqualified, enable the first stream for which the current synchronization lock status is enabled (even though the delayed version of the synchronization status is 'unlocked').

- optimize the scaling coefficients so as to minimize the weighted sum of NSRs for all qualified streams.

n-PSK Phase Ambiguity Removal

Coherent BPSK and QPSK demodulators are inherently incapable of detecting the exact received phase. The received phase is demodulated with a 0,90,180 or 270 deg. ambiguity. Once the demodulator is locked, the phase ambiguity is constant. The transmitted data stream cannot be recovered unless the phase ambiguity is removed. The COM-8003 is capable of detecting and removing the BPSK/QPSK demodulator phase ambiguity while detecting the periodic 32-bit synchronization marker.

Electrical Interface

Inputs/Outputs

Input Module Interface Shared bus	Definition
BUS_CLK_OUT	40 MHz output reference clock for use on the synchronous bus.
BUS_ADDR[3:0]	Bus address. Output (since this module is the bus Master). Designates which slave module is targeted for this read or write transaction. All 1's indicates that the write data is to be broadcasted to all receiving slave modules. Read at the rising edge of BUS_CLK_OUT.
BUS_RWN	Read/Write#. Output (since this module is the bus Master). Indicates whether a read (1) or write (0) transaction is conducted. Read at the rising edge of BUS_CLK_OUT. Read and Write refer to the bus master's perspective.
BUS_DATA[15:0]	Bi-directional data bus. Output when BUS_RWN = '0'. Input when BUS_RWN = '1'. Read latency is 2 bus clock periods. Functional definition during read: - bit 0 SAMPLE_CLK_IN. '1' when 4-bit soft-quantized samples are available. - bits(4:1) DATA_IN(3:0) soft quantized samples from demodulator. MSb is the information bit. 3 LSBs are quality bits. - bits(15:5) undefined
Output Module Interface	Definition
DATA_OUT[3:0]	4-bit soft-quantized demodulated bits. The most significant bit DATA_OUT(3) represents the demodulated information bit while the lower 3-bit represent the demodulated bit quality for use by a subsequent error correction decoder. Unsigned representation: 0000 for maximum amplitude '0', 1111 for

	maximum amplitude '1'.	
BIT_CLK_OUT	Demodulated bit clock. One CLK-wide pulse. Read the output signal at the rising edge of CLK when BIT_CLK_OUT = '1'.	
RX_LOCK	'1' when the demodulator is locked, '0' otherwise.	
CLK_OUT	40 MHz output reference clock.	

Other I/Os

Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 600mA.

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

Complete assemblies can be monitored and controlled centrally over a single serial or, when available through adjacent ComBlocks, LAN/TCP-IP, USB 2.0 or CardBus/PCMCIA connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

This module operates at a fixed internal clock rate f_{clk} of 40 MHz.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

In most applications, the active streams, superframe size and stream delays are fixed values. It is recommended to repower the COM-8003 after modifying these control values.

Parameters	Configuration
Active streams	Enable individual bit streams for combining. Maximum of 4 bit streams can be combined. Bit 0 set to enable bit stream 0. Bit 1 set to enable bit stream 1. Bit 2 set to enable bit stream 2. Bit 3 set to enable bit stream 3. REG0 bits 3-0

Super Frame Length	Number of frames per superframe. The superframe length is identical for all streams. Expressed in integer multiples of frames. Unsigned value. Valid values are restricted to 2,4,8,16,32,64,128. The superframe length is generally selected to be the smallest value consistent with unambiguous time-of-arrival detection at the receiver. A length of 2 is not recommended if phase ambiguity is to be resolved for coherent n-PSK demodulators. REG1 bits 7-0
Delay Stream *n*	Time diversity differential delay for stream *n*. Expressed as number of super frames delayed prior to combining. The sum of the delays within the splitter and combiner must be constant for each active stream so that the streams are re-aligned just prior to combining. The delay is unsigned. 0 is a valid delay. The occupied space within the SDRAM for a given stream buffer is (n+2) superframes. The user is responsible for ensuring that the total occupied space is within the 256MB SDRAM capacity. *n* BITS 15-8 BITS 7-0 0 REG3 REG2 1 REG5 REG4 2 REG7 REG6 3 REG9 REG8
Nominal bit rate (f_{bit_rate})	24-bit signed integer expressed as $f_{bit\_rate} * 2^{24} / f_{clk}$. The nominal bit rate must be stated accurately. Must be greater than the actual received bit rate. Maximum throughput is 6 Mbit/s. REG10 = bit 7-0 (LSB) REG11 = bit 15 – 8 REG12 = bit 23 – 16 (MSB)

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Monitoring

Status monitoring registers are read-only.

Parameters	Monitoring
Synchronization Lock	SREG0 Bit 0 Stream0 SREG0 Bit 1 Stream1 SREG0 Bit 2 Stream2 SREG0 Bit 3 Stream3
Reserved	SREG1
NSR0	Noise to signal ratio for Stream 0.

|	Variance of the 4-bit soft-quantized demodulated samples at the optimum sampling instant averaged over 4096 symbols. Non-linear scale. Approximates 1/SNR. A few reference points: NSR = 24 -> SNR = 8.6 dB NSR = 34 -> SNR = 5.6 dB 8 bit unsigned. SREG2 bits 7 – 0
NSR1	Noise to signal ratio for Stream 1. SREG3 bits 7 – 0
NSR2	Noise to signal ratio for Stream 2. SREG4 bits 7 – 0
NSR3	Noise to signal ratio for Stream 3. SREG5 bits 7 – 0
Combiner scaling coefficients	Combiner scaling coefficient for each stream. Format: 0.4. The sum of all coefficients is expected to be as close as possible to 1.0 (i.e. "10000"). SREG6 bits 3-0: coefficient Stream0 SREG6 bits 7-4: coefficient Stream1 SREG7 bits 3-0: coefficient Stream2 SREG7 bits 7-4: coefficient Stream3
Option o / Version v	Returns '8003ov' when prompted for option o and version v numbers.

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Points	Definition
J4/pin A7	Start Of Frame, stream 0
J4/pin B7	Synchronization Lock, Stream 0
J4/pin A8	Start Of SuperFrame, stream 0
J4/pin B8	Start Of SuperFrame, stream 1
J4/pin A9	Start Of SuperFrame, stream 2
J4/pin B9	Start Of SuperFrame, stream 3

Timing

Clocks

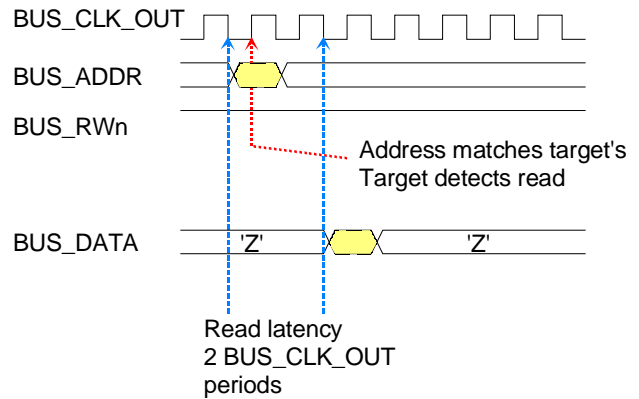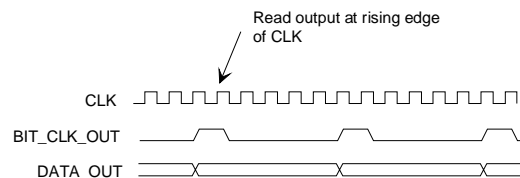The clock distribution scheme embodied in the COM-8003 is illustrated below.
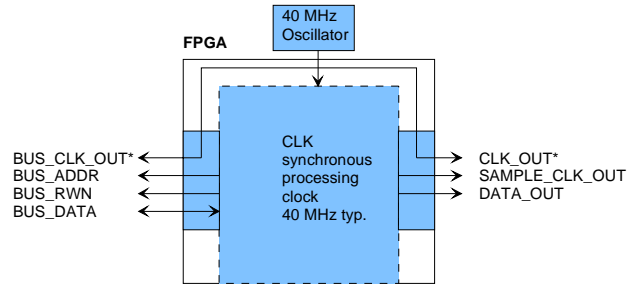
Baseline clock architecture
Darker blue = internal 40 MHz clock
* indicates edge-trigger signal

The core signal processing performed within the FPGA and all the inputs/outputs are synchronous with the 40 MHz internal oscillator.
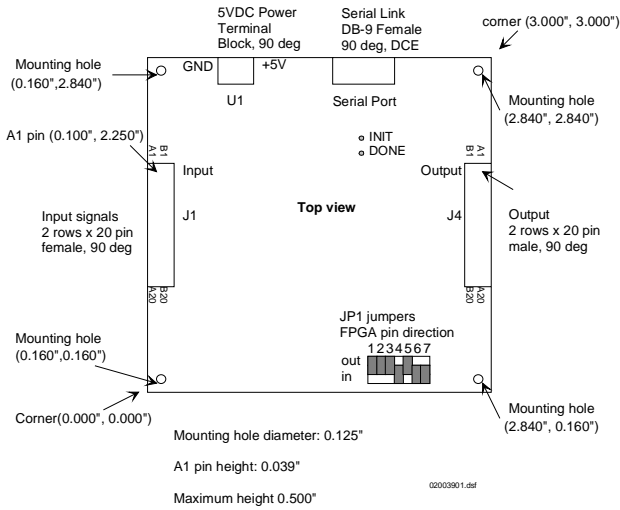
Input

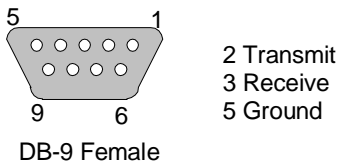## Output

Mechanical Interface

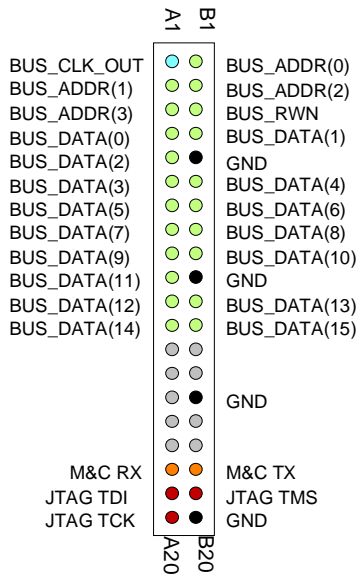Note: All seven JP1 jumpers must be installed in the 'IN' location.

Pinout

Serial Link P1

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.
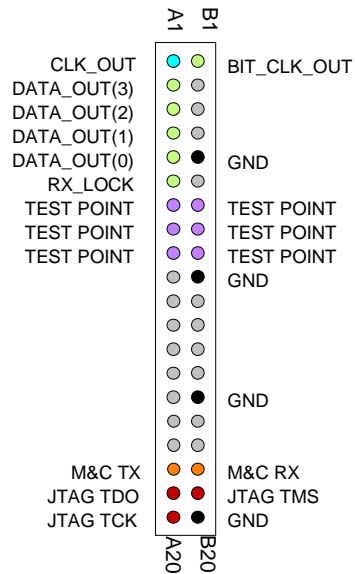

2 Transmit
3 Receive
5 Ground

DB-9 Female

Input Connector J1

	A1	B1	
BUS_CLK_OUT	○	○	BUS_ADDR(0)
BUS_ADDR(1)	○	○	BUS_ADDR(2)
BUS_ADDR(3)	○	○	BUS_RWN
BUS_DATA(0)	○	○	BUS_DATA(1)
BUS_DATA(2)	○	●	GND
BUS_DATA(3)	○	○	BUS_DATA(4)
BUS_DATA(5)	○	○	BUS_DATA(6)
BUS_DATA(7)	○	○	BUS_DATA(8)
BUS_DATA(9)	○	○	BUS_DATA(10)
BUS_DATA(11)	○	●	GND
BUS_DATA(12)	○	○	BUS_DATA(13)
BUS_DATA(14)	○	○	BUS_DATA(15)
	○	○	
	○	○	
	○	●	GND
	○	○	
	○	○	
M&C RX	○	○	M&C TX
JTAG TDI	●	●	JTAG TMS
JTAG TCK	●	●	GND

A20 B20

COM-8003 is bus master. It always drives BUS_CLK_OUT, BUS_ADDR and RD_BUS_RWN.

Output Connector J4

	A1	B1	
CLK_OUT	○	○	BIT_CLK_OUT
DATA_OUT(3)	○	○	
DATA_OUT(2)	○	○	
DATA_OUT(1)	○	○	
DATA_OUT(0)	○	●	GND
RX_LOCK	○	○	
TEST POINT	○	○	TEST POINT
TEST POINT	○	○	TEST POINT
TEST POINT	○	○	TEST POINT
	○	●	GND
	○	○	
	○	○	
	○	○	
	○	●	GND
	○	○	
	○	○	
M&C TX	○	○	M&C RX
JTAG TDO	●	●	JTAG TMS
JTAG TCK	●	●	GND

A20 B20

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-9003 8:1 multiplexing connector	COM-1005 Bit Error Rate Measurement
COM-1001 QPSK/BPSK/OQPSK demodulator	COM-7001 Turbo code decoder
COM-1018 DSSS demodulator	COM-1009 Convolutional decoder K=7, 5
COM-1027 FSK demodulator	

Configuration Management

This specification is to be used in conjunction with VHDL software revision 2.

Acknowledgments

ComBlock Ordering Information

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