COM-8001 ARBITRARY WAVEFORM GENERATOR 40 Msamples/s. VHDL SOURCE CODE OVERVIEW

Overview

The COM-8001 ComBlock Module comprises two pieces of software:

- VHDL code to run within the FPGA for all signal processing functions.
- C/Assembly code running within the Atmel AT90S8515 or ATMega8515L microprocessor for non application-specific monitoring and control functions.

The VHDL code interfaces to the monitoring and control functions by exchanging byte-wide registers on the Atmel microcontroller 8-bit data bus. The control and monitoring registers are defined in the specifications [1].

The Atmel microprocessor code is generic (i.e. non application specific), not user-programmable and functionally transparent to the user. It is thus not described here.

The COM-8001 VHDL code runs on the generic COM-8000 hardware platform. The schematics [2] for this platform are available in this CD.

Reference documents

[1] specifications: com8001.pdf

[2] hardware schematics: com_8000schematics.pdf

[3] VHDL source code in directory
com-8001_011\src

[4] Xilinx ISE project files
com-8001_011\com-8001_a.npl
com-8001_011\com-8001_b.npl

[5] .ucf constraint files
com-8001_011\src\root_arb_waveform_gen_a.ucf.ucf
com-8001_011\src\root_arb_waveform_gen_b.ucf.ucf

[6] .mcs FPGA bit files
8001_011\com8001A_011.mcs
8001_011\com8001B_011.mcs

Configuration Management

The current software revision is 11.

Configuration Options

In order to provide configuration flexibility without unduly increasing the hardware complexity, some features require generating different firmware versions. In particular, the COM-8001 can be equipped with 256 MB SDRAM (-A option) or 1 GB SDRAM (-B option). Most source files are common to both options. These common files are located in the source directory 8001_011\src\. Files specific to the –A or –B option are stored in the subdirectories 8001_011\src\a\ and 8001_011\src\b\ respectively.

Two Xinlix project files are used [4], one for each option.

VHDL development environment

The VHDL software was developed using the Xilinx ISE 6.3 development environment. The synthesis tool is XST.

Target FPGA

The VHDL code was synthesized for the Xilinx Spartan-IIE XC2S300E-6PQ208 FPGA.

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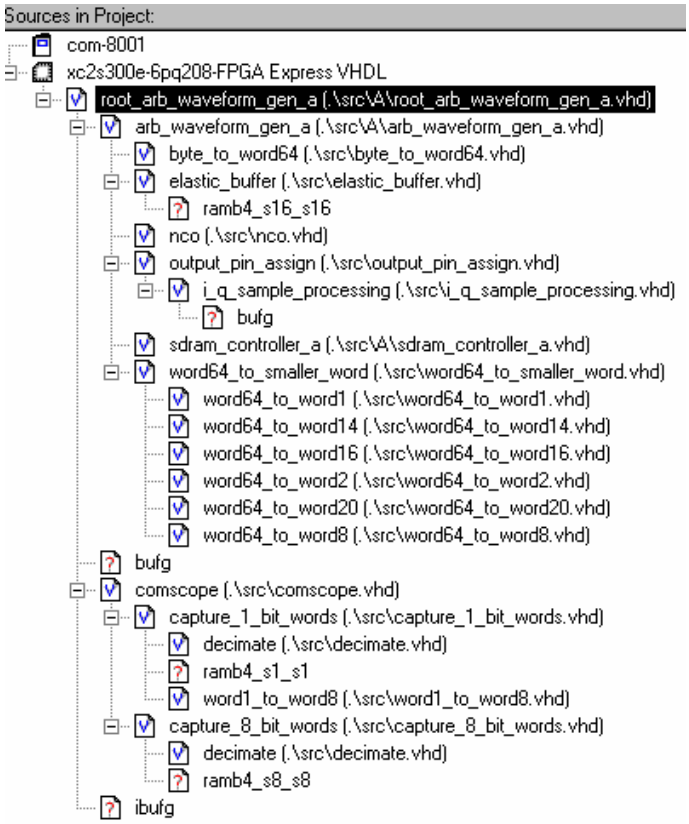
Xilinx-specific code

The VHDL source code was written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- BUFG
- IBUFG
- RAMB4_S16_S16
- RAMB4_S8_S8
- RAMB4_S1_S1

VHDL software hierarchy



The code is stored with one, and only one, entity per file as shown above.

The root program (highlighted) is *root_arb_waveform_gen_a.vhd.*

Clock / Timing

The software uses a single 40 MHz clock, CLK_IN2, as provided externally through pin A1 of the J1 input connector. CLK_IN2 served a triple purpose: (a) internal processing clock, (b) synchronous input clock and (c) synchronous output clock. The code is written to meet the timing requirements on the target FPGA at a speed of at least 40 MHz.

Principle of operation

The code is written for interfacing with generic SDRAM memories. A set of specifications can be obtained from Micron (MT48LC16M16A2 – 4 MEG X 16 X 4 BANKS). The clock provided to the SDRAM is 40 MHz, well below the specified maximum for PC100/PC133 SDRAMs.

Data transfers are done in burst of 4 read or 4 write (64bit wide x 4 = 32 bytes). Therefore, user defined start and stop addresses must be multiple of 32-bytes.

In addition to the burst read, burst write operations, the software takes care of the initial SDRAM initialization and of periodic auto refresh.

Several VHDL components (named *word64_to_wordx.vhd*) are used to break the 32-byte burst into samples of user-defined widths. The widths currently supported are as follows:
1-bit, 2-bits, 8-bits, 14-bits, 16-bits, 20-bits.

FPGA Occupancy

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Design Summary
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Number of errors:      0
Number of warnings:   81
Logic Utilization:
  Total Number Slice Registers:   2,288 out of  6,144   37%
    Number used as Flip Flops:                2,287
    Number used as Latches:                       1
  Number of 4 input LUTs:         4,650 out of  6,144   75%
Logic Distribution:
    Number of occupied Slices:                        2,889 out of  3,072   94%
    Number of Slices containing only related logic:   2,889 out of  2,889  100%
    Number of Slices containing unrelated logic:          0 out of  2,889    0%
        *See NOTES below for an explanation of the effects of unrelated logic
Total Number 4 input LUTs:        4,907 out of  6,144   79%
      Number used as logic:                   4,650
      Number used as a route-thru:              257
   Number of bonded IOBs:           136 out of    142   95%
      IOB Flip Flops:                         168
   Number of Tbufs:                  15 out of  3,200    1%
   Number of Block RAMs:             12 out of     16   75%
   Number of GCLKs:                   4 out of      4  100%
   Number of GCLKIOBs:                3 out of      4   75%

Total equivalent gate count for design:  247,954
Additional JTAG gate count for IOBs:  6,672
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Contact Information

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