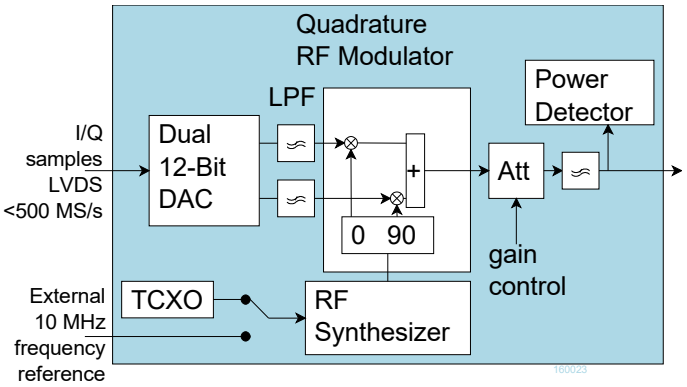
COM-4009 DIGITAL TO [400 MHz – 4.4 GHz] BROADBAND RF MODULATOR

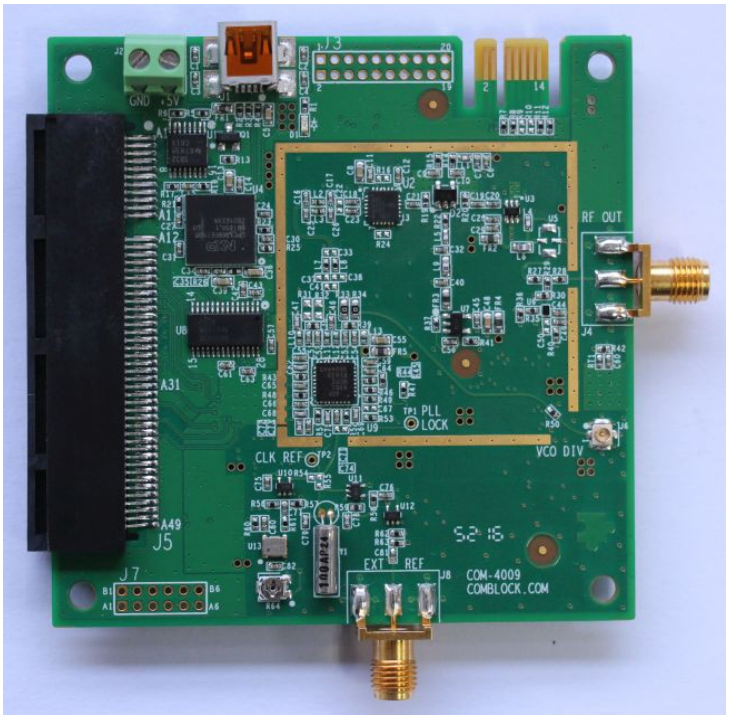


Key Features

- Broadband quadrature modulator, including DACs, agile frequency synthesizer, quadrature RF modulator and output power detector.
- Software tunable in the range 400 MHz – 4.4GHz by steps of 5 KHz or less. Customizable output harmonics rejection filter on request.
- Dual 12-bit 500 Msamples/s DACs. LVDS digital input for direct connection with FPGA module.
- Wideband modulation bandwidth > 200 MHz
- Built-in output power detector and temperature sensor.
- 8 preset frequencies for fast (200µs) frequency hopping.
- Internal 2.5ppm TCXO frequency reference (before calibration), or external 10 MHz frequency reference.
- USB Monitoring & Control Interface
- Single +5V_{DC} supply.
- Connectorized 3”x 3” module for ease of prototyping
- SMA output connector
- RS232 (3tx/5rx) and RS422 (4rx) drivers

For the latest data sheet, please refer to the **ComBlock** web site: comblock.com/com4009.html.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .



(shown without shield)

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Electrical Interface

Inputs / Outputs

Input Module Interface	Definition
D(0:31)	16 differential pairs, LVDS input. The 4 least-significant bits D(0:7) are unused. I and Q samples are alternating: I is sent first after the rising edge of the clock, Q is sent at the following edge. Format: 2's complement
DCI(0:1)	I/Q selector, LVDS input. '1' to indicate that the I sample is currently sent on the data bus D, '0' while the Q sample is sent.
CLKREF(0:1)	DAC sampling clock. LVDS input. Maximum frequency: 500 MHz.
DCO(0:1)	DAC sampling clock output, LVDS. A delayed version of CLKREF generated by the dual DAC.
EXT_REF	Optional input. External 10 MHz frequency reference for frequency synthesis. Sinewave, clipped sinewave or squarewave. J8 SMA male connector. 50 Ohm. Input is AC coupled. Minimum level 0.6Vpp. Maximum level: 3.3Vpp.

Analog Output Signals	Definition
RF_OUT	Modulated RF outputs. 400 MHz – 4.4GHz Maximum output level: +4 dBm. Impedance: 50 Ohms. SMA female connector
Control Lines	**Definition**
PDN	Power down input. Active low. As this control signal is slow to enact, it can rarely be used to switch off RF output in bursts application. In this case, use the fast TX_EN control instead. Connector J5 Pin A1.
TX_EN	Low-voltage TTL input control. Used to turn all outputs on/off. Level signal: 3.3V = ON, 0V = OFF Response time 200 µsec On/Off rejection > 83 dB. Connector J5 Pin A2. Pulled high by default.
FREQ_HOP	Low-voltage (3.3V / 0V) TTL input control. Pulled low by default. A short '1' pulse will cause the COM-4009 to jump to the next frequency by incrementing the modulo- N_{freq} frequency pointer (where N_{freq} is defined in control Register 35) RF frequency 0 -> RF frequency 1 -> RF frequency 2 -> RF frequency 0 > etc… Rising-edge triggered. Minimum pulse width: 10 µsec. The signal must be returned to zero as soon as possible as it impedes the module's communication ability. Connector J5 Pin A3.
USB Monitoring & Control	Mini-USB connector (type AB); Full speed / Low Speed
Power Interface	4.9 – 5.5VDC. Terminal block. Power consumption is 400mA.

Absolute Maximum Ratings

Supply voltage	-12V min, +5.8V max
12-pin connector digital inputs	-0.3V min, +5.0V max
EXT_REF	-0.3V min, +3.6V max

Configuration

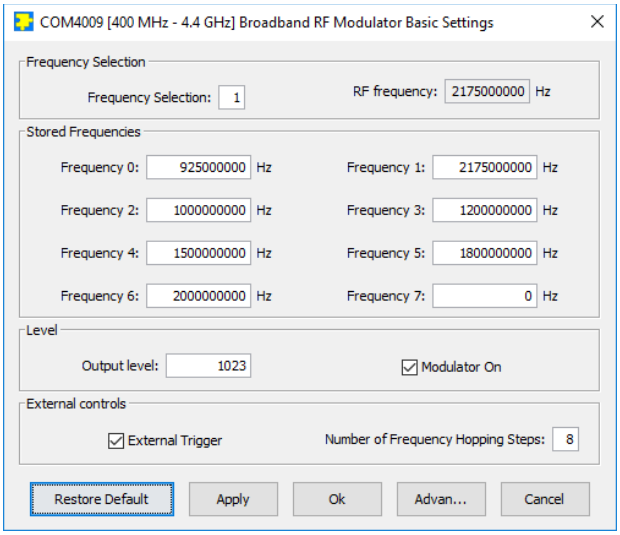
Complete ComBlock assemblies can be monitored and controlled centrally over a single USB connection using the **ComBlock Control Center** software. A mini USB cable is supplied.

The COM-4009 can also be monitored and controlled through adjacent ComBlocks using LAN/TCP-IP , USB, Serial or CardBus connection.

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-4009 is to use the ComBlock Control Center software supplied with the module(s). In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-4009 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Up to eight frequencies can be stored within each module at any given time. The current frequency is selected by an index in the range 0 to 7. Frequencies must be integer multiples of the RF synthesizer step size.

A basic frequency hopping scheme can be enabled by

(a) enabling the external trigger

(b) entering the number of frequency hopping steps in the round-robin arrangement.

For example, by specifying 4 steps, the modulator center frequency will follow the following index sequence: 0,1,2,3,0,1,2,3,0,1, etc., the index being incremented at the rising edge of each external FREQ_HOP pulse.

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Programmers developing custom applications (using the ComBlock API instead of the supplied ComBlock control center graphical user interface) should know that frequency changes are enacted upon (re-)writing to the REG6

Parameters	Configuration
RF frequency 0	Preselected frequency 0. Range 400 MHz – 4.4GHz, expressed in Hz. REG0 (LSB) – REG3 (MSB)
Output level	10-bit control. Dynamic range: 41.8 dB @ 400 MHz (typ.) 40 dB @ 0.5GHz (typ.) 33.3 dB @ 1GHz (typ.) 27.5 dB @ 2GHz (typ.) 26.5 dB @ 3GHz (typ.) REG4 LSB REG5(1:0) MSB
Modulator on/off	0 = OFF, 1 = ON Another method to turn all modulators on/off simultaneously is to use the TX_EN external control on the J5 connector. REG5(7)
External controls enabled/disabled	Enable or disable the PDN, FREQ_HOP and TX_EN external controls on the J5 connector. 0 = external controls disabled 1 = external controls enabled REG6(0)
Frequency selection	Use to switch local oscillator frequency among preselected values. Note: the external FREQ_HOP control may override this selection.
	Range 0 through 7 REG6(7:5)
RF frequency 1	Preselected frequency 1. Same format as RF frequency 0. REG7(LSB) – REG10(MSB)
RF frequency 2	Preselected frequency 2. Same format as RF frequency 0. REG11(LSB) – REG14(MSB)
RF frequency 3	Preselected frequency 3. Same format as RF frequency 0. REG15(LSB) – REG18(MSB)
RF frequency 4	Preselected frequency 4. Same format as RF frequency 0. REG19(LSB) – REG22(MSB)
RF frequency 5	Preselected frequency 5. Same format as RF frequency 0. REG23(LSB) – REG26(MSB)
RF frequency 6	Preselected frequency 6. Same format as RF frequency 0. REG27(LSB) – REG30(MSB)
RF frequency 7	Preselected frequency 7. Same format as RF frequency 0. REG31(LSB) – REG34(MSB)
Number of RF frequencies Nfreq in the scanning list	Each time a FREQ_HOP pulse is received, the frequency pointer increments modulo Nfreq. Nfreq is in the range 1 – 8. REG35(3:0)
RS232 driver enable	Set to zero to save power when the application does not use the RS232 signals. 0 = disabled 1 = enabled REG6(1)
RS422 driver enable	Set to zero to save power when the application does not use the RS422 signals. 0 = disabled 1 = enabled REG6(2)

Status Registers

Parameters	Monitoring
Power supply faults	Returns 3F or 3B when all internal supply voltages are within nominal range. SREG0(5:0)
PLL lock status	A persistent '1' indicates that the frequency synthesizer is locked to the frequency reference. SREG1(0)
Power measurement	10-bit number. The higher the number, the lower the power. The power measurement linearity is shown below. SREG2(7:0): bits 7-0 (LSB) SREG3(1:0): bits 9-8 (MSB)
Temperature measurement	Temperature (°C) measured at the

	modulator integrated circuit. 10-bit number. SREG4(7:0): bits 7-0 (LSB) SREG5(1:0): bits 9-8 (MSB)

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
CLK_REF (TP2)	Internal 19.2 MHz VCTCXO / External 10 MHz frequency reference clock, depending on the module configuration selected at the time of order.
PLL_LOCK (TP1)	Frequency synthesizer PLL lock status. Active high: '1' when locked. This information is also available in status register SREG1

Operations

Internal vs External Frequency Reference

An internal VC-TXCO provides a ±2.5ppm temperature-stable 19.2 MHz frequency reference to the RF frequency synthesizer. In addition, small calibration adjustments are possible through the trimming potentiometer R64.

If the internal TCXO stability is not sufficient for the target application, the RF frequency synthesizers can be driven by an external 10 MHz higher-stability frequency reference. The external frequency reference selection requires moving a surface mount resistor from R55 to R54. Please let us know at the time of order if an external frequency reference is preferred.

When configured for external 10 MHz frequency reference, the COM-4009 will automatically select between external 10 MHz (when present) and internal 10 MHz. However, the internal 10 MHz crystal oscillator stability is only about 10 ppm.

Tuning Step Size

The frequency translation is user programmable in the range of 400 MHz to 4.4 GHz. The step size depends on the selected frequency as listed below:

Tuning frequency	Step size
2.2 to 4.4 GHz	5 KHz
1.1 to 2.2 GHz	2.5 KHz
550 MHz to 1.1 GHz	1.25 KHz
275 MHz to 550 MHz	625 Hz
137.5 MHz to 275 MHz	312.5 Hz
68.75 MHz to 137.5 MHz	156.25 Hz

Minimum Frequency

The COM-4009 is capable of tuning in the range 68.75 MHz to 4.4 GHz. However, the sideband suppression is quite poor when operated below the specified 400 MHz lower limit. See the specifications for the ADL5375 quadrature modulator for more details

http://www.analog.com/media/en/technical-documentation/evaluation-documentation/ADL5375.pdf

Input level

The recommended maximum digital input level is –16K to +16K, that is half of the full 16-bit signed range. No damage will occur while using the full 16-bit range, but linearity will be affected.

Gain / Output Level Calibration

The COM-4009 output level is controlled by software.

To assist the user in calibrating the output levels, power measurements are displayed in the status panel.

Red LED

A red led will normally turn on for two seconds at power up. It will also turn on when one or more fault condition occurs:

- Power supply out of range
- RF synthesizer out of lock

Performance

Internal Clock Reference

The internal VCTCXO frequency reference performance is as follows:

- temperature stability (-30°C to +75°C): ± 2.5 ppm max
- aging: ±1ppm max/year

The design includes a trimmer potentiometer R64 to remove fixed known offsets through calibration.

Modulation

Quadrature phase error: 1.7 deg typ (@450 MHz)
Quadrature phase error: < 0.4 deg typ above 900 MHz
I/Q amplitude balance error: < 0.1 dB

ON/OFF rejection (using modulator on/off command only): > 85 dB typ.

Dynamic range
-30.5 to 11.3 dBm @ 400 MHz
-29.5 to 10.5 dBm @ 500 MHz
-25.5 to 7.8 dBm @ 1 GHz
-21.5 to 6 dBm @ 2 GHz
-23 to 3.5 dBm @ 3 GHz

LO leakage (Carrier feedthrough) at output, (0 dBm output)

-60 dBc @ 400 MHz, typ.
-66 dBc @ 500 MHz, typ.
-53 dBc @ 1 GHz, typ.
-43 dBc @ 2 GHz, typ.
-34 dBc @ 3 GHz, typ.

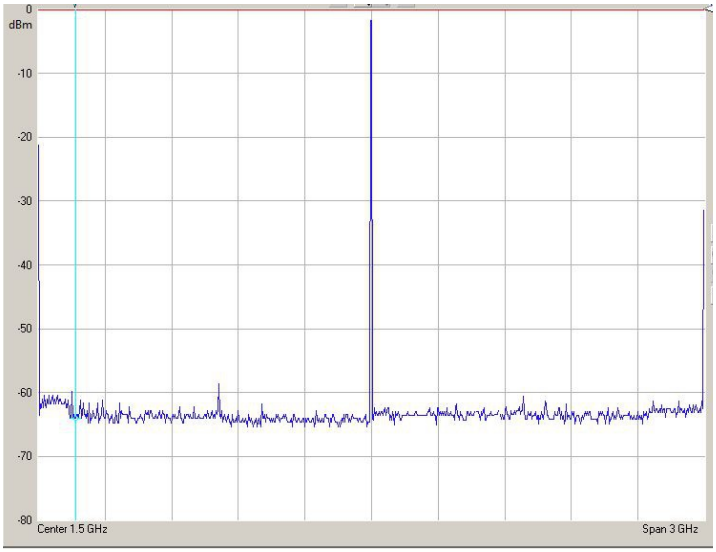
Sideband suppression:

-14 dBc @ 400 MHz, typ.
-21 dBc @ 500 MHz, typ.
-32 dBc @ 1 GHz, typ.
-65 dBc @ 2 GHz, typ.
-37 dBc @ 3 GHz, typ.

Modulation bandwidth:

±50 MHz @0.1dB
±500 MHz @1dB
±600 MHz @2dB
±700 MHz @3dB

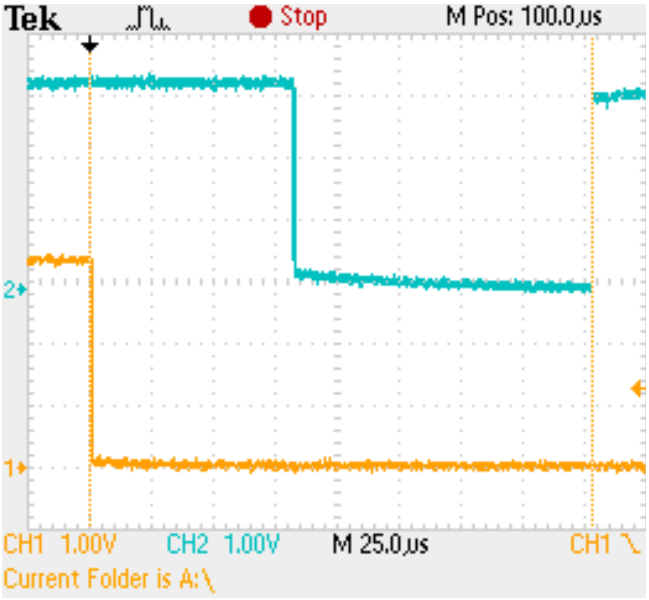
Out-of-band spurious spectral lines: < -60 dBc



Output spectrum 0 – 3GHz. 10 KHz resolution bandwidth. 1.5 GHz modulated output (0 dBm).

Frequency Synthesizer

LO frequency switching time using the FREQ_HOP signal: 203µs



Frequency hop using the FREQ_HOP signal
Yellow trace: FREQ_HOP control signal
Blue trace: RF synthesizer lock status

Phase noise @ 400 MHz
< -94 dBc/Hz @ 1 KHz
< -93 dBc/Hz @ 10 KHz
< -103 dBc/Hz @ 100 KHz

Phase noise @ 2.28 GHz
< -87 dBc/Hz @ 1 KHz
< -84 dBc/Hz @ 10 KHz
< -95 dBc/Hz @ 100 KHz

Phase noise @ 3 GHz
< -82 dBc/Hz @ 1 KHz
< -86 dBc/Hz @ 10 KHz
< -92 dBc/Hz @ 100 KHz

Above phase noise measured using the 19.2 MHz VCTCXO internal frequency reference.
Similar phase noise performance are obtained with internal and external 10 MHz frequency references.

For best phase noise, the DAC sampling frequency should be selected at least 100KHz away from integer multiples of the reference frequency (19.2 or 10 MHz).

Harmonics

Users should be aware of the strong odd harmonics. Harmonics at three, five, seven times the modulator frequency are typically in the range of –10 to –20 dBc. Depending on the application, these harmonics may fall in the band of interest and external filtering may be required.

At the time of order, please specify the maximum output frequency. We will install the appropriate harmonics rejection filter accordingly.

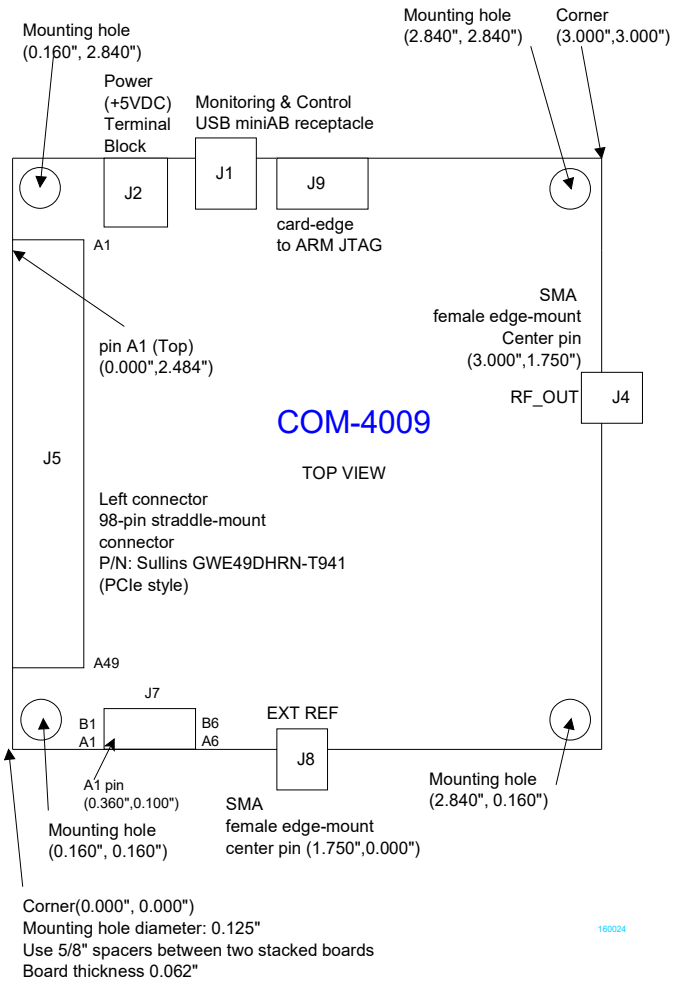
Power measurement

Accuracy (no correction, unmodulated CW carrier):
±0.5 dB
Video bandwidth: 3.5 MHz

Schematic

The board schematic is available on-line at
comblock.com/download/com_4009schematics.pdf

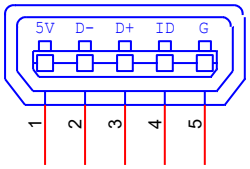
Mechanical Interface



Pinout

Mini USB Connector J1

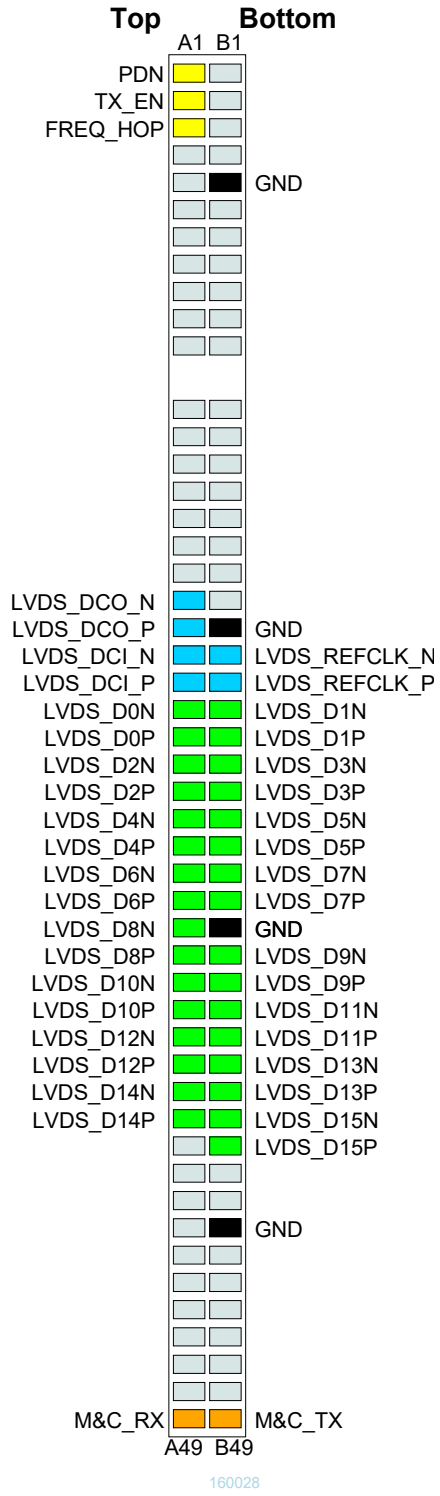
The COM-4009 is a USB device with a mini type AB connector. (G = GND)



Input Connector J5

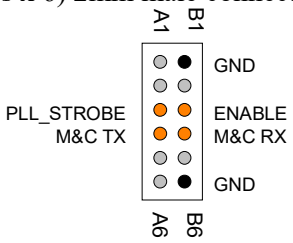
98-pin Female Connector.

This module is designed for direct connection to the COM-18xx modules.



Connector J8

12-pin (2 rows x 6) 2mm male connector.



I/O Compatibility List

(not an exhaustive list)

Input
COM-1800 FPGA + GbE LAN development platform
COM-1806 Wideband signal capture & playback
COM-1827 CPM (FSK,MSK,etc) modem

ComBlock Ordering Information

COM-4009	DIGITAL TO [400 MHz – 4.4 GHz] BROADBAND QUADRATURE MODULATOR

At the time of order, please specify:

- the maximum output frequency. We will install the appropriate harmonics rejection filter accordingly.
- Reference clock configuration: internal TCXO or 10 MHz

ECCN: 5A991.b

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