COM-3505 Dual-Band 2.4/5 GHz 2x2 MIMO Transceiver

Key Features

- Dual-Band half-duplex transceiver.
  - 2.4 – 2.5 GHz
  - 4.9 – 5.85 GHz
  - –85 dBm sensitivity
  - +15 dBm usable power at 5GHz
  - +18 dBm usable power at 2.4 GHz
  - Tx/Rx switch time < 2µs
  - Bandwidth: 40 MHz
- Two simultaneous channels can be configured
  - as 2x2 MIMO, or
  - as independent channels with distinct center frequencies.
- Baseband interface: differential analog signal
- RF interface: 50 Ohm SMA antenna port.
- USB port for monitoring and control.
- Only single +5V_{DC} supply required. Connectorized 3”x 3” module for ease of prototyping

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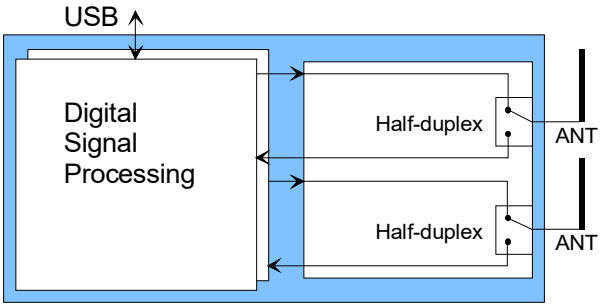
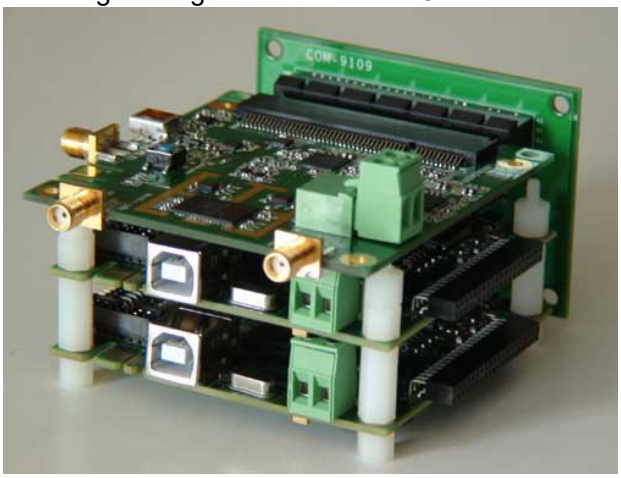
Applications Examples

3-module 2x2 MIMO configuration

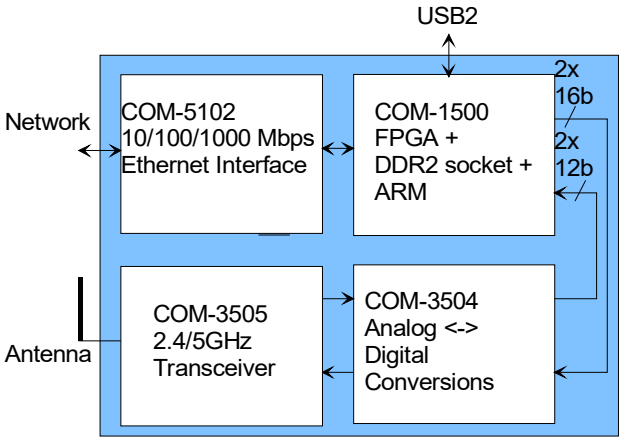


COM-1200 *2
FPGA + USB2 +
Analog <-> Digital

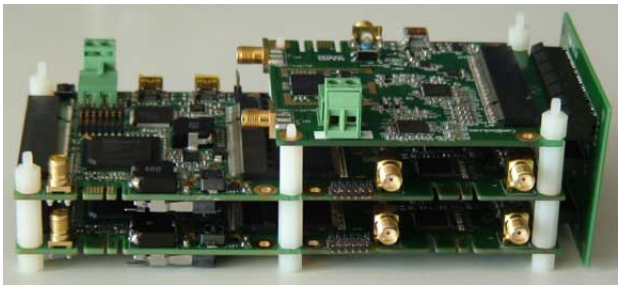
COM-3505
Dual-Band 2.4/5GHz
2x2 MIMO Transceiver



1 channel high-performance signal processing



2x2 MIMO configuration, Large Xilinx Spartan-6 FPGAs

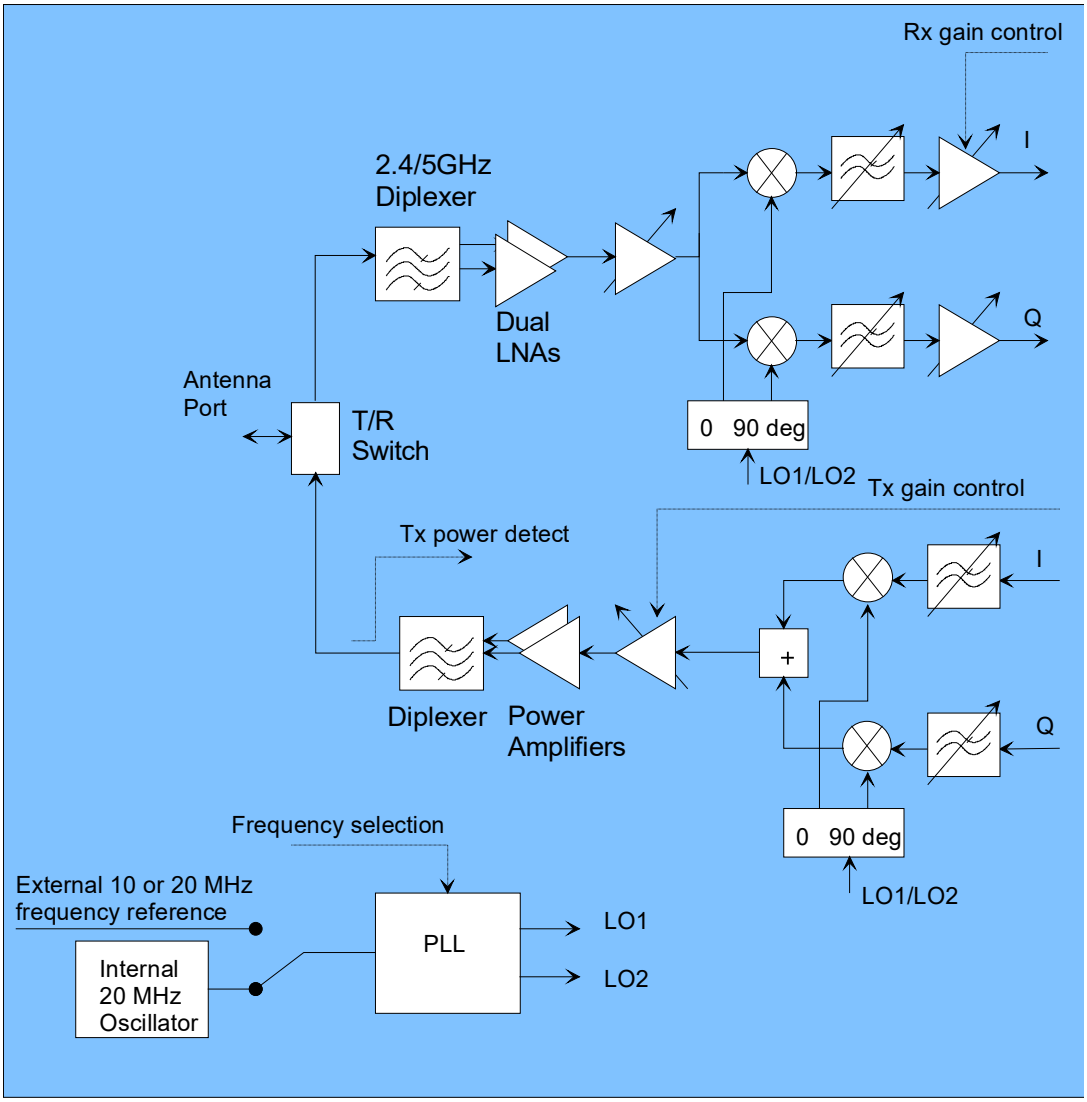


2(COM-1500 + COM-3504) + COM-3505

For the latest data sheet, please refer to the **ComBlock** web site: comblock.com/com3505.html.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to comblock.com/product_list.html

Block Diagram (1 of 2 channels)



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Electrical Interface

Baseband Interface 98-pin J3	**Definition**
RX*x*_I_P / RX*x*_I_N RX*x*_Q_P / RX*x*_Q_N	Channel*x* differential outputs. (_P for +, _N for -), -), I for in-phase, Q for quadrature. 2Vpp maximum differential voltage (1Vpp on each RX*x*_P and RX*x*_N signal). Load minimum differential resistance: 10 KOhm. AC-coupled. Receiving end is responsible for biasing these signals to the desired common mode voltage. –3dB cut-off frequency: 100 Hz.
TX*x*_I_P / TX*x*_I_N TX*x*_Q_P / TX*x*_Q_N	Channel*x* differential inputs. (_P for +, _N for -), I for in-phase, Q for quadrature. Full range 2.0Vpp differential (1.0Vpp on each TX*x*_P and TX*x*_N signal). AC-coupled inputs. Input impedance: 60 KOhm.
RX*x*_RSSI	Channel*x* received RF signal strength output. Analog output. Range 0.5 – 2.5V Slope: 22.5mV/dB Settling time < 1us
RX*x*_AGC	Receiver gain control. Analog input in the range 0 – 3.3V. Range > 90 dB log scale. 0V yield the maximum gain. Meaningful only when selecting the external AGC loop mode. Ignored otherwise.
RX_TXN*x*	Receive/Transmit# selection. '0' = transmit '1' = receive. Controls the T/R switch. LVTTL input. Recommended guard time: 5us.
TX*x*_POWER_DET	Transmitter directional power detection. Represents a measurement in the range 0 – 20 dBm prior to the Tx/Rx antenna switch. 1 dB accuracy. Analog output in the range 0.35 – 0.9V. Non-linear scale.
TX*x*_GAIN_CTRL	Transmitter gain control. Analog input in the range 0 – 3.3V. Range: 30 dB Non-linear scale. 3.3V yield the maximum gain.
FREQ_STROBE*x*	Low-voltage (3.3V / 0V) TTL input control. Used to increment the modulo-N_{freq} frequency pointer (where N_{freq} is defined in Register 35) RF frequency 0 ->RF frequency 1 ->RF frequency 2 ->RF frequency 0 > etc… Rising edge triggered. Minimum pulse width: 10 µsec.
Antenna port	**Definition**
ANT*x*	50 Ohm, SMA female connector with standard thread (i.e. not compatible with a reverse thread antenna). Rx sensitivity: -85 dBm Maximum input level: + 10 dBm Usable tx power: +15 dBm @ 5 GHz +18 dBm@ 2.4 GHz
External frequency reference	**Definition**
FREQ_REF*x*	Optional higher-stability external frequency reference. 10 MHz or 20 MHz.

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	Sinewave, clipped sinewave or squarewave. J6 SMA female connector. 50 Ohm. Minimum level: 2Vpp. Maximum level: 3.3Vpp.
Other Interfaces	**Definition**
USB Monitoring & Control	Mini-USB connector Type AB Full speed / Low Speed
Power Interface	4.75 – 5.75V_{DC}; Terminal block Power consumption is 500 mA 2ch receive only 1300 mA 1ch transmit 2500 mA 2ch transmit at maximum powermA

Absolute Maximum Ratings

Supply voltage	-8V min, +6.5V max
Baseband input signals	-0.3V min, +3.6V max
ANT input	+10 dBm

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB (requires a mini-USB cable)

or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

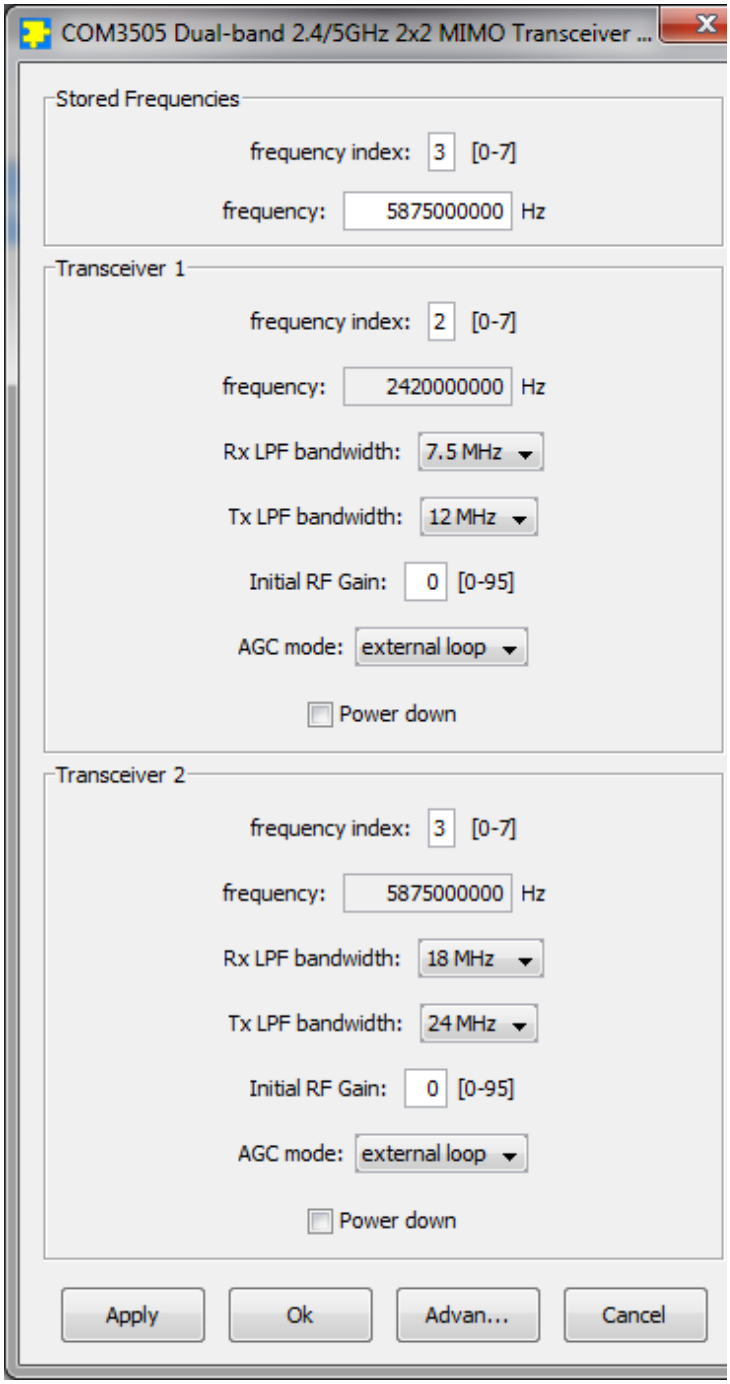
Configuration (Basic)

The easiest way to configure the COM-3505 is to use the **ComBlock Control Center** software supplied with the module on CD. In the ComBlock Control Center window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-3505 module to be configured and click the *Settings* button to display the *Basic Settings* window shown below.

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

The module configuration parameters are stored in non-volatile memory. All control registers are read/write. Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.



Basic Settings Window

Channel 1	
Parameters	**Configuration**
Frequency translation index	Select the frequency translation value by pointing to one of eight pre-selected frequencies stored as Frequency 0 through 7. Writing to this register causes the frequency synthesizer to be reprogrammed. REG0(2:0)
Power Down	0 = normal operation 1 = power down REG0(7)
Receive AGC loop selection	Select the receive AGC loop. 0 = open loop. The receive gain is fixed according to the value set in control register REG2. 2 = external AGC loop. Follow-on modules (demodulator for example) adjust the receive gain based on the supplied RX_RSSI information and other salient level information such as RX_I/Q level, possible saturation at the external A/D converter, etc. The gain control signal is RX1_AGC. REG1(1:0)
Rx-only or Tx-only modes	Generally, the transceiver is configured to switch rapidly between transmit and receive mode under control of the external RX_TXN1 signal. For applications requiring transmit only or receive only mode of operation, the mode can be fixed by this control register. 0 = as controlled by RX_TXN1 1 = receive-only. RX_TXN1 ignored 2 = transmit-only. RX_TXN1 ignored REG1(3:2)
Receiver low-pass filter programmable bandwidth	LPF -3dB corner frequency (one-sided bandwidth). 00 = 7.5 MHz 01 = 9.5 MHz 10 = 14 MHz 11 = 18 MHz REG1(5:4)
Transmitter low-pass filter programmable bandwidth	LPF -3dB corner frequency (one-sided bandwidth). 00 = 12 MHz 01 = 18 MHz 10 = 24 MHz REG1(7:6)
Initial receive gain	Initial receiver RF gain (before the AGC takes over). Approximately 2 dB steps. REG2(6:0)
Channel 2	
Parameters	**Configuration**
Same parameters as for channel 1.	Use REG3/4/5 (with the same definitions as REG0/1/2 for channel 1.
Common controls (all channels)	
Parameters	**Configuration**
Analog test point selection	Select which analog signal is to be monitored at the multi-purpose test point labeled TPA: 0= disabled (for slightly faster AGC response) 1 = RX1_RSSI 2 = RX2_RSSI 3 = RX1_AGC 4 = RX2_AGC 5 = TX1_GAIN_CTRL 6 = TX2_GAIN_CTRL 7 = TX1_POWER_DET 8 = TX2_POWER_DET See schematics for more details about these signals. REG6(3:0)
Stored up-conversion frequencies	
Frequency 0 f_0	Frequency translation between the baseband and RF inputs/outputs. The RF frequency synthesizers are reprogrammed upon (re-)writing to the frequency translation index register (REG0/3) Valid ranges: 2412 - 2500 MHz 4900 – 5350 MHz 5470 - 5875 MHz Expressed in units of 2 Hz Steps of 228Hz (2.4GHz band) or 382 Hz (5GHz band) REG8: bits 7:0 (LSB) REG9: bits 15:8 REG10: bits 23:16

	REG11: bits 31:24 (MSB)
Frequency 1	Same format as Frequency 0 REG12 (LSB), REG13, REG14, REG15(MSB)
Frequency 2	Same format as Frequency 0 REG16 (LSB), REG17, REG18, REG19(MSB)
Frequency 3	Same format as Frequency 0 REG20 (LSB), REG21, REG22, REG23(MSB)
Frequency 4	Same format as Frequency 0 REG24 (LSB), REG25, REG26, REG27(MSB)
Frequency 5	Same format as Frequency 0 REG28 (LSB), REG29, REG30, REG31(MSB)
Frequency 6	Same format as Frequency 0 REG32 (LSB), REG33, REG34, REG35(MSB)
Frequency 7	Same format as Frequency 0 REG36 (LSB), REG37, REG38, REG39(MSB)
Number of RF frequencies N_{freq} in the scanning list	Each time a FREQ_STROBE pulse is received, the frequency pointer increments modulo N_{freq}. N_{freq} is in the range 1 – 8. REG40

Monitoring

Monitoring the status of the COM-3505 is performed by viewing the S*tatus* window in ComBlock Control Center. All register values are displayed in hexadecimal, but other formats are displayed by hovering over the hex value with the cursor.

Parameters	Monitoring
Internal Power Supply Fault	0 = Normal Operation 1 = Fault Condition SREG0(0)
RF synthesizers lock detect	1 indicates that the frequency synthesizer is locked. SREG1(0): ch1 synth. lock SREG1(1): ch2 synth. Lock
Channel 1 RSSI	SREG2
Channel 2 RSSI	SREG3
Channel 1 rx gain	SREG4 Range 0 - 95
Channel 2 rx gain	SREG5 Range 0 – 95
Channel 1 tx power detection	Transmit power detection. Range 0 to 20 dBm. 1dB accuracy. Inverted scale: 0 = 0 dBm 0 = 20 dBm@2.4 GHz 0 = 18 dBm @ 5 GHz Valid only while transmitting. SREG6: LSB SREG7(3:0): MSB
Channel 2 tx power detection	SREG8: LSB SREG9(3:0): MSB

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
RX1_I / TP2	Received ch1 baseband in-phase signal
RX1_Q / TP3	Received ch1 baseband quadrature signal
RX1_RSSI / TP4	Received ch1 signal strength
RX2_I / TP5	Received ch2 baseband in-phase signal
RX2_Q / TP6	Received ch2 baseband quadrature signal
RX2_RSSI / TP7	Received ch2 signal strength
TPA	Multi-purpose analog test point. Represents one of several analog signals as selected using control register REG6

Operations

Internal vs External Frequency Reference

An external 10 MHz frequency reference can be used when the user application requires high frequency stability. In this case, simply connect a 10 MHz sinewave, clipped sinewave or square wave to the J6 EXT-REF SMA connector. Detection is automatic, thus no configuration change is needed. Upon removal of the external 10 MHz frequency reference signal, the COM-3505 automatically reverts to the internal frequency reference.

Receive Gain Control

The receiver AGC loop is split between this module and an external 'brain' (external AGC loop). This module is the gain actuator while the gain adjustment decision is taken by an external circuit based on various sensors, including the RX_RSSI received level, RX_I/Q level, etc. The gain control signals are RX1_AGC and RX2_AGC for transceiver 1 and 2 respectively.

The receiver AGC loop can also be open while the user defines a fixed receiver gain.

Frequency Hopping

Frequency Strobe allows for quick jumps of up-conversion frequencies among 8 pre-selected values. Switching is in a "round robin" fashion sequentially through up to 8 frequencies (the actual number of frequencies in the round robin pool is set by N_{freq}. For example, when $N_{freq} = 3$, the up-conversion frequencies will be selected in the following index sequence: 0,1,2,0,1,2,0,1,2…

FREQ_STROBE is an edge-triggered signal. FREQ_STROBE pulse width should be at least 62.5nS long. Switching time using the FREQ_STROBE signal is < 500µs.

Schematics

The schematics are available on the ComBlock CD shipped with every module (in the "Hardware schematics" folder).

Performance

Internal Clock Reference

The internal crystal performance is as follows:

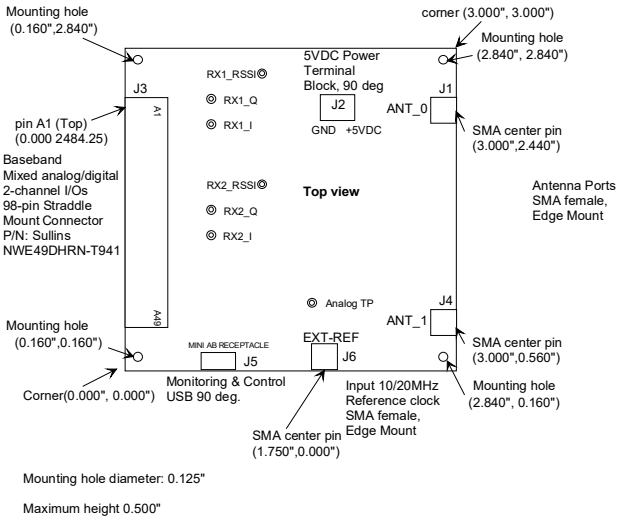
- tolerance: [-5 to +15] ppm max @25°C
- temperature stability (-10°C to +60°C): ± 50 ppm max
- aging: ±5ppm/year max (1st year) @25°C

Frequency Synthesizer

Phase noise @2.4GHz:
-89 dBc/Hz @ 1KHz from the carrier
-90 dBc/Hz @ 10 KHz from the carrier
-90 dBc/Hz @ 100 KHz from the carrier

Phase noise @5GHz
-86 dBc/Hz @ 1KHz from the carrier
-86 dBc/Hz @ 10KHz from the carrier
-86 dBc/Hz @ 100KHz from the carrier

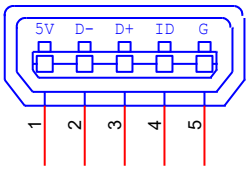
Mechanical Interface



Pinout

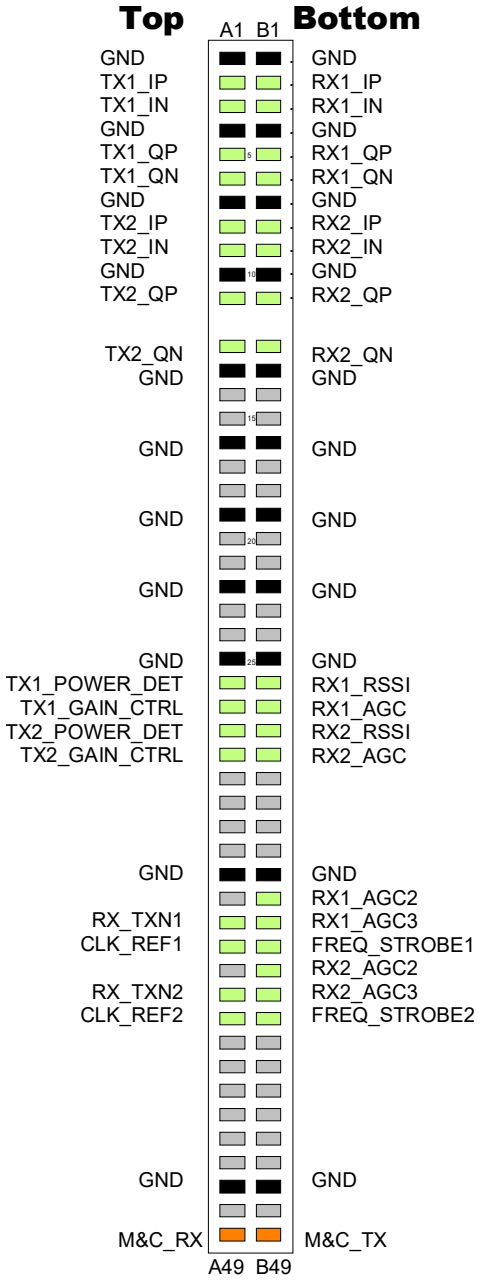
Mini USB Connector, J5

The COM-3505 is a USB device with a mini type AB connector. (G = GND)



Baseband Connector J3

98-pin Female Connector.



I/O Compatibility List

(not an exhaustive list)

I/O
COM-1700-A Low-power compact development Platform FPGA + ARM + DACs + ADCs + VGA + GbE LAN + USB2+ NAND + TCXO + RS422. Option –A.
COM-1705 Low-power compact PSK modem + Viterbi Convolutional FEC + IP router
COM-3504 Dual Analog <-> Digital Conversions [using 98-pin – 40 pin adapter COM-9109]
COM-1200 FPGA/VHDL development platform Xilinx Spartan3-1000 & Analog front-end. [using 98-pin – 40 pin adapter COM-9109]
COM-2802 Synchronized 8-channel 900 MSamples/s

Digital-to-Analog conversion
[for 2-channel transmit-only assembly]

ComBlock Ordering Information

COM-3505
Dual-Band 2.4/5 GHz 2x2 MIMO Transceiver

ECCN: 5A991.b.1

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