COM-3003
L-BAND [1500 – 1740 MHz] RECEIVER

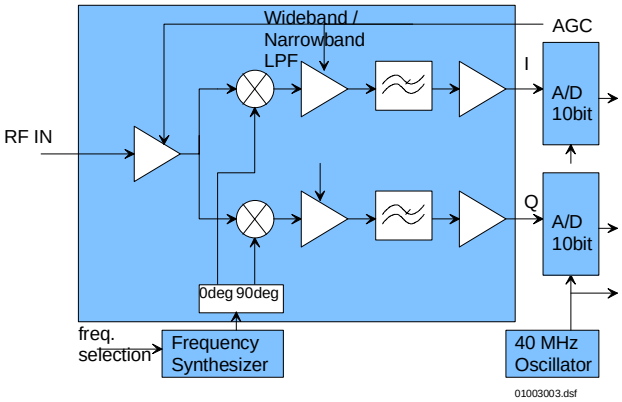
Key Features

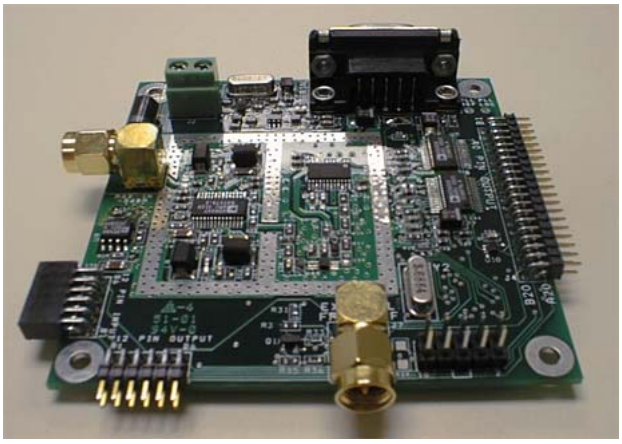
- L-band [1500-1740 MHz] receiver.
- Sensitivity: -56 dBm RF input for full scale 10-bit output samples.
- Built-in RF AGC, 70 dB dynamic range.
- Low phase-noise frequency synthesizer can be tuned over entire range by steps of 100, 31.25 or 25 KHz.
- 8 preset frequencies for fast (<2ms) local oscillator frequency tuning.
- Selectable internal / external 10 MHz frequency reference for the frequency synthesizer.
- Dual 10-bit Analog-to-Digital converters, 40 Msamples/s.
- Two baseband filtering options:
  - Narrow-band (<300 KHz)
  - Wideband applications (< 20 MHz).
- SMA connectors. Single 5V supply. Connectorized 3”x 3” module for ease of prototyping.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com3003.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Block Diagram





(shown without shield)

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Electrical Interface

Inputs / Outputs

Inputs	Definition
RF_IN	1500 - 1740 MHz. J3 SMA male connector. 50 Ohm impedance. Receiver sensitivity: -56 dBm at RF input for full scale signal at A/D converter. Maximum input (operating): -5 dBm Maximum input (no damage): +10 dBm AGC range: 70 dB.
EXT_REF_CLK	External 10 MHz frequency reference for frequency synthesis. Sinewave, clipped sinewave or squarewave. Minimum level 0.5Vpp. Maximum level: 3.3Vpp. J7 SMA male connector.
Digital Output Signals	**Definition**
DATA_I_OUT[9:0]	In-phase baseband signal. 10-bit digital samples. 40 Msamples/s. Unsigned.
DATA_Q_OUT[9:0]	Quadrature baseband signal. 10-bit digital samples. 40 Msamples/s. Unsigned.
CLK_OUT	Digital clock. 40 Msamples/s. Read the samples at the rising edge of CLK_OUT.
ADC_CLK_OUT	Same as CLK_OUT.
AGC_IN	Input signal to control the analog gain prior to A/D conversion. Can be digital (pulse-width modulated) or analog. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain. Without any subsequent module, the COM-3003's gain is set at its maximum and may thus saturate.
Control Lines	**Definition**
PLL_STROBE	Low-voltage (3.3V / 0V) TTL input control. Used to increment the modulo-N_{freq} frequency pointer (where N_{freq} is defined in Register 35) in a round-robin sequence. Rising edge triggered. Minimum pulse width: 10 µsec. Connector J6 Pin A3.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.9 – 5.25VDC. Terminal block. Power consumption is 250mA typ.

Important: digital I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

Complete assemblies can be monitored and controlled centrally over a single asynchronous serial connection or, when available through adjacent ComBlocks, LAN/TCP-IP , USB, or CardBus connection.

The module configuration is stored in non-volatile memory.

Configuration (Basic)

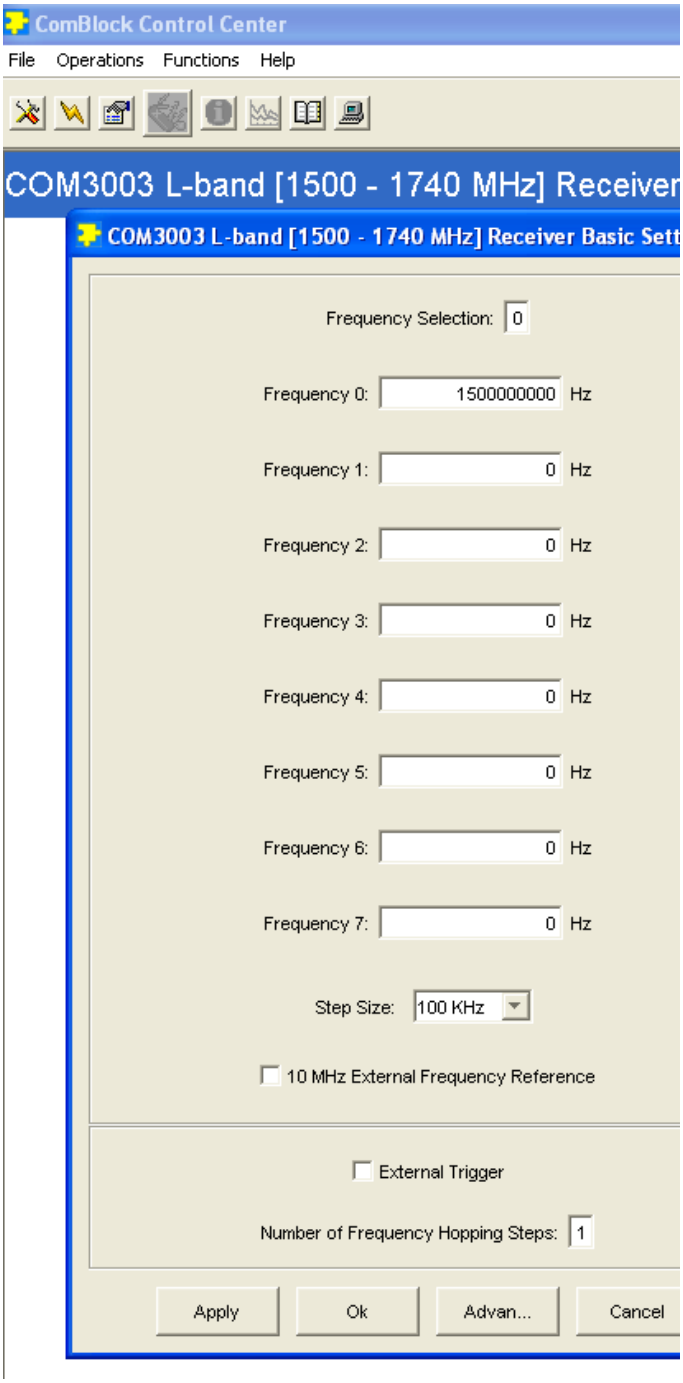
The easiest way to configure the COM-3003 is to use the ComBlock Control Center software supplied with the module(s). After detecting the ComBlock modules (2nd button from left), highlight the COM-3003 module to be configured. Then press the settings button (3rd button from the left).

Up to eight frequencies can be stored within each module at any given time. The current frequency is selected by an index in the range 0 to 7. Frequencies must be integer multiples of the RF synthesizer step size.

A basic frequency hopping scheme can be enabled by

(a) enabling the external trigger
(b) entering the number of frequency hopping steps in the round-robin arrangement.

For example, by specifying 4 steps, the receiver center frequency will follow the following index sequence: 0,1,2,3,0,1,2,3,0,1, etc., the index being incremented at the rising edge of each external PLL_STROBE pulse.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Programmers developing custom applications (using the ComBlock API instead of the supplied ComBlock control center graphical user interface) should know that frequency changes are enacted upon (re-)writing to the last register (REG35).

Parameters	Configuration
RF frequency 0	Valid range 1500 MHz – 1740 MHz, steps of 25, 31.25 or 100 KHz. Expressed in Hz. REG0: bit 7:0 (LSB) REG1: bit 15:8 REG2: bit 23:16 REG3: bit 31:24 (MSB)
External/Internal frequency reference	0 = internal 1 = external. REG4 bit 0
External controls enabled/disabled	Enable or disable the PLL_STROBE external control on the J6 connector. 0 = external control disabled 1 = external control enabled REG6: bit 1
Step size selection	Chose between 100, 31.25 or 25 KHz step size. 00 = 100 KHz step 01 = 31.25 KHz step 10 = 25 KHz step REG6 bits 4-3.
Frequency selection	Use to switch local oscillator frequency among preselected values. Range 0 through 7 REG6 bits 7-5.
RF frequency 1	Preselected frequency 1. Same format as RF frequency 0. REG7: bit 7:0 (LSB) REG8: bit 15:8 REG9: bit 23:16 REG10: bit 31:24 (MSB)
RF frequency 2	Preselected frequency 2. Same format as RF frequency 0. REG11: bit 7:0 (LSB) REG12: bit 15:8 REG13: bit 23:16 REG14: bit 31:24 (MSB)
RF frequency 3	Preselected frequency 3. Same format as RF frequency 0. REG15: bit 7:0 (LSB) REG16: bit 15:8 REG17: bit 23:16 REG18: bit 31:24 (MSB)

RF frequency 4	Preselected frequency 4. Same format as RF frequency 0. REG19: bit 7:0 (LSB) REG20: bit 15:8 REG21: bit 23:16 REG22: bit 31:24 (MSB)
RF frequency 5	Preselected frequency 5. Same format as RF frequency 0. REG23: bit 7:0 (LSB) REG24: bit 15:8 REG25: bit 23:16 REG26: bit 31:24 (MSB)
RF frequency 6	Preselected frequency 6. Same format as RF frequency 0. REG27: bit 7:0 (LSB) REG28: bit 15:8 REG29: bit 23:16 REG30: bit 31:24 (MSB)
RF frequency 7	Preselected frequency 7. Same format as RF frequency 0. REG31: bit 7:0 (LSB) REG32: bit 15:8 REG33: bit 23:16 REG34: bit 31:24 (MSB)
Number of RF frequencies N_{freq} in the scanning list	Each time a PLL_STROBE pulse is received, the frequency pointer increments modulo N_{freq}. N_{freq} is in the range 1 – 8. REG35: bit 7:0.

Note: Fine frequency tuning (down to Hz precision) is typically implemented digitally at the demodulator. See demodulators specifications (COM-1001, COM-1011/1018, COM-1027, COM-1008 etc) for details.

Monitoring

Parameters	Monitoring
Option o / Version v	Returns '3003ov' when prompted for the option and version number.

Operations

Internal vs External frequency reference for frequency synthesizer

The L-band local oscillator frequency generated by the frequency synthesizer is frequency-locked onto a 10 MHz reference clock. The source of this 10 MHz reference clock (internal versus external) is user-selected by software commands.

In order to use the external frequency reference, connect a 10 MHz sinewave, clipped sinewave or square wave to the SMA connector J7. Then select external frequency reference by software command from the ComBlock control center.

In order to use the internal frequency reference, either physically disconnect the external 10 MHz signal at SMA connector J7, or place the external input signal in high impedance mode. Then select internal frequency reference by software command from the ComBlock control center.

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	Baseband signal, I-channel, at A/D converter input. The nominal amplitude is 1Vpp when the AGC loop is closed with the following demodulator (COM-1001, COM-1011/1018, COM-1027, COM-1008 or equivalent).
TP2	Baseband signal, Q-channel, at A/D converter input. Nominal amplitude is 1Vpp when the AGC loop is closed.
PLL_LOCK	Frequency synthesizer PLL lock status. Active low: '0' when locked. Note: do not connect any long test cable to this test point as it may inject noise into the RF PLL.
PLL_REF	Reference clock (10 MHz external or 20 MHz internal)

Performance

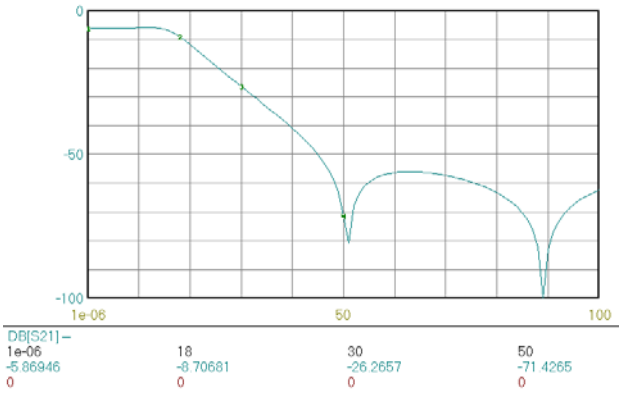
Internal Clock Reference

The internal crystal performance is as follows:

- tolerance: ± 75 ppm max @25C
- temperature stability (-10C to +60C): ± 50 ppm max
- aging: ±5ppm/year max @25C

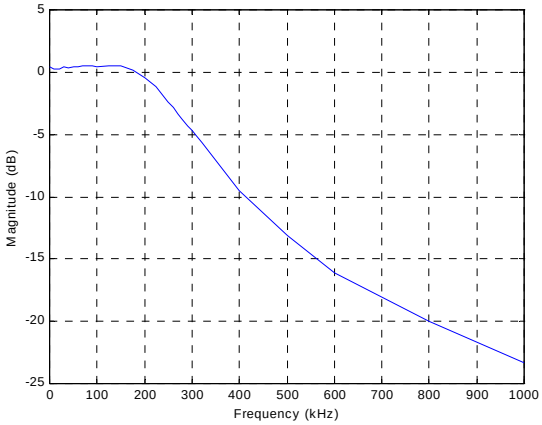
Low Pass Filter

Each A/D converter is preceeded by a 4th order elliptic low-pass filter. The 3 dB cutoff frequency for model COM-3003-B (wideband applications) is 20 MHz.



COM-3003-B baseband low-pass filter frequency response. Span 100 MHz, 10dB/div.

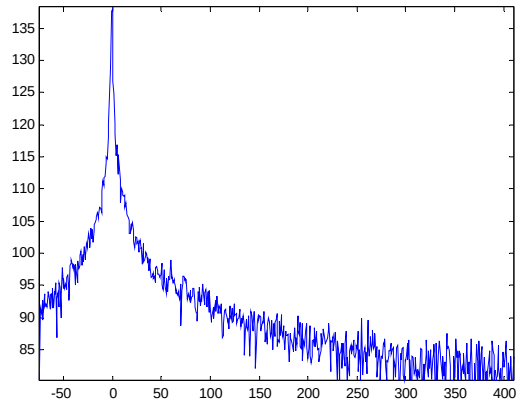
The 3 dB cutoff frequency for model COM-3003-A (narrow band applications) is 265 KHz. In-band ripple within +/- 150 KHz is less than +/- 0.1 dB.



COM-3003-A baseband low-pass filter frequency response. Span 1 MHz, 5dB/div.

Phase noise

Typical phase noise performances (100 KHz step size) are:
-50 dBc @100 Hz away from the carrier
-65 dBc @1 KHz
-75 dBc @10 KHz
-100 dBc @ 100 KHz

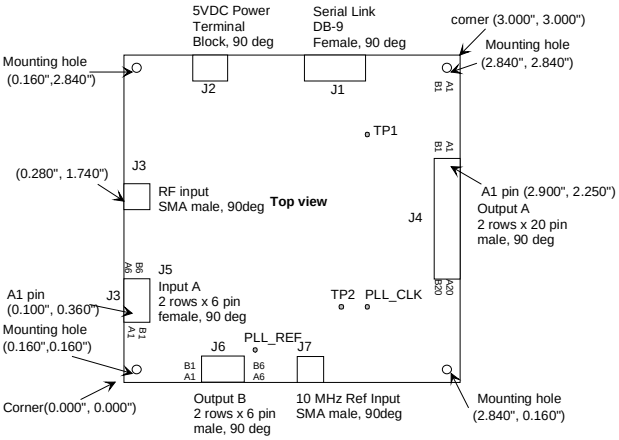


Typical close-in phase noise, 1 Hz resolution bandwidth, 400 Hz span, 5dB/div.

Spectral spurious lines are at –65 dBc or lower, with the exception of two spectral lines at +/- 100 KHz (-55 dBc).

LO frequency switching time: <2 ms

Mechanical Interface



Mounting hole diameter: 0.125"

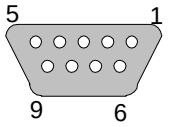
A1 pin height: 0.039"

Maximum height 0.500"

Pinout

Serial Link J1

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.

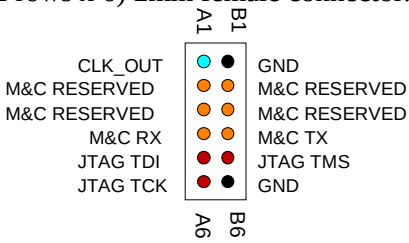


DB-9 Female

2 Transmit
3 Receive
5 Ground

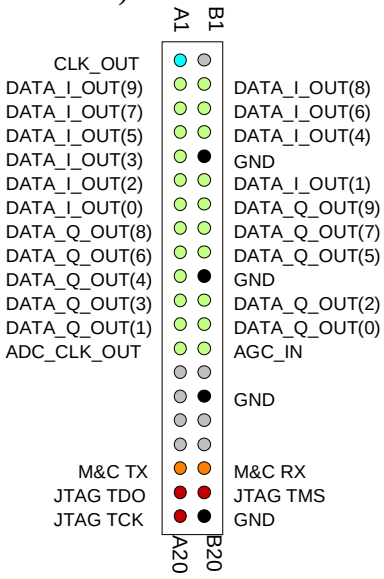
Input Connector J5

12-pin (2 rows x 6) 2mm female connector.



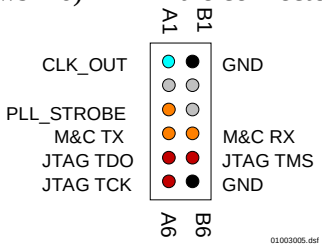
Output Connector J4

40-pin (2 rows x 20) 2mm male connector.



Connector J6

12-pin (2 rows x 6) 2mm male connector.



I/O Compatibility List

(not an exhaustive list)

Input	Output
	COM-1001 BPSK/QPSK/OQPSK demodulator
	COM-1011/1018 Direct-sequence spread-spectrum demodulator
	COM-1027 FSK/MSK/GFSK/GMSK demodulator
	COM-1008 Variable decimation
	COM-8002 High-speed data acquisition. 256MB, 1Gbit/s, 50 Msamples/s.
	COM-2001 Dual D/A converter (baseband)

Configuration Management

This specification is to be used in conjunction with Atmel microcontroller software revision A.

ComBlock Ordering Information

COM-3003-A L-band [1500-1740 MHz] Receiver. Narrow-band Applications.

COM-3003-B L-band [1500-1740 MHz] Receiver. Wideband Applications.

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