. COM-2204 CCSDS TELEMETRY MODEM

.Key Features

- Telemetry modem, including
  - BPSK/QPSK/OQPSK modulation
  - Convolutional error correction (inner code)
  - Interleaving/Deinterleaving
  - Reed-Solomon error correction (outer code)
  - network interface:
    TCP server for data input and output.
    UDP server for output.
- Flexible programmable features:
  - RF frequency 70 MHz – 6 GHz
  - Symbol rate up to 30.7 Msymbols/s
  - MODCODs
- RF: -1 dBm output @2.2GHz
  sensitivity: -85 dBm @2.2GHz
- Frequency acquisition range > ±12% of symbol rate. Tracking symbol rates over ±50ppm around nominal setting.
- Implementation loss < 0.5 dB down to Eb/No = 2dB.
- TCP server for modulator data input and demodulator output. UDP server for demodulator output.
- Built-in tools: PRBS-11 pseudo-random test sequence, BER tester, AWGN generator, internal loopback mode, carrier frequency error measurement.
-  **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Single 12V supply
- Compliant with the CCSDS standard

Subsystem	CCSDS reference
Modulator	[2] Section 5.2.1.1.as2_1 [3] Section 2.4.10
Convolutional encoder	[1] Section 3
Attached Sync Marker	[1] Section 9.1.2, 9.2, 9.3.1, 9.3.5
Randomizer	[1] Section 10
Transfer Frame Length	[1] Sections 11, 11.6
Interleaver De-Interleaver	[1] Sections 4, 4.3.5, 11.6
Reed-Solomon encoder	[1] 2.2.3, 3.2.3, 4.2.2

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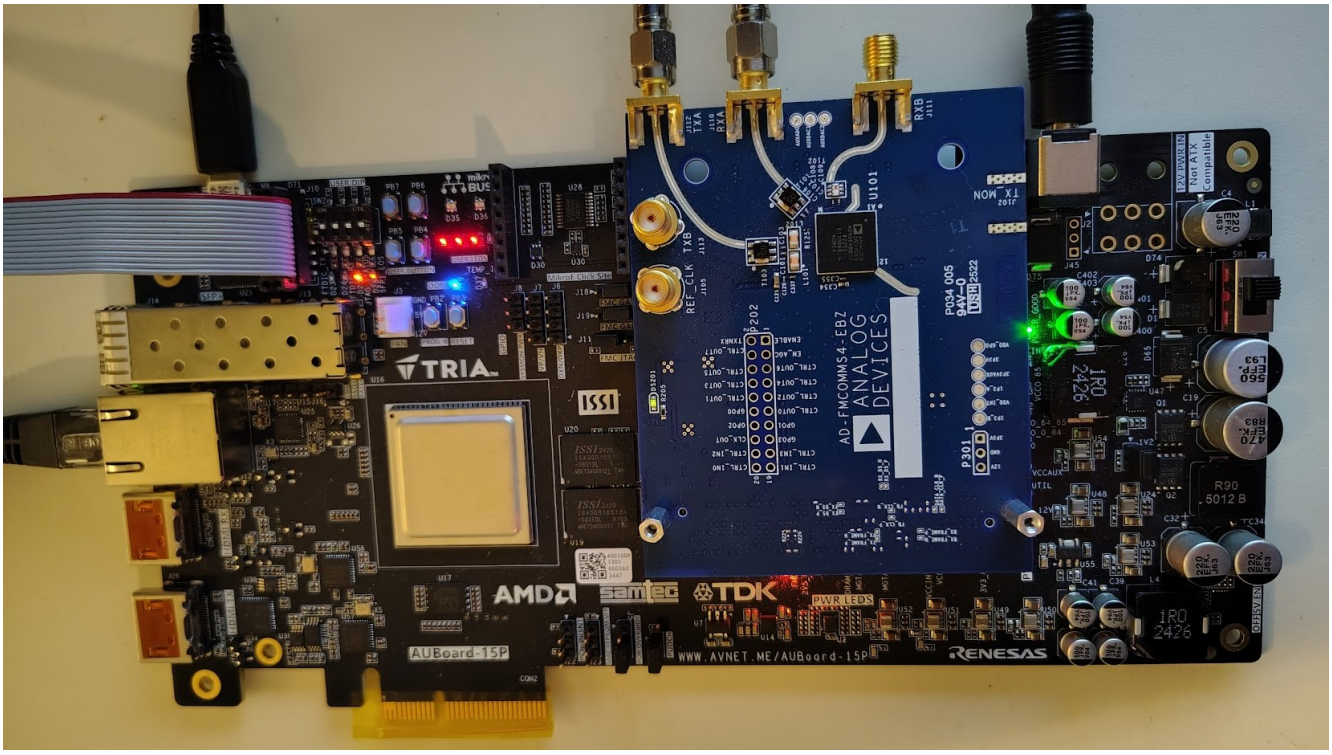

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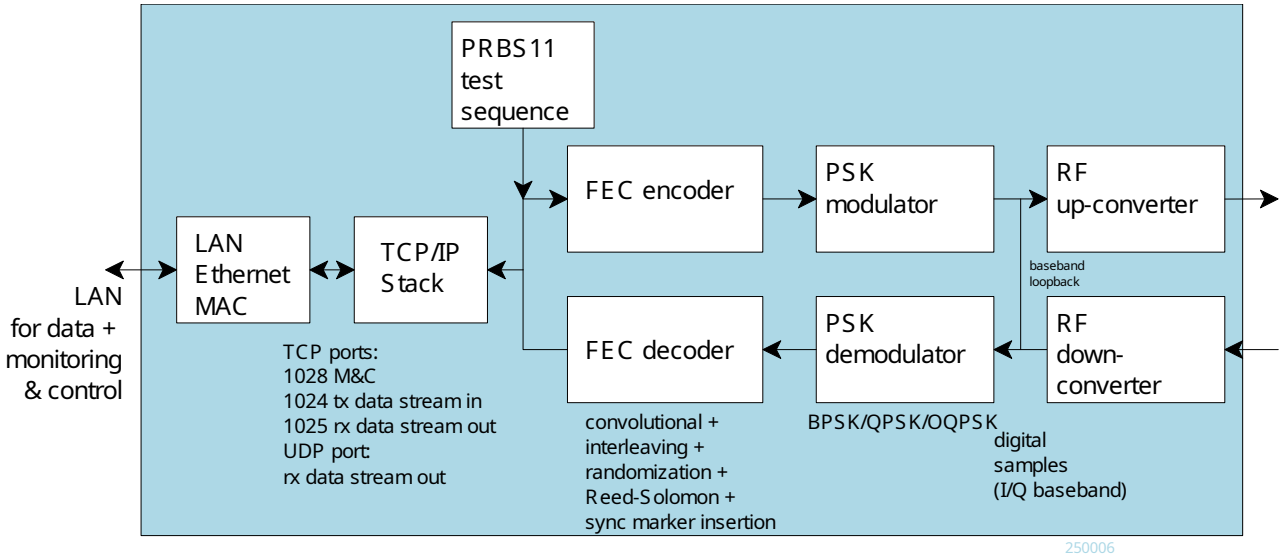
Block Diagram



Overall block diagram

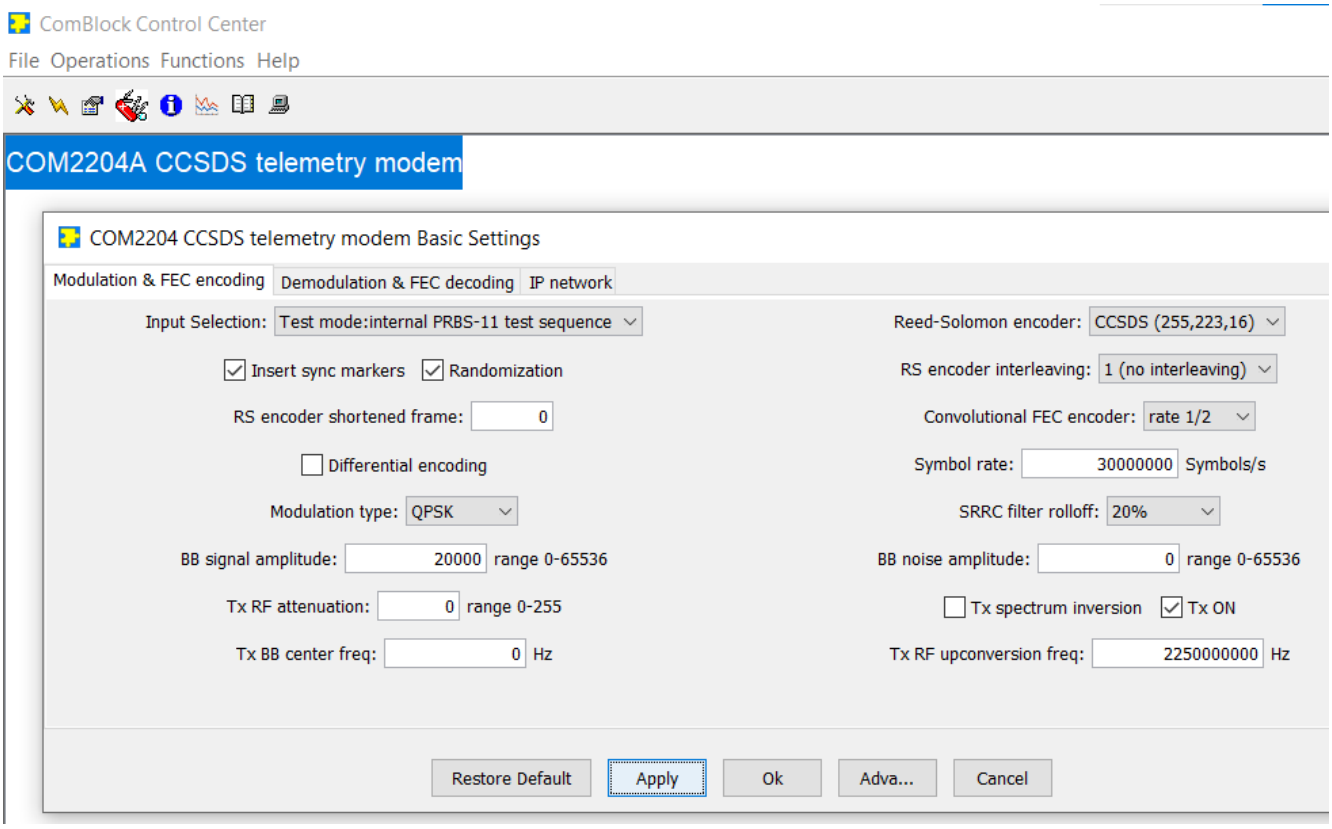
.Configuration

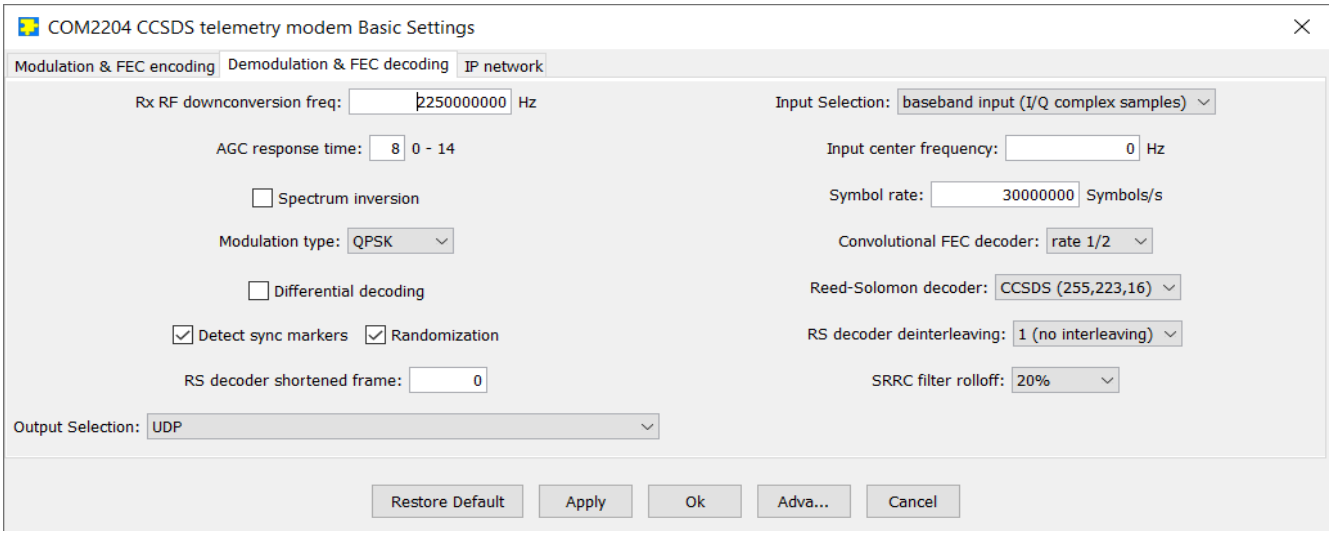
An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer over 10/100 Mbps Ethernet LAN/TCP-IP.

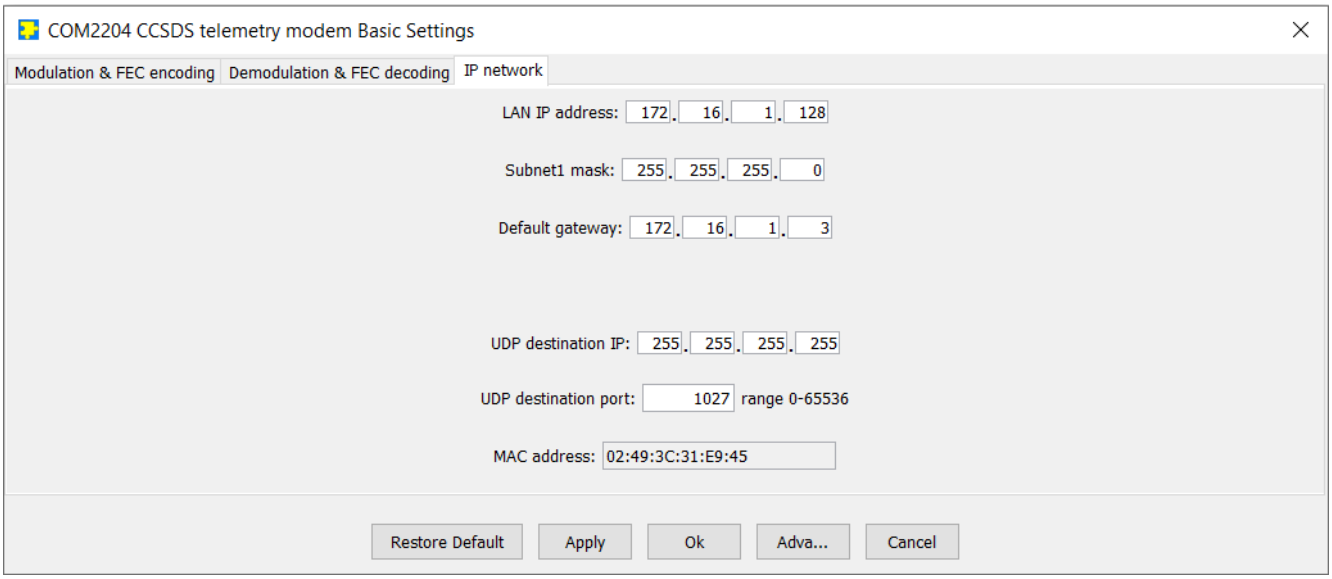
The module configuration is stored in non-volatile memory.

.Configuration (Basic)

The easiest way to configure the COM-2204 is to use the latest version of the **ComBlock Control Center** software downloadable from www.comblock.com/download.html. This GUI only runs on Windows OS. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-2204 module to be configured, next click the *Settings* button to display the *Settings* window shown below.




COM2204 CCSDS telemetry modem Basic Settings
Modulation & FEC encoding
Demodulation & FEC decoding
IP network
Rx RF downconversion freq: 2250000000 Hz
Input Selection: baseband input (I/Q complex samples)
AGC response time: 8 0 - 14
Input center frequency: 0 Hz
Spectrum inversion
Symbol rate: 30000000 Symbols/s
Modulation type: QPSK
Convolutional FEC decoder: rate 1/2
Differential decoding
Reed-Solomon decoder: CCSDS (255,223,16)
Detect sync markers
Randomization
RS decoder deinterleaving: 1 (no interleaving)
RS decoder shortened frame: 0
SRRC filter rolloff: 20%
Output Selection: UDP
Restore Default
Apply
Ok
Adva...
Cancel


COM2204 CCSDS telemetry modem Basic Settings
Modulation & FEC encoding
Demodulation & FEC decoding
IP network
LAN IP address: 172 . 16 . 1 . 128
Subnet1 mask: 255 . 255 . 255 . 0
Default gateway: 172 . 16 . 1 . 3
UDP destination IP: 255 . 255 . 255 . 255
UDP destination port: 1027 range 0-65536
MAC address: 02:49:3C:31:E9:45
Restore Default
Apply
Ok
Adva...
Cancel

.Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

.Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Several key parameters are computed on the basis of the receive sampling clock $\mathbf{f}_{clk\_rx}$ and transmit sampling clock $\mathbf{f}_{clk\_tx,}$ both 61.44 MHz. Outside the modulator/demodulator, the processing clock is 125 MHz.

Modulator	
Parameters	**Configuration**
Input selection	1 = LAN TCP port 1024 3 = internal pseudo-random test sequence 4 = zero input 7 = unmodulated test mode (carrier only) CREG0(3:0)
DAC sampling rate $\mathbf{f}_{clk\_tx}$	The DAC sampling rate is fixed at 61.44 Msamples/s
Modulator symbol rate $\mathbf{f}_{symbol\ rate\ tx}$	Modulator symbol rate is expressed as $\mathbf{f}_{symbol\_rate\_tc} * 2^{32} / \mathbf{f}_{clk\_tx}$ CREG1 (LSB) – CREG4 (MSB)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK CREG6(5:0)
Spectrum inversion	Invert Q bit. (Inverts the modulated spectrum only, not the subsequent frequency translation) 0 = off 1 = on CREG6(6)
Square root raised cosine filter rolloff	0 = 35%, 1 = 25%, 2 = 20% CREG7(2:0)
Turn output on/off	Controls the external RF modulator through the ENABLE pin. The TX_ENB control signal to the RF modulator will also be turned off when there is no input data to transmit. 0 = off 1 = on CREG7(7)
RF transmitter attenuation	0 for maximum output power CREG8
Digital Signal gain	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Please check for saturation (see status register) when changing either the symbol rate or the signal gain. CREG10 (LSB) – CREG11 (MSB)
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation (see status register) when changing this parameter. CREG12 (LSB) – CREG13 (MSB)
Baseband center frequency ($\mathbf{f}_c$)	The digital modulated signal center frequency can be shifted in frequency 32-bit signed integer (2's complement representation) expressed as $\mathbf{f}_c * 2^{32} / \mathbf{f}_{clk\_tx}$ CREG14 (LSB) – CREG17 (MSB)

RF frequency up-conversion ($\mathbf{f_{tx\_lo}}$)	The tx RF frequency translation is implemented by a VCO (frequency range 6-12 GHz) followed by a power of two frequency divider. The VCO frequency is expressed as ($\mathbf{f_{tx\_vco}}$ / 80 MHz) * 2^{32} CREG18 (LSB) – CREG21 (MSB) Example: x64 for 8 GHz VCO Frequency divider is expressed in power of 2: CREG9(3:0) The final output center frequency is the sum of the RF frequency translation and the baseband center frequency.

Convolutional FEC encoder	
Parameters	**Configuration**
Convolutional FEC encoding	'1' enabled, '0' bypassed CREG22(7)
Convolutional FEC encoding constraint length K and rate R	1011 = (K = 7, R=1/2, CCSDS) 1100 = (K = 7, R=2/3, CCSDS/DVB) 1101 = (K = 7, R=3/4, CCSDS/DVB) 1110 = (K = 7, R=5/6, CCSDS/DVB) 1111 = (K = 7, R=7/8, CCSDS/DVB) CREG22(3:0)
Differential convolutional FEC encoding:	0 = disabled 1 = enabled CREG22(4)

Reed Solomon FEC encoder	
Parameters	**Configuration**
RS encoding	'1' enabled, '0' bypassed (encompasses frame marker insertion, randomization, interleaving, dual-basis, RS encoding proper) CREG23(7)
RS code	Standard selection 5 = CCSDS (255,223,16) 6 = CCSDS (255,239,8) CREG23(3:0)
RS encoder controls	bit 0: attached sync marker 0x1ACFFC1D at the RS encoder output (1) or ignore (0). Enable when using convolutional code + RS encoding. bit 2: bit randomization on (1) /off(0) Other bits set to zero. CREG24(7:0)
RS interleaving	number of interleaved blocks CCSDS valid values 1 (no interleaving),2,3,4,5,8 CREG25(3:0)
Shortened frame	Uncoded blocks can be shortened by RS_SHORT Bytes. RS_SHORT Bytes (zeroes) are inserted before the payload data prior to encoding. They are not sent over the transmission channel. In effect, the shortened payload size in a frame is RS_I*(RS_K - RS_SHORT). This setting must be consistent between transmitter and receiver. CREG26

Demodulator	
Parameter	**Configuration**
RF frequency down-conversion ($\mathbf{f_{rx\_lo}}$)	The rx RF frequency translation is implemented by a VCO (frequency range 6-12 GHz) followed by a power of two frequency divider. The VCO frequency is expressed as ($\mathbf{f_{tx\_vco}}$ / 80 MHz) * 2^{32} CREG31 (LSB) – CREG34 (MSB) Example: x64 for 8 GHz VCO Frequency divider is expressed in power of 2: CREG30(3:0)

	Example: 1 for divide by 4 The final output center frequency is the sum of the RF frequency translation and the baseband center frequency.
ADC sampling rate f_{clk_rx}	The ADC sampling rate is fixed at 61.44 Msamples/s
Demod input selection	0 = baseband input (I/Q complex samples) 1 = IF input (I as real input, Q is ignored) 7 = internal loopback CREG35(6:4)
External AGC response time	Users can to optimize AGC response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and modulation symbol rate). The AGC_DAC gain control signal is updated as follows 0 = every symbol, 1 = every 2 input symbols, 2 = every 4 input symbols, 3 = every 8 input symbols, etc…. 10 = every 1000 input symbols. Valid range 0 to 14. CREG36(4:0)
Nominal input center frequency (f_c)	The nominal center frequency is a fixed frequency offset applied to the input samples. It is used for fine frequency corrections, for example to correct clock drifts. 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk\_rx}$ CREG37 (LSB) – CREG40 (MSB)
Nominal symbol rate f_{symbol_rate}	Nominal symbol rate, defined as $f_{symbol\_rate} * 2^{32} / f_{clk\_rx}$ CREG41 (LSB) – CREG44 (MSB)
CIC_R decimation	CIC_R largest integer < 4*input sampling rate/symbol rate. 0 is illegal. Min value 1. CREG45(LSB) - CREG46(MSB)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK CREG47(5:0)
Spectrum inversion	Invert Q bit 0 = off 1 = on CREG47(6)

Square root raised cosine filter rolloff	0 = 35% 1 = 25% 2 = 20% CREG48(2:0)
AGC	0 = AGC enabled 1 = fixed receiver gain as per CREG29 CREG5(0)
Fixed rx gain	Range 0 – x4C (76d) Enabled when CREG5(0) = '1' CREG29

Convolutional FEC decoder	
Parameters	**Configuration**
Convolutional (Viterbi) FEC decoding	'1' enabled, '0' bypassed CREG52(7)
Viterbi decoding constraint length K and rate R	1011 = (K = 7, R=1/2, CCSDS) 1100 = (K = 7, R=2/3, CCSDS/DVB) 1101 = (K = 7, R=3/4, CCSDS/DVB) 1110 = (K = 7, R=5/6, CCSDS/DVB) 1111 = (K = 7, R=7/8, CCSDS/DVB) CREG52(3:0)
Viterbi decoding: Differential Decoding	0 = disabled 1 = enabled CREG52(4)

Reed Solomon FEC decoder	
Parameters	**Configuration**
RS decoding	'1' enabled, '0' bypassed (encompasses frame synchronization, de-randomization, deinterleaving, dual-basis, RS decoding proper) CREG53(7)
RS code	Standard selection 5 = CCSDS (255,223,16) 6 = CCSDS (255,239,8) CREG53(3:0)
RS decoder controls	bit 0: detect and remove the attached sync marker 0x1ACFFC1D at the RS decoder input (1) or ignore (0). Enable when using convolutional code + RS decoding. bit 2: bit de-randomization on (1) /off(0) Other bits set to zero. CREG54
RS interleaving	number of interleaved blocks CCSDS valid values 1 (no interleaving),2,3,4,5,8 CREG55(3:0)
Shortened frame	Uncoded blocks can be shortened by RS_SHORT Bytes. RS_SHORT Bytes (zeroes) are inserted before the payload data prior to encoding. They are not sent over the transmission channel. In effect, the shortened payload size in a frame is RS_I*(RS_K - RS_SHORT). This setting must be consistent between transmitter and receiver. CREG56

Receiver output path	
Output selection	1 = LAN TCP port 1025 2 = UDP 3 = serial data bit + bit clock, left connector. J4 left connector CREG55(6:4)

Network Interface	
Parameters	**Configuration**
Static IP address	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 CREG61(MSB) - CREG64 (LSB)
Subnet mask	CREG65 (MSB) – CREG68(LSB)
Gateway IP address	CREG69 (MSB) – CREG72(LSB)
Destination IP address	4-byte IPv4 address Destination IP address for UDP frames with decoded data. CREG73 (MSB) – CREG76(LSB)
Destination ports	CREG77(LSB) – CREG78(MSB)

AD9364 RF module advanced controls	
Parameters	**Configuration**
Write data byte	CREG49
Write address	CREG50(7): 1 for write, 0 for read CREG50(1:0): address MSbs CREG51: address Lsbs
Read register address	CREG58: MSB CREG59: LSB
CTRL_OUT test points definition	See AD9364 reference manual Table 46 CREG60

(Re-)Writing to the last control register CREG78 is recommended after a configuration change to enact the change.

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.Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-9 SREG0(3:0): xF clocks PLL locked SREG0(7:6): DIP switch position SREG1: x22 LAN PHY ID
FPGA Configuration options enabled in this active firmware	'1' when instantiated '0' when disabled/bypassed SREG2(0): transmitter SREG2(1): RS encoder SREG2(2): convolutional enc. SREG2(3): AWGN generation SREG2(4): receiver SREG2(5): RS decoder SREG2(6): Viterbi decoder
Temperature	Measured by the analog/RF board SREG3
AD9364 register output	SREG4
Tx: Modulator saturation	Saturation in the output signal path. 0 when no saturation. These flags are reset upon reading status register SREG0. SREG10(0)
Tx: Measured modulated signal power	SREG11(LSB) – SREG13(MSB)
Tx: Measured AWGN power	Approximation: noise power is uniform over a range of +/- 2*symbol rate SREG14(LSB) – SREG16(MSB)
FEC decoder input BER measurement (convolutional code)	The burst-mode FEC decoder computes the input BER prior to decoding. Meassured in a frame. This method works with any bit sequence. SREG17 (LSB) - SREG19 (MSB)
RS decoder input BER measurement	BER measured in the periodic sync words. Measured over 1024 bits SREG30 (LSB) - SREG31 (MSB)
Viterbi decoder lock status	(Only when convolutional FEC) 0 = unlocked 1 = locked SREG20(0)
SOF locked	Detected periodic start of frame synchronization sequences (only when RS code is enabled) SREG20(1) 0 = not synchronized 1 = synchronized
BER tester synchronized	SREG20(2): 1 when the BERT is synchronized with the received PRBS-11 test sequence.
Bit error rate	Monitors the BER (number of bit errors over 80,000 received bits) when the modulator is sending a PRBS-11 test sequence. BER measurement is only valid when the BERT is synchronized (see above) Note that x013880 indicates that all bits are inverted. This can occur due when the PSK demod phase ambiguity is not resolved by the subsequent FEC decoder. SREG21 (LSB) – SREG23 (MSB)
AGC	Front-end AGC gain settings. 12-bit unsigned. Inverted (0 for maximum gain) SREG24 (LSB) SREG25(3:0) (MSB)
Carrier frequency offset2	Residual frequency offset with respect to the nominal carrier frequency. 32-bit signed integer expressed as fcerror * * 2^{30} / f_{symbol_rate} SREG26 (LSB) – SREG29 (MSB)

Inverse SNR	A measure of noise over signal power. 0 represents a noiseless signal. Valid only when demodulator is locked. SREG32
Received baseband signal power	SREG33(LSB) - SREG35(MSB)
Demod status	Bit 0: carrier lock Bit 1: rx signal presence SREG36
RSSI	RF receive signal strength indicator SREG37

TCP-IP Connection Monitoring	
Parameters	**Monitoring**
MAC address	Unique 48-bit hardware address (802.3). In the form SREG40:SREG41:SREG42: …:SREG45
Ethernet MAC RX frames counter	SREG46 (LSB) SREG47 (MSB)
Ethernet MAC bad RX CRC counter	SREG48 (LSB) – SREG49(MSB)
TCP connection	SREG50 bit0: server port 1028 (monitoring and control) bit1: server port 1024 (transmit data stream) bit2: server port 1025 (receive data stream)

Multi-byte status variables are latched upon (re-)reading SREG0.

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.ComScope Monitoring

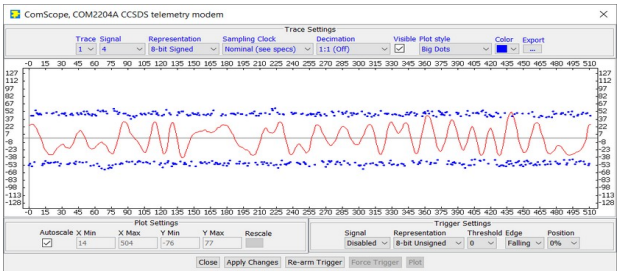
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. Click on the button to start, then select the signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: I-channel input, directly from ADC	8-bit signed	ADC clock f_{clk_rx}	512
2: front-end AGC	8-bit unsigned	2 samples/ symbol	512
3: symbol timing loop: accumulated timing correction	8-bit signed	1 sample / symbol	512
4: Demodulated I-channel	8-bit signed	1 sample / symbol	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Q-channel input, directly from ADC	8-bit signed	ADC clock f_{clk_rx}	512
2: I signal after elastic buffer, interpolation and resampling at 4 samples/symbol	8-bit signed	4 samples/ symbol	512
3: carrier tracking loop: accumulated phase correction	8-bit signed	4 samples/ symbol	512
4: Inverse SNR	8-bit signed	1 sample / symbol	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1. tx I data	8-bit signed	DAC clock f_{clk_tx}	512
2. tx Q data	8-bit signed	DAC clock f_{clk_tx}	512

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk_rx} demod clock as real-time sampling clock.

In particular, selecting the f_{clk_rx} demod clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing demodulated I symbols (blue), baseband input waveform (red)

.Digital Test Points

N/A

.Options

N/A

.LEDs

- Blue 'DONE' LED, D19. When lit, it indicates that the FPGA is properly configured.
- D31 LAN TCP connection for M&C port 1028
- D32 LAN TCP connection for tx data port 1024
- D33 SOF lock
- D34 BER tester synchronized

.Operation

.Transmitter Inputs

The user sends payload data to the transmitter over a 10/100 Mbps Ethernet LAN. The user (TCP client) opens a TCP connection to the COM-2204 (TCP server) at port 1024. The COM-2204 static IP address is configurable via the GUI.

Input flow control considerations:
The transmitter sets the pace of transmission by configuring the modulation symbol rate. The external data source does not control the tx data rate. The external data source must follow the flow control signal to prevent a buffer underflow or overflow condition.

When using TCP-IP to send telemetry data, the TCP protocol automatically regulates the flow of data. Thus, the TCP client must send data as fast as allowed by the TCP connection, so as to avoid buffer underflow condition.

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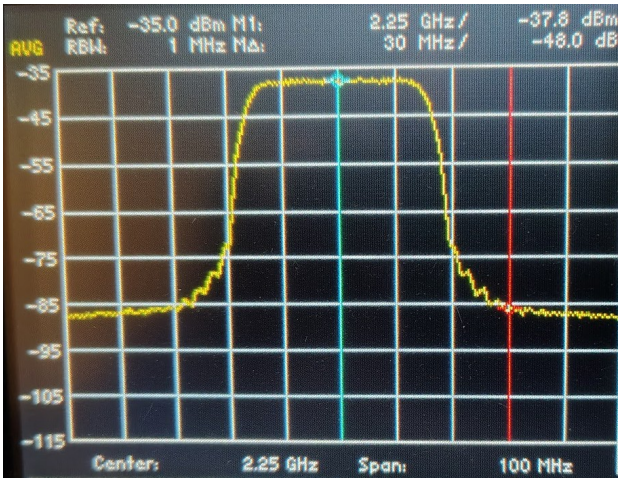
.Transmitter Outputs



Output RF spectrum example
2.25 GHz, 30 Msymbols/s, SRRC filter rolloff 20%

For many applications, an external RF LPF/BPF is recommended to filter out the center frequency harmonics.

RF transmit level:
350 MHz
+4 dBm (modulated)
+7.1 dBm (carrier-only)

2.2 GHz
-1 dBm (modulated)
+3.4 dBm (carrier-only)

3 GHz
-1.5dBm (modulated)
+2.2 dBm(carrier-only)

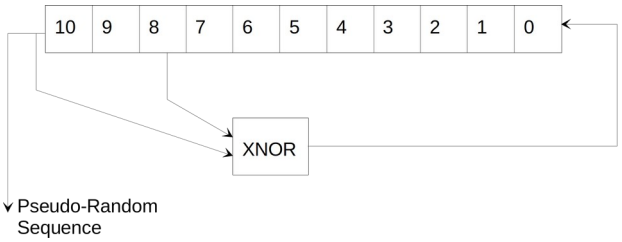
Programmable attenuation:
64.5 dB at 340 MHz
62.5 dB at 2.2GHz
62.5 dB at 3 GHz

Phase noise @ 1KHz offset from the LO frequency
350 MHz: -92 dBc/Hz
2.2 GHz: -90 dBc/Hz
3 GHz: -90 dBc/Hz

.PRBS-11 Pseudo-Random Bit Stream

In order to perform bit error rate measurements at the receiver, a pseudo-random binary sequence can be inserted at the transmitter input (thus replacing any user data). BER measurement is made by

counting actual errors in the received bit stream. The received bit stream is compared with a locally generated replica of the reference PRBS-11 sequence.
The reference sequence is a periodic 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:



The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100 1100111000 0000010011 1111010001 1110110100 1101001100 0011000001

Receiver Outputs

The receiver supports two output types:

1. A TCP server listening/waiting for a client connection over Gigabit Ethernet (10/100/1000 Mbps) at port 1025. Once the remote client is connected, the receiver forwards the demodulated data stream to the TCP client.

2. A UDP server sending frames to the user-specified destination IP address. UDP frames are sent when upon receiving 1024 bytes of data or after 0.5 second, whichever event comes first. The UDP frame format is as follows:
16-bit frame size
16-bit frame counter
12 null bytes
up to 1024 data bytes.

RF input operating range:
-85 dBm to 0 dBm

Note: it is important to specify a valid destination address when using the UDP output. If the destination IP is not an active node on the network, the UDP source may overwhelm the LAN and blocks user communication. To recover, see the recovery section.

.Phase Ambiguity Resolution

The QPSK/OQPSK demodulator exhibits an inherent 0/90/180/270 phase ambiguity. The ambiguity is automatically resolved by detecting persistent high BER at the Viterbi decoder and/or inverted sync marker at the Reed-Solomon decoder input.

Note that, when the Reed-Solomon decoder is bypassed, the receiver is not capable of resolving simple inversions. In this case the BER detector will report either 0 errors or 80000 bit errors in a 80000 bit measurement window.

.Bit Timing Tracking

A first order loop is capable of acquiring and tracking bit timing differences between the transmitter and the receiver of at least ± 50 ppm.

.AGC

To maintain linearity throughout the receive path, several AGC loops control the signal level. While

most AGC loops are internal, an additional AGC loop is dedicated to controlling an RF front-end.

.Specifications

[1] CCSDS "TM Synchronization and Channel Coding", CCSDS 131.0-B-5, September 2023

[2] CCSDS "Flexible Advanced Modulation and Coding Scheme for High-Rate Telemetry Applications", CCSDS 131.2-B-2, February 2023

[3] CCSDS "Radio Frequency and Modulation Systems, Part 1", CCSDS 401.0-B-32, October 2021

[4] Analog Devices AD9364 reference manual ug-673

[5] Analog Devices AD9364 register map reference manual ug-672

.Acronyms

Acronym	Definition
ADC	Analog to Digital Converter
ASI	Asynchronous Serial Interface
AWGN	Additive White Gaussian Noise
BRAM	Dual-port Block RAM
BER	Bit Error Rate
CCSDS	Consultative Committee for Space Data Systems
DAC	Digital to Analog Converter
DVB	Digital Video Broadcast
FPGA	Field Programmable Gate Arrays
LO	Local Oscillator
LSb	Least Significant bit
LSB	Least Significant Byte
M&C	Monitoring and Control
MODCOD	Modulation and Coding configuration
MSb	Most Significant bit
MSB	Most Significant Byte
N/A	Not Applicable
OS	Operating System
PRBS-11	Pseudo-Random Binary Sequence, 2047-bit period
RF	Radio Frequency
SOF	Start Of Frame
SoC	System on Chip
TC	Telecommand
TM	Telemetry
UART	Universal Asynchronous Receiver/Transmitter

.Load Software Updates

From time to time, ComBlock software updates are released on the comblock.com/download folder.

The software configuration files are named with the .bit or .bin extension.

To load a new software version from the AMD/Vivado tool, connect a USB cable from the PC to the JTAG/USB port on the digital board.

Note: the FTDI chip driver must be installed on the host PC to use the JTAG connection.

From Vivado, open the hardware manager and program the new .bit/.bin file directly into the FPGA or indirectly into the QSPI flash memory.

The option and revision for the software currently running within the FPGA are listed at the bottom of the advanced settings window.

.Recovery

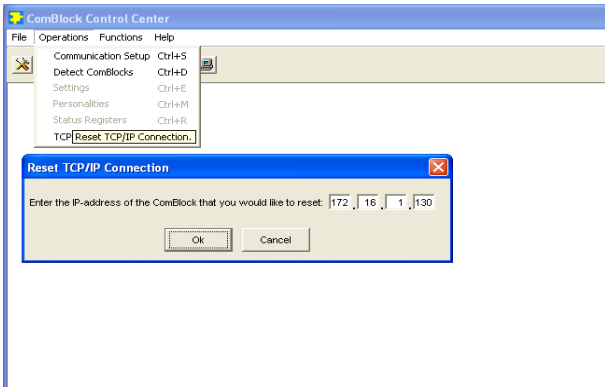
This module is protected against corruption by an invalid invalid configuration. To recover communication from such occurrence, set the DIP switch bit 0 (left most) to ‘1’ and power up for at least 25 seconds. Then return the DIP bit 0 to ‘0’ without switching off the power. This restores the default IP address to 172.16.1.128. Correct control register values can then be redefined using the ComBlock Control Center.

.UDP Reset

Port 1029 is open as a UDP receive-only port. This port serves a single purpose: being able to reset the modem (and therefore the TCP-IP connection) gracefully. This feature is intended to remedy a common practical problem: it is a common occurrence for one side of a TCP-IP connection to end abnormally without the other side knowing that the connection is broken (for example when a client ‘crashes’). In this case, new connections cannot be established without first closing the previous ones. The problem is particularly acute when the COM-2204 is at a remote location.

The command “@001RST<CR><LF>” sent as a UDP packet to this port will reset all TCP-IP connections within the COM-2204.

TCP-IP connections can also be cleared remotely from the ComBlock Control Center as illustrated below:



.VHDL code

The VHDL source code is available separately for licensing (see https://comblock.com/com1804soft.html). This IP core is written in VHDL. It does not use any IP core or third-party software. It occupies the following FPGA resources:

Resource	Utilization	Available	Utilization %
LUT	29543	77760	37.99
LUTRAM	155	40320	0.38
FF	26757	155520	17.20
BRAM	46.50	144	32.29
DSP	116	576	20.14
IO	78	228	34.21
MMCM	2	3	66.67

Xilinx Artix Ultrascale 15P target

.Interfaces

Interfaces	Definition
10/100 Mbps LAN	RJ-45 connector Shared among - transmit data stream (TCP port 1024) - receive data stream (TCP port 1025 or UDP) - monitoring and control (TCP port 1028)
RF output	SMA female, edge connector "TXA"
RF input	SMA female, edge connector "RXA"
Power supply	12VDC 2.5mm DC barrel jack (included with the external universal AC power supply)

.Hardware

The COM-2204 hardware is an assembly of two third-party boards:

- Analog Devices AD-FMCOMMS4-EBZ RF board (AD9364) https://www.analog.com/en/resources/evaluation-hardware-and-software/evaluation-boards-kits/eval-ad-fmcomms4-ebz.html

- Avnet/Tria AU board 15P FPGA development kit (AMD XCAU15P Artix ultrascale+ FPGA) https://www.avnet.com/americas/products/avnet-boards/avnet-board-families/auboard-15p-fpga-development-kit/

.USB

The USB port is equipped with micro-B USB connector. It is used primarily as a JTAG path to (re-) program the QSPI flash memory with the FPGA configuration (.bit / .bin) file.

Configuration Management

This specification is to be used in conjunction with VHDL software revision 1 and ComBlock control center revision 4.04p and above.

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-2204, then go to the settings. The option and version are listed at the bottom of the configuration panel.

For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com2204.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

.ComBlock Ordering Information

COM-2204 CCSDS telemetry modem

ECCN: EAR99

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