COM-1905 L/S-band continuous-mode PSK transceiver

Key Features

- L/S-band modem to send and receive continuous streams over wireless, satellite or cable. (for burst-mode see COM-1902)
- BPSK/QPSK/OQPSK modulation. Programmable symbol rate, up to 40 MSymbols/s
- Nominal frequency of operation: 950 – 2175 MHz for direct connection to external LNB or BUC. Customization to other frequency bands is possible.
- Convolutional or Turbo code error correction.
- Built-in IP router with gigabit Ethernet LAN port
- Supply voltage: 18 – 36VDC with reverse voltage and surge protection. (5.6V min when not supplying external LNB)
- Frequency reference: internal TCXO or input for an external, higher-stability 10 MHz frequency reference.
- Built-in tools: PRBS-11 pseudo-random test sequence, BER tester, AWGN generator, internal loopback mode.
- Monitoring:
  - Carrier frequency error
  - SNR
  - BER
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.

For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com1905.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

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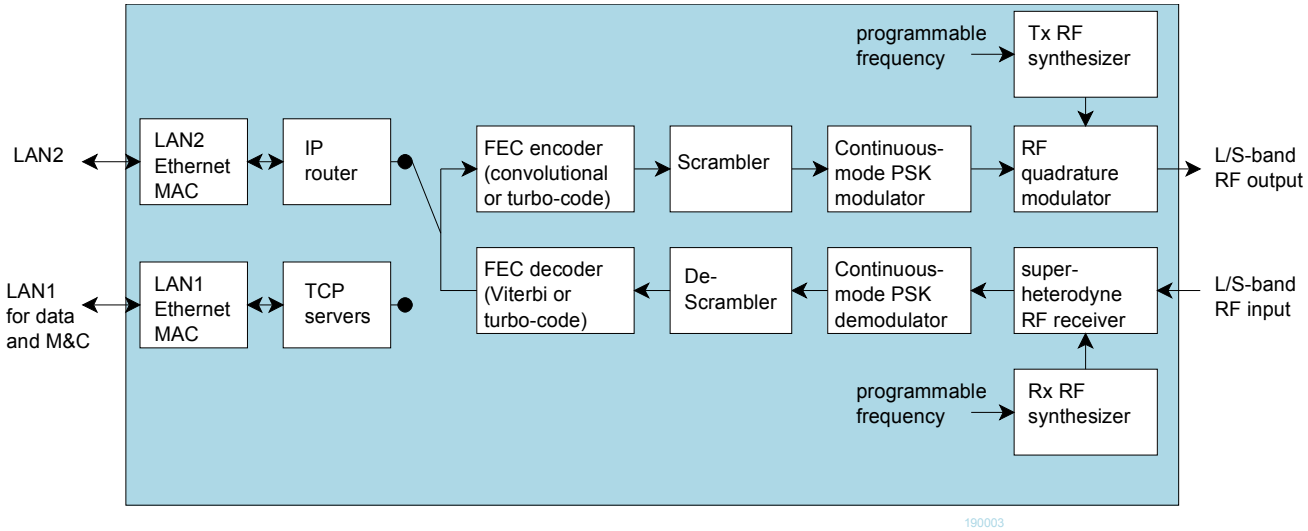
Functional Block Diagram

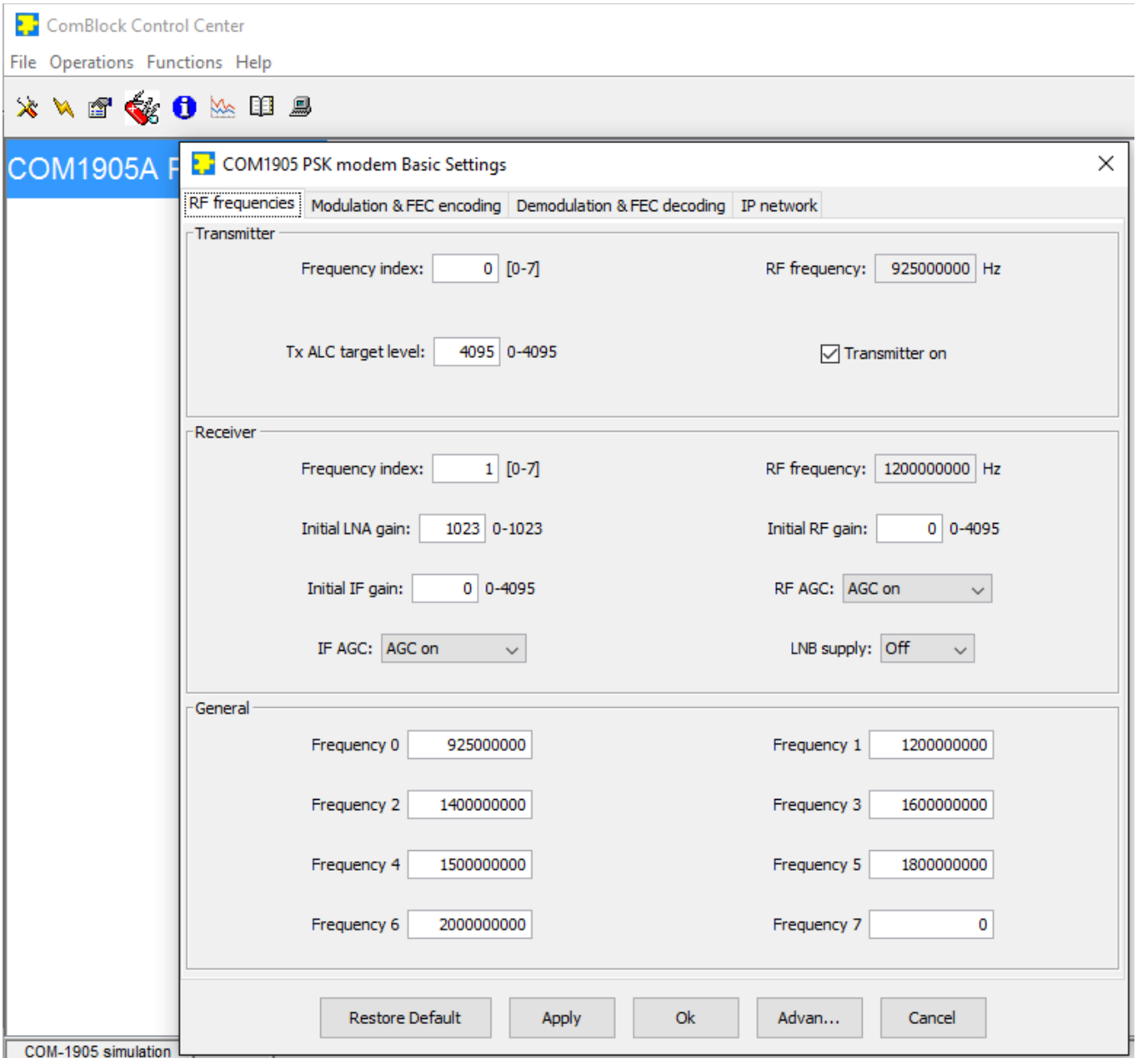


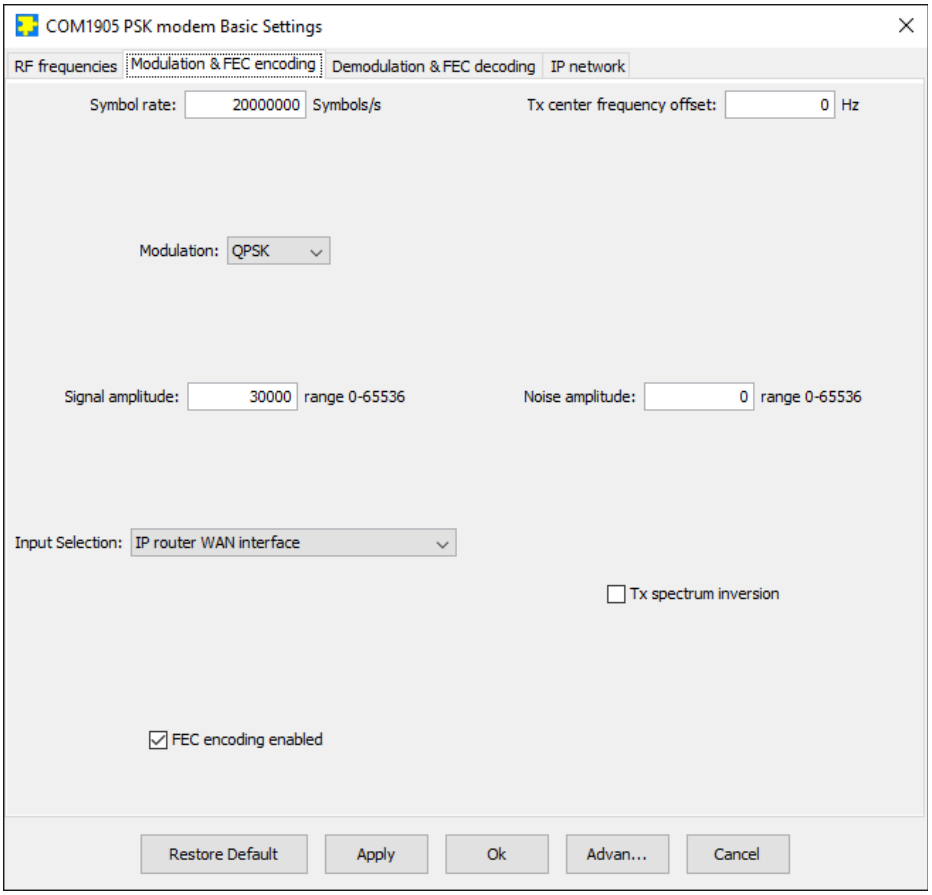
Configuration (Basic)

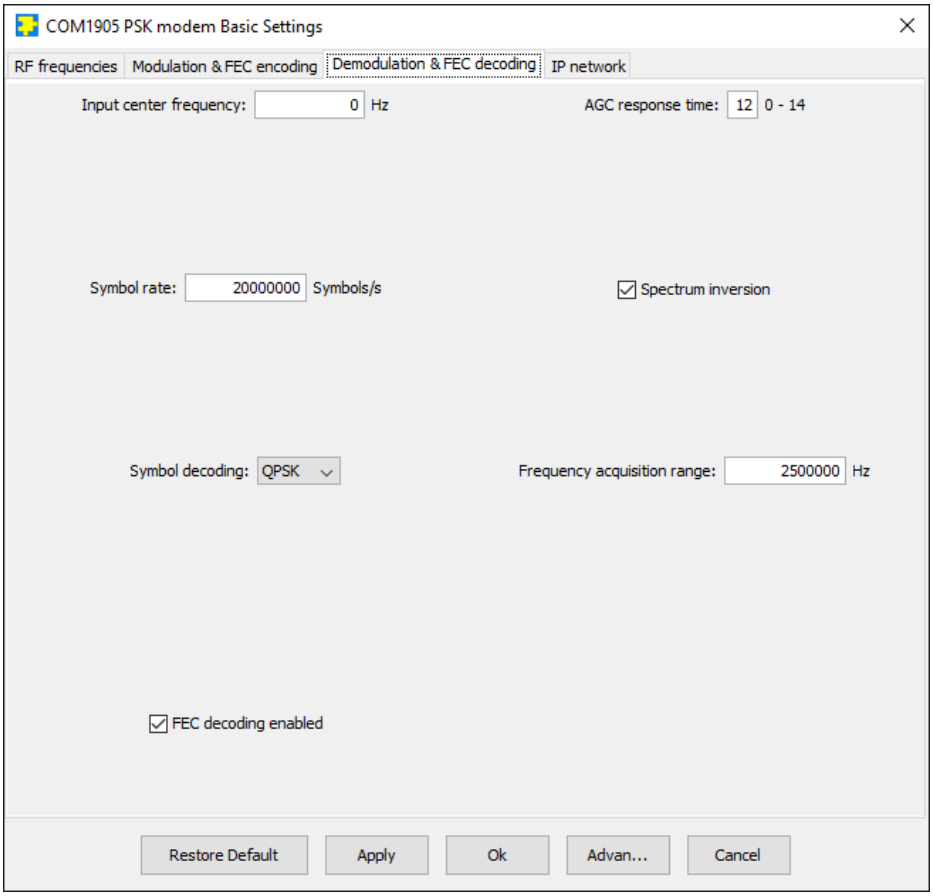
The easiest way to configure the COM-1905 is to use the **ComBlock Control Center** software supplied with the module on CD. Please follow the few simple steps described in the user manual "ccchelp.pdf" document to install the ComBlock Control Center software "ComBlock_Control_Center_windows_rev.exe"

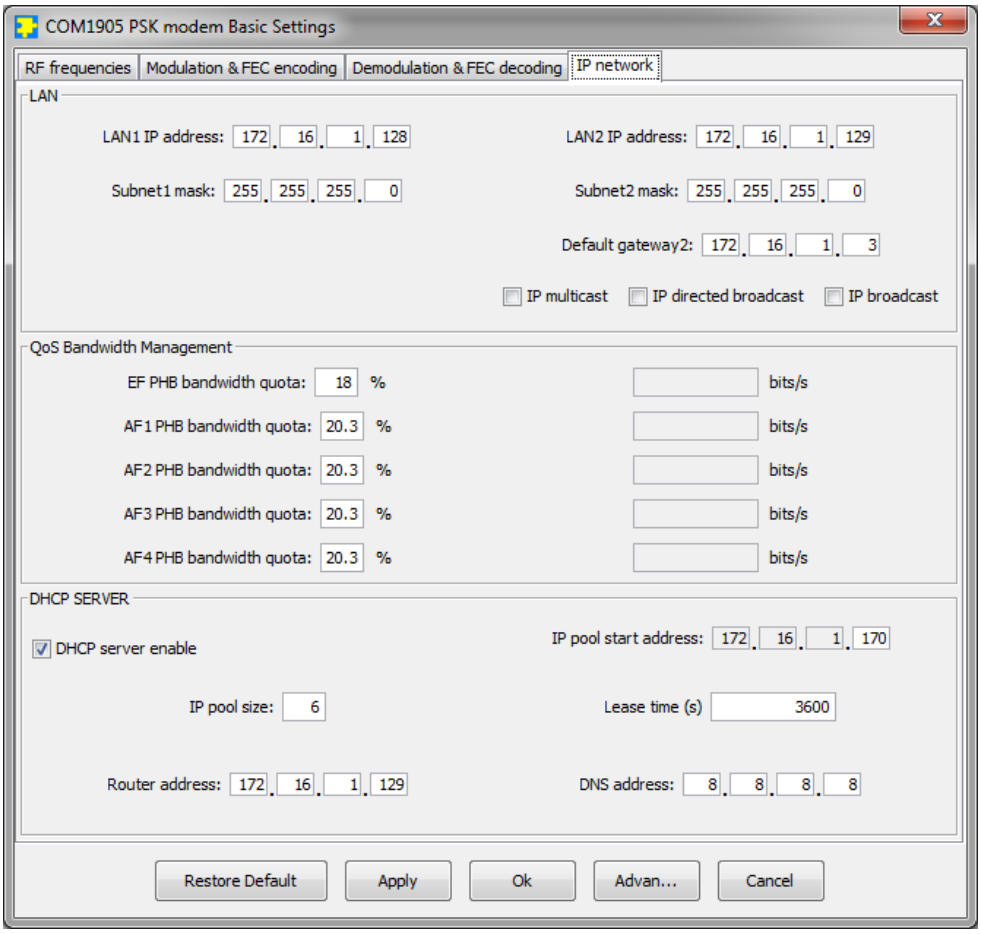
Connect the LAN cable between PC and transceiver RJ45 connector labeled "M&C LAN". Turn the transceiver power supply on and wait approximately 5-10 seconds. In the **ComBlock Control Center** window, click on the left-most button and select LAN as primary communication media. The default IP address is 172.16.1.128.

In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1905 module to be configured, next click the *Settings* button to display the *Settings* window shown below.




COM1905 PSK modem Basic Settings
RF frequencies
Modulation & FEC encoding
Demodulation & FEC decoding
IP network
Symbol rate: 20000000 Symbols/s
Tx center frequency offset: 0 Hz
Modulation: QPSK
Signal amplitude: 30000 range 0-65536
Noise amplitude: 0 range 0-65536
Input Selection: IP router WAN interface
Tx spectrum inversion
FEC encoding enabled
Restore Default
Apply
Ok
Advan...
Cancel


COM1905 PSK modem Basic Settings
RF frequencies
Modulation & FEC encoding
Demodulation & FEC decoding
IP network
Input center frequency: 0 Hz
AGC response time: 12 0 - 14
Symbol rate: 20000000 Symbols/s
Spectrum inversion
Symbol decoding: QPSK
Frequency acquisition range: 2500000 Hz
FEC decoding enabled
Restore Default
Apply
Ok
Advan...
Cancel



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center "Advanced" configuration or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). The stored configuration is automatically loaded up at power up. All control registers are read/write.

Note: several multi-byte fields like the IP addresses are enacted upon (re-)writing to the last control register (REG148)

Several key parameters are computed on the basis of the 160 MHz ADC clock $\mathbf{f_{clk\_adc}}$ or the 120 MHz internal processing clock $\mathbf{f_{clk\_p}}$.

RF	Configuration
Stored frequency $\mathbf{f_0}$	Preselected transmitter or receiver frequency $\mathbf{f_0}$. (one of eight stored frequencies) Valid range 925 MHz – 2.175 GHz, expressed in Hz. REG0: bit 7:0 (LSB) REG1: bit 15:8 REG2: bit 23:16 REG3: bit 31:24 (MSB)
Receiver frequency selection	Use to switch the receiver center frequency among preselected values. Range 0 through 7 REG6(2:0)
Transmitter frequency selection	Use to switch the transmitter center frequency among preselected values. Range 0 through 7 The rx/tx frequencies change is enacted upon writing to REG6. REG6(6:4)
Stored frequency $\mathbf{f_x}$	Seven additional preselected frequencies x = 1 through 7 Same format as $\mathbf{f_0}$. REG(3+4*x): bits 7:0 (LSB) REG(4+4*x): bits 15:8 REG(5+4*x): bits 23:16 REG(6+4*x): bits 31:24 (MSB)
Receiver RF Gain	Initial RF gain (before the RF AGC takes over). 12-bit. 0 for the minimum gain, 4095 for the maximum gain. The receiver RF gain change is enacted upon writing to REG5. REG4: bits 7:0 (LSB) REG5(3:0): bits 11:8
Receiver IF Gain	Initial IF gain (before the IF AGC takes over). 12-bit. 0 for the minimum gain, 4095 for the maximum gain. The receiver IF gain change is enacted upon writing to REG36. REG35: bits 7:0 (LSB) REG36(3:0): bits 11:8
Receiver LNA Gain	LNA gain 10-bit. 0 for the minimum gain, 1023 for the maximum gain. The receiver IF gain change is enacted upon writing to REG41. REG40: bits 7:0 (LSB) REG41(3:0): bits 11:8
Transmitter ALC target	The transmit gain is automatically adjusted so that the measured tx power equals this field. The transmitter gain change is enacted upon writing to REG38. REG37: bits 7:0 (LSB) REG38(3:0): bits 11:8
Receiver LNA AGC loop	0 = open loop. LNA path gain is fixed by control registers. 1 = AGC on. Gain is adjusted on the basis of the RSSI measurement. REG39(0)
Receiver RF AGC loop	0 = open loop. RF path gain is fixed by control registers. 1 = AGC on. Out-of-range conditions are detected at the RF mixer and IF power detector.

	REG39(1)
Receiver IFAGC loop	0 = open loop. IF1 path gain is fixed by control registers. 1 = AGC on. Out-of-range conditions are detected at the IF power detector. REG39(3:2)
Transmitter ON	0 = off 1 = on REG39(6)
LNB power (13/18V) ON	The transceiver is capable of supplying up to 500mA at 13VDC or 18VDC to an external LNB. This supply voltage is multiplexed with the RF input signal onto the "RF Rx" input. 0 = LNB supply off 1 = LNB supply on **Warning: Enabling the LNB supply may cause damage to test equipment unless a DC block is used.** REG43(0)
LNB power selection	0 = 13V 1 = 18V REG43(1)
General Parameters	**Configuration**
Internal/External frequency reference	10 MHz output generated from 10 MHz input (-B firmware option) or 19.2 MHz TCXO (-A firmware option) REG46(1): enable(1)/disable(0) CLKREF_OUT (special connector on front-panel) REG46(2): enable(1)/disable(0) CLK_LNB (multiplexed with received signal) REG46(3): enable(1)/disable(0) CLK_TX (multiplexed modulated transmit signal + 10 MHz)
FEC	
FEC encoding	0 = bypassed 1 = FEC encoding enabled REG47(0)
FEC decoding	0 = bypassed 1 = FEC decoding enabled REG47(1)
Convolutional encoding constraint length K and rate R	When the FPGA is configured with the convolutional/Viterbi FEC firmware version 0000 = (K=5, R=1/7) Intelsat IESS-308/309 0001 = (K = 7, R=1/2, Intelsat) 0010 = (K = 7, R=2/3, Intelsat) 0011 = (K = 7, R=3/4, Intelsat) 0100 = (K = 7, R=5/6, Intelsat) 0101 = (K = 7, R=7/8, Intelsat) 0110 = (K = 9, R=1/3) 0111 = (K = 9, R=1/2) 1000 = (K = 9, R=2/3) DVB ETS 300 421 DVB ETS 300 744

	1010 = (K = 7, R=1/2, DVB) 1011 = (K = 7, R=1/2, CCSDS) 1100 = (K = 7, R=2/3, CCSDS/DVB) 1101 = (K = 7, R=3/4, CCSDS/DVB) 1110 = (K = 7, R=5/6, CCSDS/DVB) 1111 = (K = 7, R=7/8, CCSDS/DVB) REG54(4:1)
Convolutional encoder: Differential Encoding	When the FPGA is configured with the convolutional/Viterbi FEC firmware version Differential encoding is useful in removing phase ambiguities at the PSK demodulator, at the expense of doubling the bit error rate. When enabled, the differential decoding must be enabled at the receiving end. There is no need to use the differential encoding to remove phase ambiguities at the PSK demodulator when the Viterbi decoder and HDLC decoder are enabled. 0 = disabled 1 = enabled REG54 (5)
Viterbi decoding constraint length K and rate R	When the FPGA is configured with the convolutional/Viterbi FEC firmware version 0001 = (K = 7, R=1/2, Intelsat) 0010 = (K = 7, R=2/3, Intelsat) 0011 = (K = 7, R=3/4, Intelsat) 0100 = (K = 7, R=5/6, Intelsat) 0101 = (K = 7, R=7/8, Intelsat) 1010 = (K = 7, R=1/2, DVB) 1011 = (K = 7, R=1/2, CCSDS) 1100 = (K = 7, R=2/3, CCSDS/DVB) 1101 = (K = 7, R=3/4, CCSDS/DVB) 1110 = (K = 7, R=5/6, CCSDS/DVB) 1111 = (K = 7, R=7/8, CCSDS/DVB) REG55(4:1)
Viterbi decoding: Differential Decoding	When the FPGA is configured with the convolutional/Viterbi FEC firmware version 0 = disabled 1 = enabled REG55(5)
Turbo code encoder Uncoded payload size in Bytes.	When the FPGA is configured with the turbo codec firmware version Preferred sizes: 14, 63, 250 Bytes Must NOT be an integer multiple of 15 Maximum 254 Bytes. REG95
Turbo code encoder rate	0 = rate 1/3 1 = rate 1/2 2 = rate 2/3

	3 = rate 3/4 4 = rate 4/5 5 = rate 5/6 6 = rate 6/7 7 = rate 7/8 REG96(3:0)
Turbo code encoder **E**ncoded frame size in bits	Encoded frame size in bits. For example: when payload size is 14, rate 1/3, the encoded frame size is 14*8*3 = 336 bits. Does not include any periodic synchronization field. REG97 LSB REG98(6:0) (MSB)
Turbo code decoder **D**ecoded payload size in Bytes.	Preferred sizes: 14, 63, 250 Bytes Must NOT be an integer multiple of 15 Maximum 254 Bytes. REG99
Turbo code decoder rate	0 = rate 1/3 1 = rate 1/2 2 = rate 2/3 3 = rate 3/4 4 = rate 4/5 5 = rate 5/6 6 = rate 6/7 7 = rate 7/8 REG100(3:0)
Turbo code decoder **C**oded frame size in bits	Coded frame size in bits. For example: when payload size is 14, rate 1/3, the coded frame size is 14*8*3 = 336 bits. Does not include any periodic synchronization field. REG101 LSB REG102(6:0) (MSB)
Turbo code decoder maximum number of iterations	1 – 15. Typical settings is 7. Must be an odd number REG103
Scrambling	
Scrambler enabled	Scrambling is performed after FEC encoding. Sync marker insertion is required in order for the descrambler to synchronize. 0 = bypassed 1 = enabled REG47(2)
Descrambler enabled	Descrambling is performed prior to FEC decoding. Sync marker insertion is required in order for the descrambler to synchronize. 0 = bypassed 1 = enabled REG47(3)
Scrambler key	32-bit key REG59-REG62
Descrambler key	32-bit key REG63-REG66
PSK Demodulator Parameters	**Configuration**
Tx-Rx loopback	REG42(0): enable (1) or disable(0) loopback test mode
Input frequency offset (f_{c_rx})	Modulated signal center frequency offset. Typically 0. 32-bit signed integer (2's complement representation) expressed as $f_{c\_rx} * 2^{32} / f_{clk\_adc}$

	REG85: LSB REG86 REG87 REG88: MSB
Frequency acquisition range (scan)	The demodulator natural frequency acquisition range is around 20% of the symbol range (depending on modulation, SNR). The frequency acquisition range can be extended by frequency scanning. Scanning steps are spaced ($f_{symbol\ rate\ rx}$ /4) apart. The user can thus trade-off acquisition time versus frequency acquisition range by specifying the number of scanning steps here. For example, 4 steps yield a frequency acquisition range of +/-$f_{symbol\ rate\ rx}$ REG94
AGC response	REG89(4:0)
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG89(5)
BPSK / QPSK decoding	0 = BPSK 1 = QPSK 2 = OQPSK REG89(7:6)
Symbol rate f_{symbol_rate}	$f_{symbol\_rate} * 2^{32} / f_{clk\_adc}$ REG90 = bits 7 – 0 (LSB) REG91 = bits 15 – 8 REG92 = bits 23 – 16 REG93 = bits 31 – 24 (MSB)
Detect and remove periodic sync marker	Enabled (1)/ Disabled(0) A periodic sync marker is required for synchronizing the turbo code decoder and the descrambler. It also helps resolving the demod phase ambiguity. Generally enabled unless compatibility with other systems is needed. REG47(5)
PSK Modulator Parameters	**Configuration**
Processing clock f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock. Expressed as as f_{clk_tx} = 120 MHz * M / (D * O)) where D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 1.0. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 1.0. Fixed point format 7.3 Note: the graphical use interface computes the best values for M, D and O. f_{clk_tx} recommended range 80-160 MHz. REG48(6:0) = D REG49 = M(7:0) REG50(1:0) = M(9:8) REG51 = O(7:0) REG52(1:0) = O(10:8)
Symbol rate f_{symbol_rate}	The modulator symbol rate is in the form $f_{symbol\ rate\ tx} = f_{clk\_tx} / 2^n$ where n ranges from 1 (2 samples per symbol) to 15 (symbol rate = f_{clk_tx} / 32768). n is defined in REG53(3:0)
Digital Signal gain	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend checking for saturation at the D/A converter when changing either the symbol rate or the signal gain. (see status registers SREG39)

	Enacted upon writing the MSB. REG67 = LSB REG68 = MSB
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation at the D/A converter when changing this parameter. (see status registers SREG39) REG69 = LSB REG70 = MSB
Modulation type	Modulation type 0 = BPSK 1 = QPSK 2 = OQPSK REG71(5:0)
Spectrum inversion	Invert Q bit. (Inverts the modulated spectrum only, not the subsequent frequency translation) 0 = off 1 = on REG71(6)
Input selection / format, test modes	Select the origin of the modulator input data stream. 0 = IP router WAN interface 1 = test sequence: internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream) 2 = test sequence: unmodulated carrier. This helps checking the follow-on RF modulator. 3 = input data from remote TCP client via the built-in LAN1/TCP server at port 1024 Test sequences override external input bit stream. REG72(2:0)
Output Center frequency ($\mathbf{f}_{c\_tx}$)	Fine tuning of center frequency. Typically 0 Hz. 32-bit signed integer (2's complement representation) expressed as $\mathbf{f}_{c\_tx} * 2^{32} / \mathbf{f}_{clk\_tx}$ For a clean output waveform, we recommend keeping the maximum frequency (center frequency + ½ symbol rate) below $1/10^{th}$ of the processing clock $\mathbf{f}_{clk\_tx}$. Note: as the AWGN noise samples are not frequency translated, noise tests should only be performed while the center frequency translation is smaller than the modulation bandwidth. REG73: LSB REG74 REG75 REG76: MSB
Sinusoidal frequency offset	In addition to the fixed frequency offset above, a sinusoidal frequency offset can be generated to mimic Doppler rate in highly mobile applications. This offset is characterized by two parameters: amplitude and period. The amplitude (a frequency) is expressed as $\mathbf{f}_{c\_amplitude} * 2^{32} / \mathbf{f}_{clk\_tx}$ in the following control registers: REG150: LSB REG151 REG152 REG153: MSB The period is expressed as $2^{32} / (\mathbf{f}_{clk\_tx} * T)$ in the following control registers: REG154: LSB

	REG155 REG156 REG157: MSB
Insert periodic sync marker	Enabled (1)/ Disabled(0) A periodic sync marker is required for synchronizing the turbo code decoder and the descrambler. It also helps resolving the demod phase ambiguity. Generally enabled unless compatibility with other systems is needed. REG47(4)
Network Interface	
Parameters	**Configuration**
LAN1 IP address	LAN1 is for monitoring & control and TCP server (IP router is on LAN2) 4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 REG132 (MSB) - REG135(LSB)
LAN1 Subnet mask	Typically 0x FF FF FF 00 (255.255.255.0) REG136 (MSB) - REG139(LSB)
LAN2 IP address	LAN1 is for payload data traffic through the built-in IP router. No monitoring and control capabilities. 4-byte IPv4 address. Example : 0x AC 10 01 81 designates address 172.16.1.129 The new address becomes effective immediately (no need to reset the ComBlock). REG140 (MSB) - REG143(LSB)
LAN2 Subnet mask	Typically 0x FF FF FF 00 (255.255.255.0) REG144 (MSB) – REG147(LSB)
LAN2 Gateway IP address	Where to forward IP frames received over the modem link but not destined to this LAN. REG108 (MSB) - REG111 (LSB)
IP forwarding	The IP router can be configured to forward(1) or not forward (0): REG148(0): IP multicast frames REG148(1): IP directed broadcast frames REG148(2): IP broadcast frames The recommended setting is zero.
LAN MAC address LSB	REG236(7:1). To ensure uniqueness of MAC address. The MAC address most significant bytes are tied to the FPGA DNA ID. However, since Xilinx cannot guarantee the DNA ID uniqueness, this register can be set at the time of manufacturing to ensure uniqueness.

DHCP server	
Parameters	**Configuration**
Enable DHCP server	Enable(1)/disable(0) DHCP server. The DHCP server automatically assigns IP addresses to devices on the LAN. REG112(0)
IP pool starting address	The DHCP server assigns IP addresses from a pool of contiguous addresses, starting at address x.y.z.REG113, where x.y.z are the most significant bytes of this IP router. REG113
IP pool size	Number of IP addresses in the DHCP pool. Constraint1: maximum 253. Constraint2: IP router IP address must be outside the pool address. Constraint3: REG113+REG114 < 254 REG114
Lease time	Lease time (in seconds) for the IP addresses dynamically assigned by the DHCP.

	REG115 (LSB) - REG118 (MSB)
Gateway IP address	In addition to assigning an IP address to devices which request it, the DHCP server informs those devices of the designated gateway IP address. In most cases, this IP address is that of the IP router (see control REG100-103) REG119 (MSB) – REG122 (LSB)
DNS address	In addition to assigning an IP address to devices which request it, the DHCP server informs those devices of a Domain Name Server (DNS) IP address. For example 8.8.8.8 for Google DNS. REG123 (MSB) – REG126 (LSB)
QoS bandwidth management LAN -> WAN IP forwarding	
EF PHB bandwidth quota (%)	Differentiated Services configuration: Percentage of the overall LAN-to-WAN transmit bandwidth allocated to the Expedited Forwarding (EF). Expressed as percentage: 128 represents 100%. REG127
AF1 PHB bandwidth quota (%)	Differentiated Services configuration: Percentage of the overall LAN-to-WAN transmit bandwidth allocated to the Assured Forwarding class 1 (AF1). Expressed as percentage: 128 represents 100%. REG128
AF2 PHB bandwidth quota (%)	Differentiated Services configuration: Percentage of the overall LAN-to-WAN transmit bandwidth allocated to the Assured Forwarding class 2 (AF2). Expressed as percentage: 128 represents 100%. REG129
AF3 PHB bandwidth quota (%)	Differentiated Services configuration: Percentage of the overall LAN-to-WAN transmit bandwidth allocated to the Assured Forwarding class 3 (AF3). Expressed as percentage: 128 represents 100%. REG130
AF4 PHB bandwidth quota (%)	Differentiated Services configuration: Percentage of the overall LAN-to-WAN transmit bandwidth allocated to the Assured Forwarding class 4 (AF4). Expressed as percentage: 128 represents 100%. REG131

Monitoring

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-4, SREG16-18 Properly operating hardware will result in the following sequence being displayed: SREG0-SREG4 = 01 F1 1D xx 7F, where xx (bad NAND flash sectors) must be less than 10 SREG16-18 = 0x22 22 87
Power supply check	SREG4(0): PGOOD1 RF1_+3.1V SREG4(1): PGOOD2 IF1+_3.1V SREG4(2): PGOOD3 A_+4.75V SREG4(3): PGOOD4 MOD_+4.8V SREG4(4): PGOOD5 TX_SYNTH_+3.3V SREG4(5): PGOOD6 RX_+4.75V SREG4(6): PGOOD7 RX_SYNTH_+3.3V Overall valid response: 0x7F
RSSI	Received signal strength indicator. 12-bit number Practical range –70 to -5 dBm after LNA See RF_POWER_DET1 in schematic. SREG5 = LSB SREG6(3:0) = MSB
Received power at RF mixer	Power detection at RF mixer. Target is 0xEC0 while the RF AGC is tracking See RF_POWER_DET2 in schematic. SREG7 = LSB SREG8(3:0) = MSB
Received power at IF	Power detection at IF after bandpass filter and IF gain control. Target is 0xE80 while the IF AGC is tracking. See IF1_POWER_DET in schematic. SREG9 = LSB SREG10(3:0) = MSB
Transmit power	Power detection at the RF transmit output. See TX_POWER_DET in schematic. SREG11 = LSB SREG12(3:0) = MSB
RF synthesizers locked	‘1’ when locked SREG19(0): rx synthesizer locked SREG19(1): tx synthesizer locked
FEC codec type	0 = convolutional K=7 rate ½ 1 = hardware TPC (when installed on PCB) 2 = turbo-code SREG19(7:4)
Demodulator monitoring	
Carrier lock status	SREG20(0) 0 = unlocked 1 = locked
Signal presence (from FFT)	SREG20(2) 0 = not present 1 = present
SOF locked	Detected periodic synchronization sequences SREG20(3) 0 = not synchronized 1 = synchronized
Inverse SNR	A measure of noise over signal power. 0 represents a noiseless signal. Valid only when demodulator is locked.

	SREG21
Carrier frequency offset1	Residual frequency offset with respect to the nominal carrier frequency. Part 1/2. Includes receiver frequency scanning and carrier tracking loop. 32-bit signed integer expressed as fcerror * 2^{32} / f_{clk_p} SREG22 (LSB) – SREG25 (MSB)
Carrier frequency offset2	Residual frequency offset with respect to the nominal carrier frequency. Part 2/2. Includes FFT-based frequency measurement (fixed after acquisition) 32-bit signed integer expressed as fcerror * 2^{31} / f_{symbol_rate} SREG26 (LSB) – SREG29 (MSB)
Turbo code decoder monitoring	
Frame error counter	SREG30 (LSB) – SREG33 (MSB)
Viterbi FEC decoder monitoring	
Synchronized	(FEC_DEC_LOCK_STATUS variable) Solid '1' when the Viterbi decoder is locked. '0' or toggling when unlocked. SREG30(0)
Decoder built-in BER	The Viterbi decoder computes the BER on the received (encoded) data stream irrespective of the transmitted bit stream. Encoded stream bit errors detected over a 1000-bit measurement window. SREG31 = bits 7 – 0 (LSB) SREG32 = bits 15 – 8 SREG33 = bits 23 – 16 (MSB)
BER tester monitoring	
Bit error rate	Monitors the BER (number of bit errors over 8,000,000 received bits) when the modulator is sending a PRBS-11 test sequence. SREG35: LSB SREG36: SREG37: SREG38: MSB
BER tester synchronized	SREG34(0): 1 when the BERT is synchronized with the received PRBS-11 test sequence.
Transmit SNR calibration	
Measured modulated signal power	SREG54(LSB) SREG55 SREG56(MSB)
Measured AWGN power (Noise bandwidth is twice the modulated signal bandwidth)	SREG57(LSB) SREG58 SREG59(MSB)
Tx saturation	Proper operation is predicated on operating in a linear channel, i.e. one without saturation. Saturation may occur after changing the symbol rate, the signal level or the noise level. Please verify the absence of saturation by reading this status register after adjusting these controls. Saturation occurrence in the last one second window for the following signals: Bit 0: PSK modulator output Bit 1: noise I-channel Bit 2: noise Q-channel Bit 3: signal + noise, I channel Bit 4: signal + noise, Q channel SREG39
IP router monitoring	
Parameters	**Monitoring**
MAC addresses	The 48-bit LAN1 ethernet MAC address is fixed and unique for each transceiver. It is displayed in status registers 19-24. The LAN2 Ethernet MAC address is incremented by

	one. SREG40-45
Transmitted to WAN	Monitors the number of payload bytes forwarded to WAN (does not include HDLC overhead or empty frames). 32-bit counter. SREG46 (LSB) to SREG49 (MSB)
Received from WAN	Monitors the number of payload bytes received from WAN (does not include HDLC overhead or empty frames). 32-bit counter. SREG50 (LSB) to SREG53 (MSB)

ComScope Monitoring

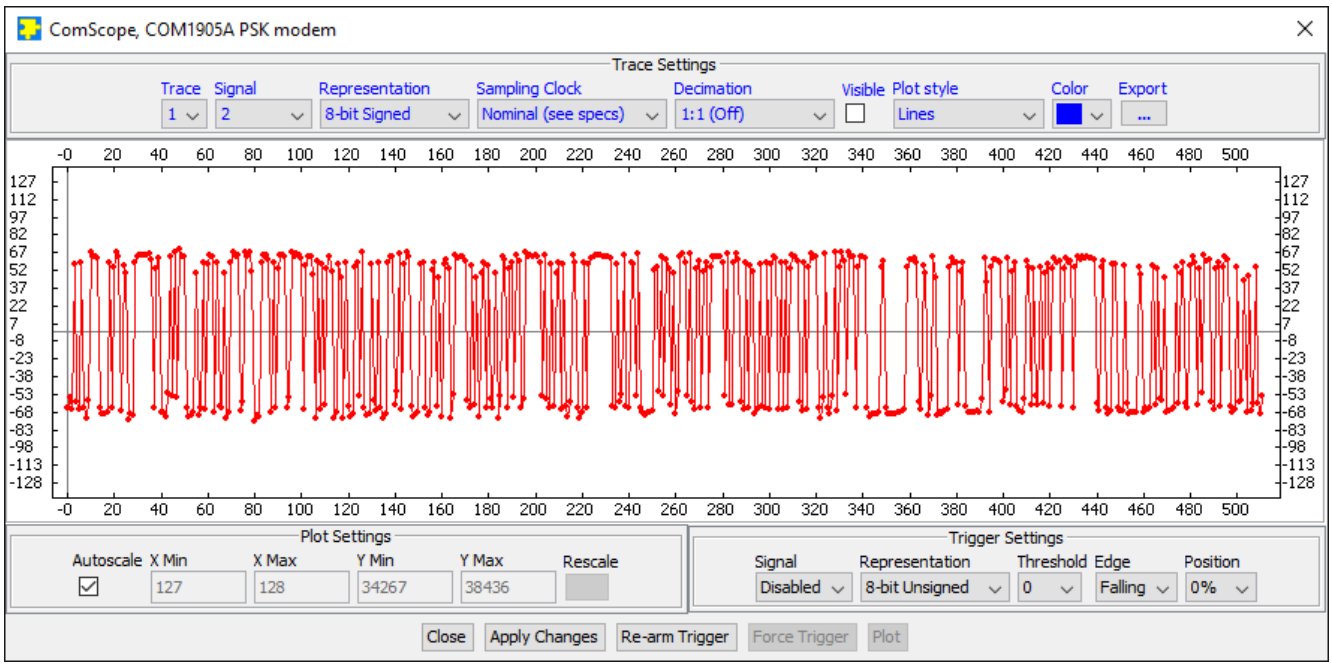
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. Click on the button to start, then select the signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: IF Input signal	8-bit signed	Input sampling rate	512
2: Input signal (I-channel) after AGC, frequency translation, decimation	8-bit signed	Input sampling rate/R	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Demodulated I-channel	8-bit signed	1 sample / symbol	512
2: AGC19 gain	8-bit signed	1 sample / symbol	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Demodulated Q-channel	8-bit signed	1 sample / symbol	512
2: Carrier tracking phase	8-bit signed	Input sampling rate/R	512
3: Symbol tracking phase (accumulated)	8-bit signed	1 sample / symbol	512
4: Inverse SNR	8-bit unsigned	1 sample / symbol	512
Trigger Signal	**Format**		
N/A			

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock.

In particular, selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope example: showing demodulated I-channel

LEDs

LED	Definition
Power	Green when power is applied
Alarm (red)	Red when one of these conditions occur: • Tx RF frequency synthesizer is out of lock • Rx RF frequency synthesizer is out of lock
Tx	Blink green when an IP frame is forwarded from LAN to WAN
Rx	Blink green when an IP frame is forwarded from WAN to LAN
Tx on	Yellow when the transmitter is on
Sync	Yellow when carrier lock, SOF lock and, when enabled, FEC decoder lock

Digital Test Points

The test points are only accessible after opening the enclosure. They are intended to be used only for debugging purposes.

Test Point	Definition
TP1 PLL_LOCK	Tx RF frequency synthesizer lock status ('1' when locked)
TP2 DONE	FPGA configured ('1' when successfully configured)
TP3 PLL_LOCK	Rx RF frequency synthesizer lock status ('1' when locked)
TP4 RSSI	Received signal strength indicator. Practical range –70 to -5 dBm after LNA

Operation

Power supply

This unit is designed for a +28V DC (18 – 36V) power supply. Power consumption depends somewhat on the configuration. Maximum power consumption: 350mA under 28V.
Power supply is through the front-panel connector.

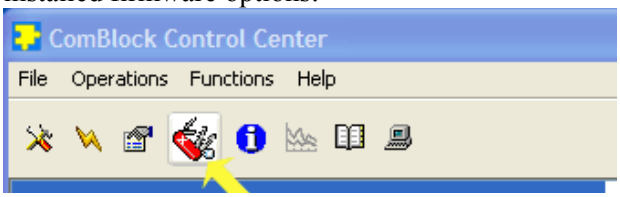
A lower supply voltage, down to 5.6V, can be used when the LNB supply output is unused.

Frequency reference

Depending on the firmware version loaded, the frequency reference is an external 10 MHz signal supplied through the front panel (**-B** firmware option) or an internal 19.2 MHz VC-TCXO (**-A** firmware option).
Both **-A** and **–B** firmware options are pre-loaded and can be switched easily.

Warning: when selected as external frequency reference, the 10 MHz frequency reference must be present prior to powering on the modem.

Click on the button below to switch between installed firmware options:



Output 10 MHz frequency reference

A 10 MHz frequency reference signal can be multiplexed with RF signals on the RF input (to an external LNB) and RF output (to an external BUC). The same 10 MHz is also available as an output on the front panel, labeled "10 MHz OUT". Each one of these three clocks signals can be enabled or disabled by software command.

Error Correction

Two error correction techniques are available, depending on the loaded firmware:

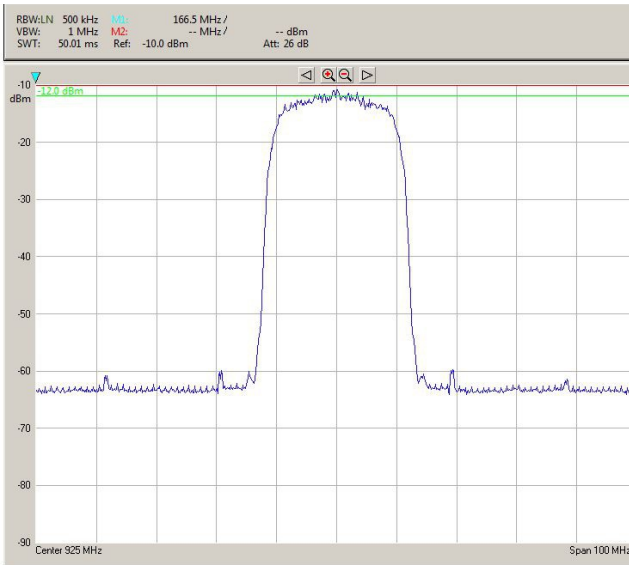
- Convolutional FEC K=7 rate ½, or
- Turbo Code (DVB-RCS2 standard)

Check the GUI or status register SREG19(7: 4) to verify which codec is currently active.

The convolutional FEC is only available for rate ½ (one redundancy bit for each information bit), whereas the Turbo-Code codec is flexible in its rate configuration.

Transmitted spectrum

Examples of transmitted spectrum are shown below:



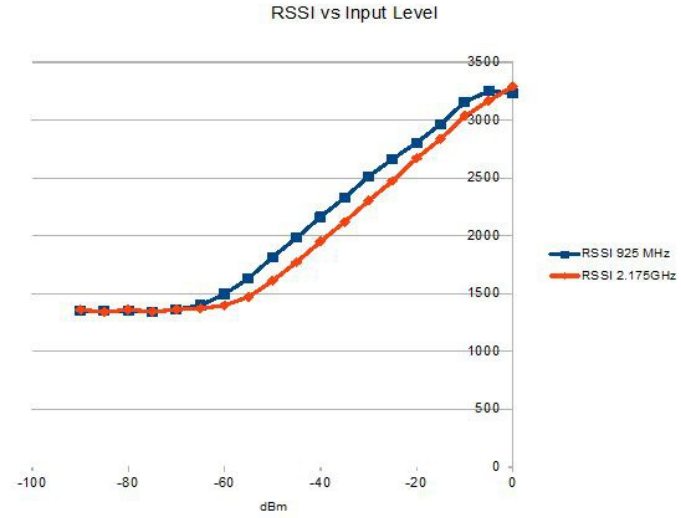
20 Msymbols/s QPSK

Scrambler

The bit stream can be scrambled prior to modulation and descrambled after demodulation. The scrambling sequence is generated by a 32-bit linear feedback shift register initialized with a 32-bit key. The scrambler and descrambler can be independently enabled and configured through control registers REG47, REG59-62, REG63-66.

RSSI

The RSSI measurements (as reported in status registers SREG5/6) versus the receiver input level is plotted below for the two extreme operational frequencies. The measurements are monotonous between -70 dBm and -5 dBm.



Note: RSSI measurement below –50Bm is affected by the presence of 10 MHz frequency reference when supplied to an external LNB (see control register REG46(2)).

Customization

The transceiver design can be customized to meet alternate customer requirements. The customizable features are

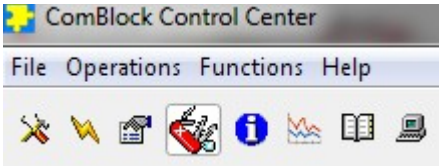
- Custom radio-frequency bands within 400 MHz– 3GHz at no extra charge.

Customization has to be specified and quoted at the time of order.

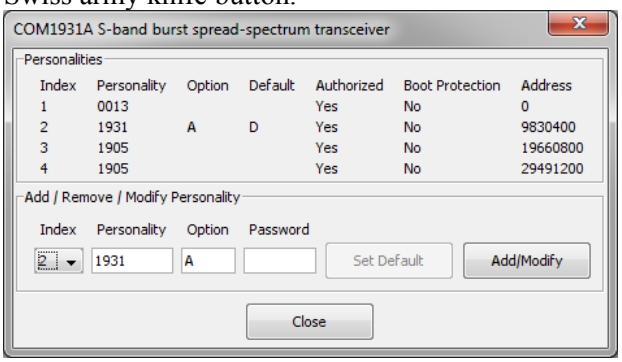
Load Software Updates

From time to time, ComBlock software updates are released.

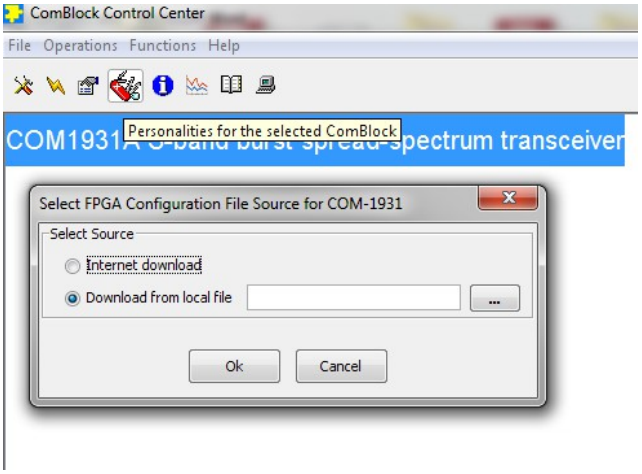
To manually update the software, highlight the ComBlock and click on the Swiss army knife button.



The receiver can store multiple personalities. The list of personalities stored within the ComBlock Flash memory will be shown upon clicking on the Swiss army knife button.



The default personality loaded at power up or after a reboot is identified by a 'D' in the Default column. Any unprotected personality can be updated while the Default personality is running. Select the personality index and click on the "Add/Modify" button.



The software configuration files are named with the .bit extension. The bit file can be downloaded via the Internet, from the ComBlock CD or any other local file.

The option and revision for the software currently running within the FPGA are listed at the bottom of the advanced settings window.

Two firmware options are available for this receiver:
-A firmware uses an internal VCTCXO frequency reference.
-B firmware option requires an external 10 MHz frequency reference.

Recovery

The toggle button under the backpanel can be used to

(α) Prevent the FPGA configuration at power up. This can be useful if a bad FPGA configuration was loaded which resulted in loss of communication with the user.
(β) Reset the LAN1 IP address to 172.16.1.128.

To prevent the FPGA configuration at power up, turn off power. Toggle the button. Turn on power, wait 1 second, then toggle the button a second time.

To reset the LAN1 IP address to a factory default of 172.16.1.128: Turn on power. Toggle the button, wait at least 30 seconds, during which time the red led blinks, then toggle the button a second time. Wait another 10 seconds, then cycle power off/on.

Interfaces

10/100/1000 Ethernet LAN for data, monitoring and control	Two RJ45 connectors Supports auto MDIX to alleviate the need for crossover cable. LAN1 is for monitoring and control only LAN2 is for IP routing
10 MHz frequency reference input	10 MHz frequency reference input for frequency synthesis. Sinewave, clipped sinewave or squarewave. SMA female connector Input is AC coupled. Minimum level 0.6Vpp. Maximum level: 3.3Vpp.
10 MHz frequency reference output	10 MHz frequency reference output generated either from the 10 MHz frequency reference input (**-B** firmware option) or from the internal TCXO (**-A** firmware option)
RF Rx	Receiver input. 50 Ohm, SMA female connector. Operating range: -60 to -10 dBm Maximum no damage input level: + 20 dBm Two other signals can be multiplexed onto the same coaxial connection between the COM-1905 transceiver and an external LNB: • 10 MHz frequency reference (software enabled) Level: -2 dBm typ. • 13/18V supply (software enabled)
RF Tx	Transmitter output. 50 Ohm, SMA female connector. Transmit level: -30 to 0 dBm, user selectable. One other signal can be multiplexed onto the same coaxial connection between the COM-1905 transceiver and an external BUC: • 10 MHz frequency reference (software enabled) Level: 0 dBm typ.

Operating input voltage range

Supply voltage	+18V min, +36V max 350mA typ. under +28VDC
Supply voltage (when no LNB 13/18V supply needed)	+5.6V min, +36V max

The positive voltage is on the center pin, the ground on the outer barrel.

Absolute maximum ratings

Supply voltage	+45 V max
RF input	+20dBm max

Mechanical Interface

Aluminum enclosure with rubberized end caps.
L x W x H: 168.5mm x 138.96 mm x 40.98 mm.
Includes two optional 40mm mounting flanges for mounting to a flat support plate.

Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1900schematics.pdf

Configuration Management

This specification is to be used in conjunction with VHDL software revision 1 and ComBlock control center revision 3.11g and above.

ARM processor firmware version:
CB1900_1_6b.hex 6/20/17

FPGA/VHDL version:
COM-1905_006 1/28/20

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1905 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

Troubleshooting Checklist

Excessive power consumption:

- The receiver input is capable of supplying 13/18V DC to an external LNB. When using RF attenuators at the input in a RF loopback test, please make sure to use a DC block between the RFin and the attenuator.

Demodulator can't achieve lock even at high signal-to-noise ratios:

- Make sure the modulator baseband I/Q signals do not saturate, as such saturation would strongly distort the modulation phase information. (this is a phase demodulator!)

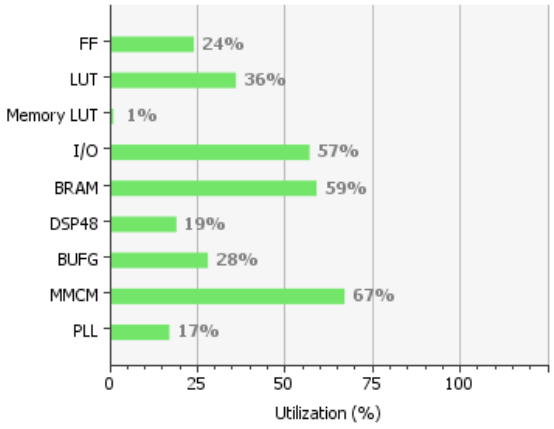
IP router does not forward IP frames to the WAN (Tx led not blinking):

- Make sure the sending PC has declared the LAN/IP2 address as "gateway"
- Verify that the modulator is configured in "IP router WAN interface" and is not in test mode.

VHDL code / IP core

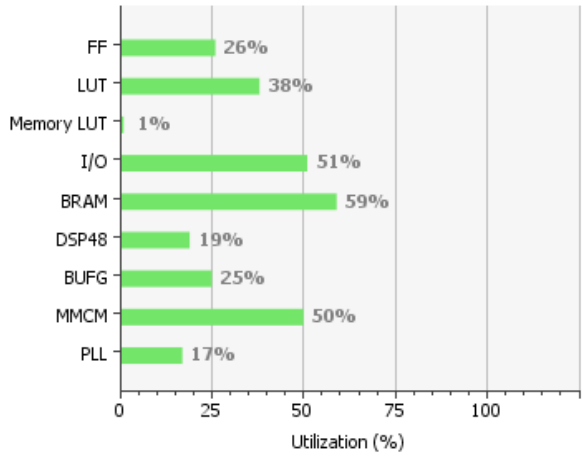
The FPGA code is written in VHDL. It does not use any third-party software. It occupies the following FPGA resources:

Turbo-Code codec case:



Resource	Utilization	Available	Utilization %
FF	30485	126800	24.04
LUT	22637	63400	35.71
Memory LUT	120	19000	0.63
I/O	162	285	56.84
BRAM	79.5	135	58.89
DSP48	46	240	19.17
BUFG	9	32	28.12
MMCM	4	6	66.67
PLL	1	6	16.67

Convolutional FEC case:



Resource	Utilization	Available	Utilization %
FF	33282	126800	26.25
LUT	24191	63400	38.16
Memory LUT	118	19000	0.62
I/O	146	285	51.23
BRAM	79.5	135	58.89
DSP48	46	240	19.17
BUFG	8	32	25.00
MMCM	3	6	50.00
PLL	1	6	16.67

The maximum symbol rate is limited by

- The FPGA technology. For example nearly 80 MSymbols/s for Xilinx Artix 7 –1 speed (XC7A100T-1)
- The receiver IF band-pass filter (40 MHz bandwidth)

The IP core, which includes all VHDL source code, can be purchased separately. It is not needed to operate the ready-to-use COM-1905 transceiver. See http://www.comblock.com/download/com1805soft.pdf

ComBlock Ordering Information

COM-1905 L/S-band continuous-mode PSK transceiver

ECCN: 5A001.b.3

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