COM-1833 TDRSS MODULATOR & CHANNEL SIMULATOR

Key Features

The COM-1833 implements real-time modulation and channel simulation of a TDRSS user-to-ground link in four distinct blocks, each with distinct parameters controls:

- TDRSS customer modulator, including spread-spectrum and narrow-band PSK
- TDRSS transponder induced distortions
- Ground terminal induced distortions
- Orbit dynamic effects

Supported input signals:

- Raw (unmodulated) user data received through the LAN/TCP server input
- Internal PRBS11 test sequence
- Synchronous serial input

Output signals (specify at the time or order):

- SDDS or VITA49 formatted stream transmitted over gigabit Ethernet (up to 25 MSamples/s) by either UDP or TCP protocol.
- Modulated RF output

All signal processing is implemented within a single FPGA. The same hardware can be configured as TDRSS DSSS demodulator (COM-1826 firmware) or TDRSS modulator and channel simulator (this COM-1833 firmware), depending on the selected firmware.

- Modulations:
  - Spread-spectrum (BPSK, SQPN) 3 MChips/s. Up to 300 Kbits/s per channel.
  - Narrow-band PSK(BPSK,QPSK,OQPSK,8-PSK) up to 6 MSymbols/s
- CCSDS error correction encoding:
  - Reed-Solomon
  - Interleaving
  - Convolutional
- Channel impairments:
  - Additive white Gaussian noise
  - Distortion FIR filter with programmable taps
  - 16-path multi-path emulation (Rician fading)
- Monitoring and Control:
  - Local (USB)

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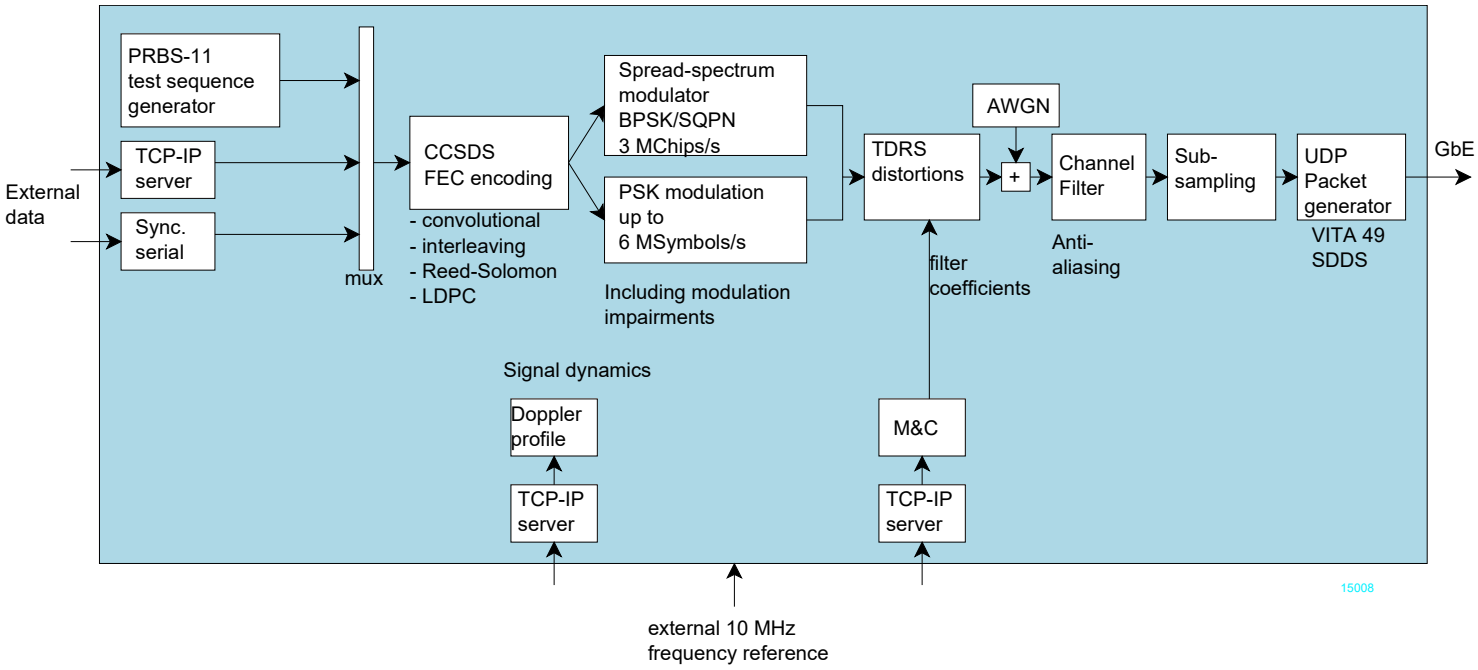
 Issued 7/30/2016

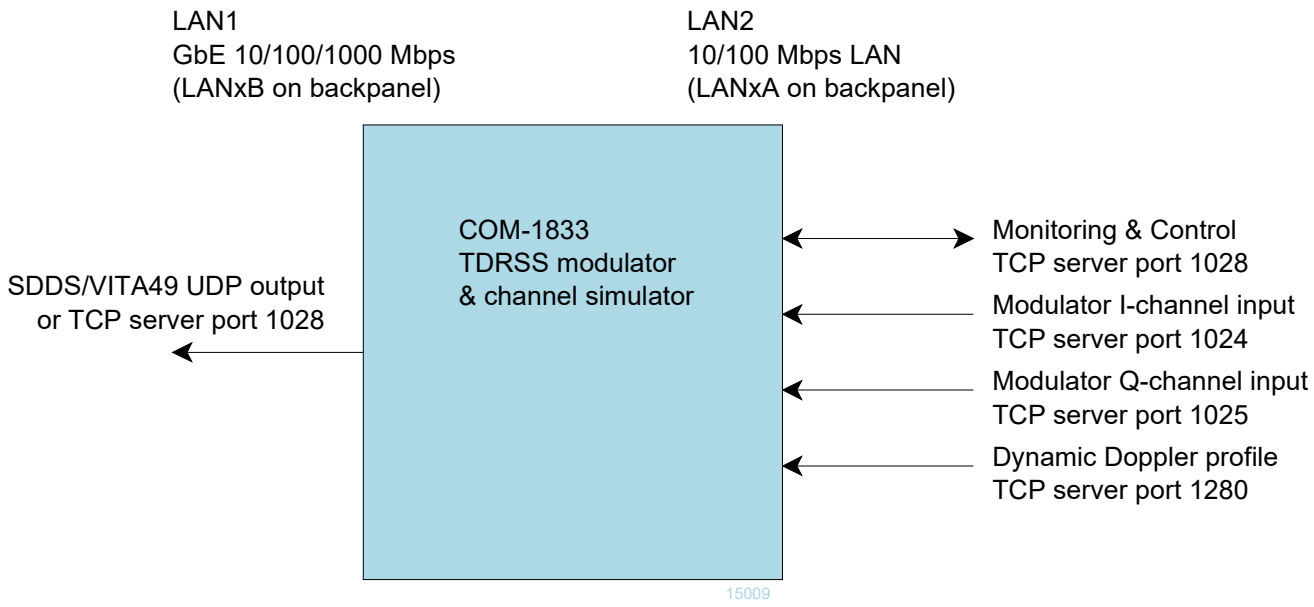
    - Remote (TCP-IP)
- Frequency reference:
    - Internal TCXO
    - External 10 MHz
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- 90VAC – 264VAC power supply

For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com1833.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

Block Diagram





LAN I/Os

Configuration

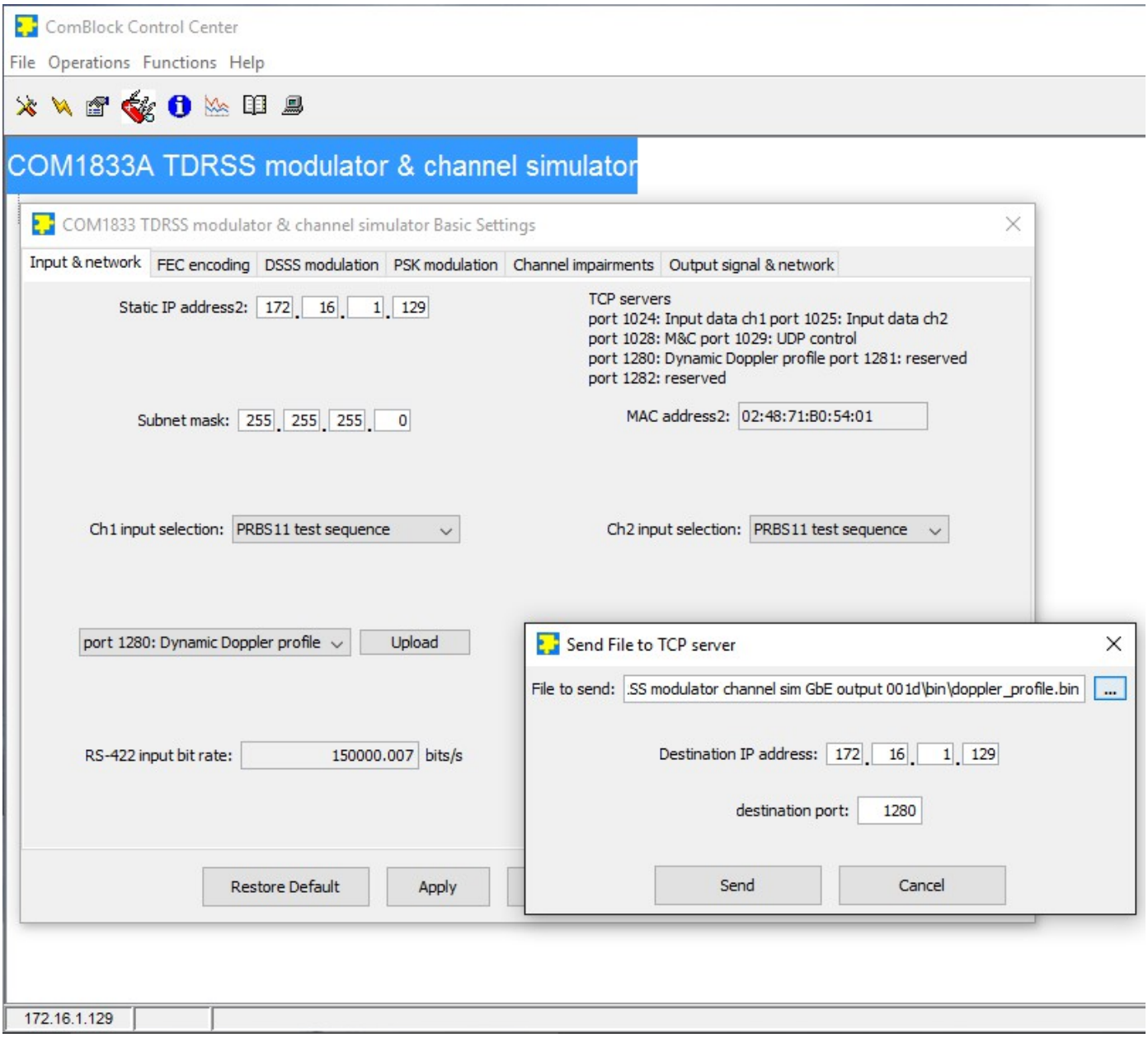
This ComBlock assembly can be monitored and controlled centrally over a single connection with a host computer. Connection types are:

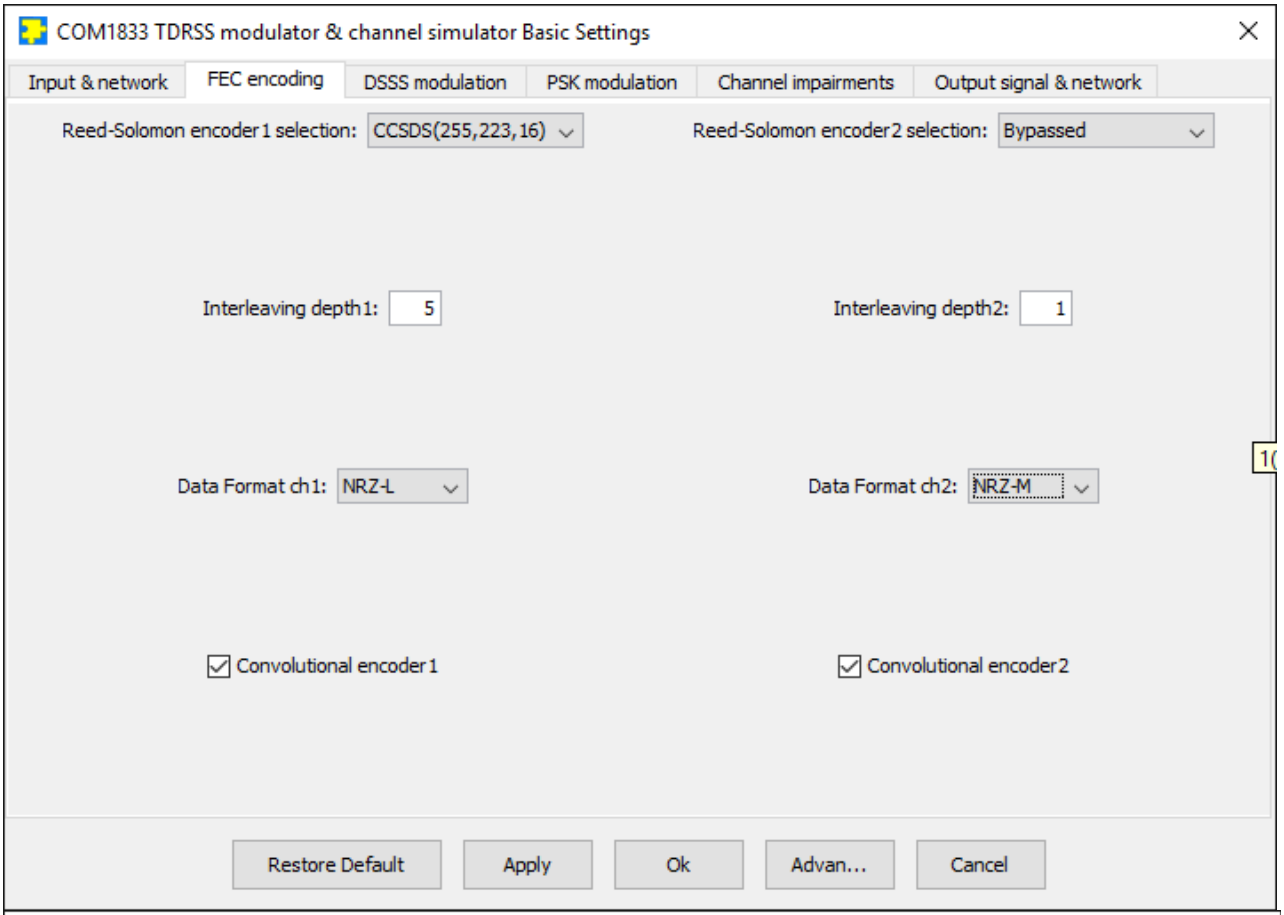
- USB
- TCP-IP/LAN

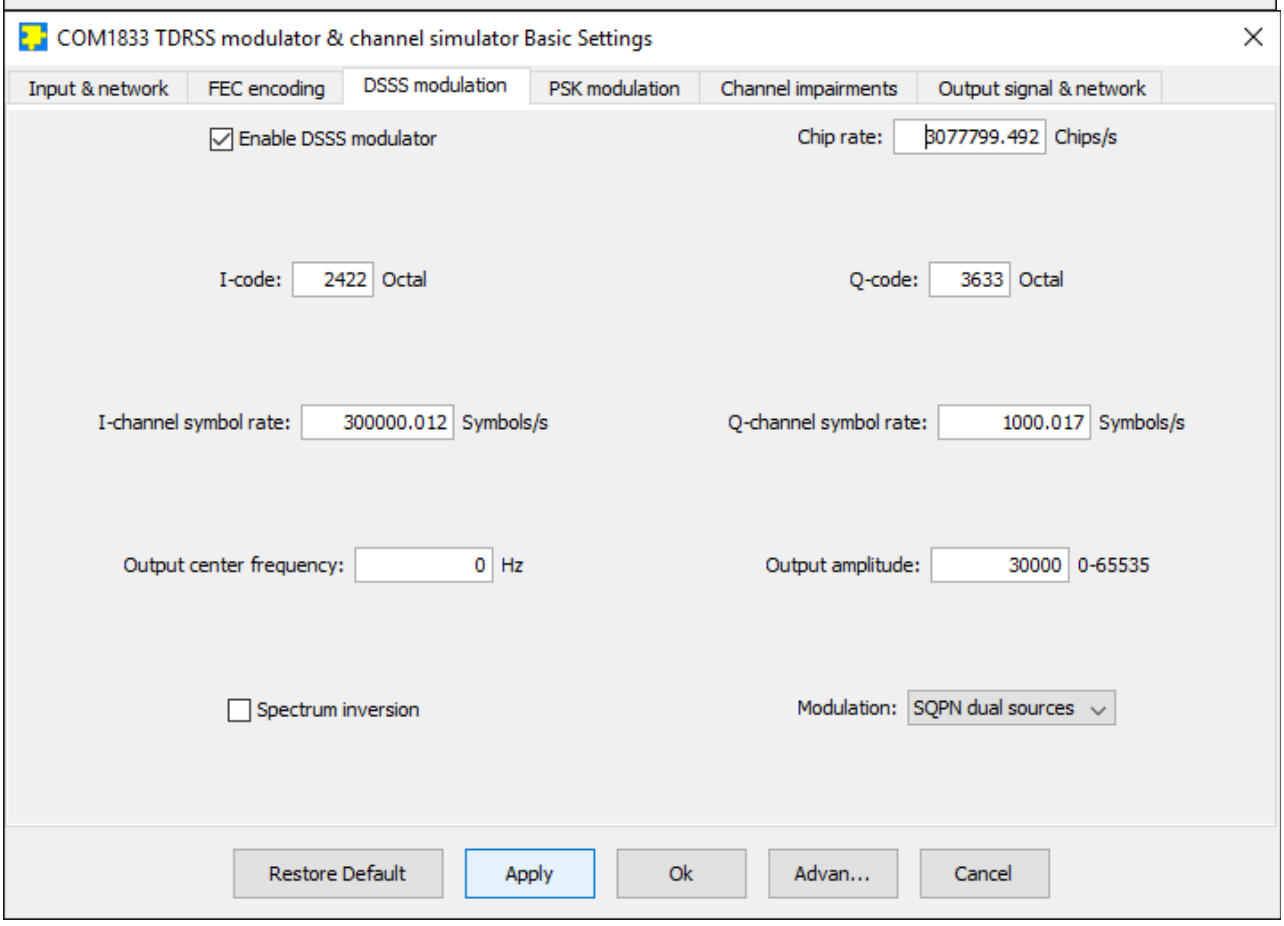
The module configuration is stored in non-volatile memory.

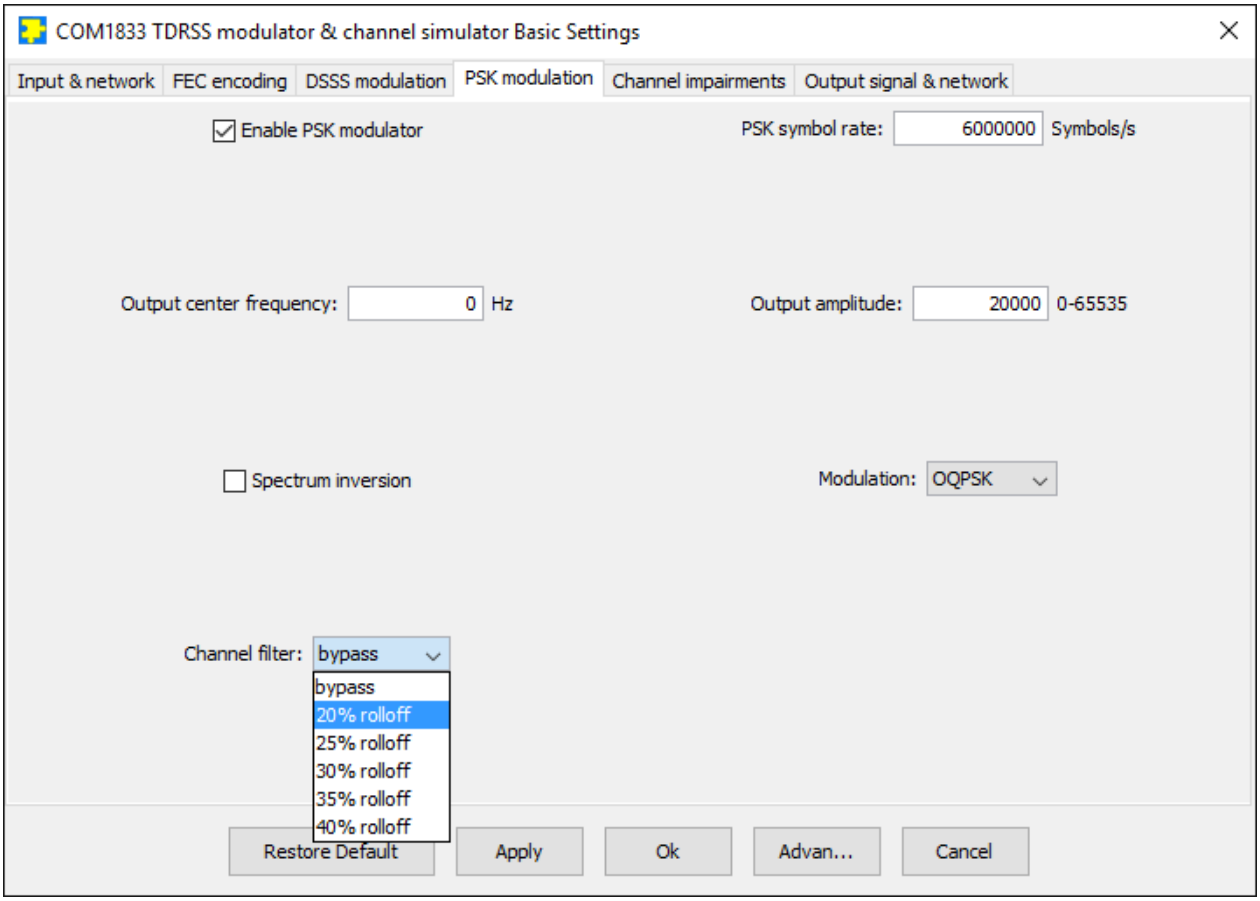
Configuration (Basic)

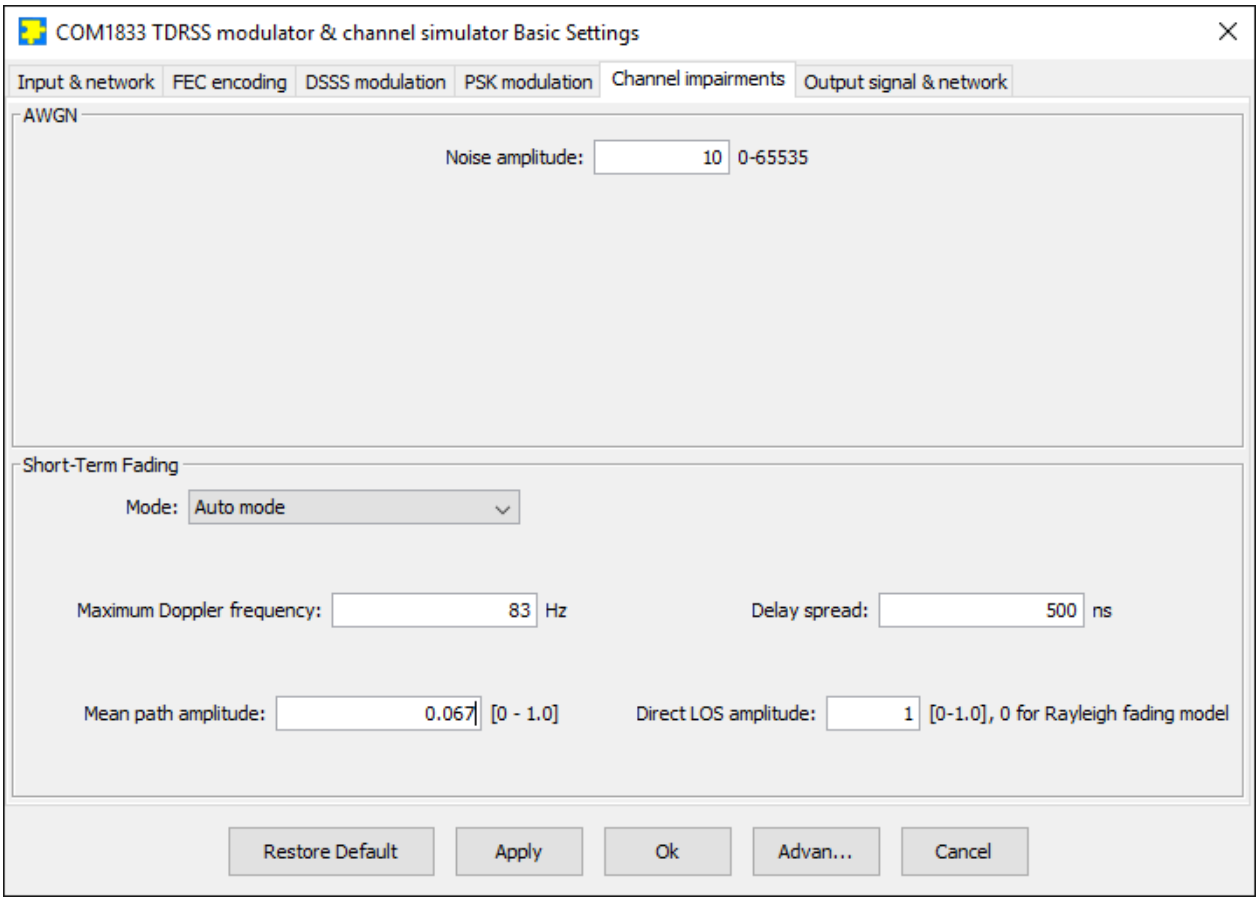
The easiest way to configure the COM-1833 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1833 module to be configured, next click the *Settings* button to display the *Settings* window shown below.

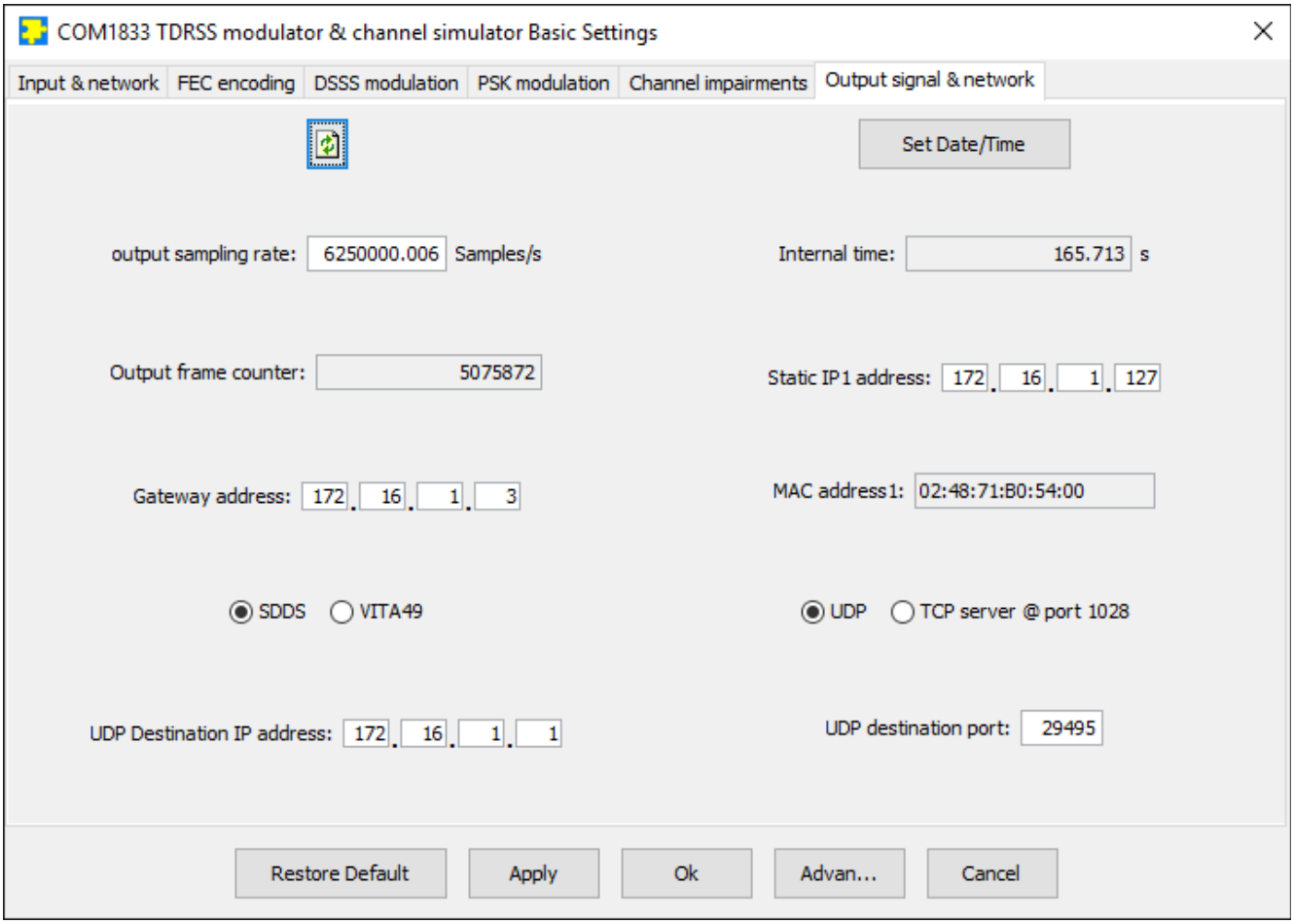



COM1833 TDRSS modulator & channel simulator Basic Settings
Input & network
FEC encoding
DSSS modulation
PSK modulation
Channel impairments
Output signal & network
Reed-Solomon encoder1 selection:
CCSDS(255,223,16)
Reed-Solomon encoder2 selection:
Bypassed
Interleaving depth1:
5
Interleaving depth2:
1
Data Format ch1:
NRZ-L
Data Format ch2:
NRZ-M
Convolutional encoder1
Convolutional encoder2
Restore Default
Apply
Ok
Advan...
Cancel


COM1833 TDRSS modulator & channel simulator Basic Settings
Input & network
FEC encoding
DSSS modulation
PSK modulation
Channel impairments
Output signal & network
Enable DSSS modulator
Chip rate:
3077799.492
Chips/s
I-code:
2422
Octal
Q-code:
3633
Octal
I-channel symbol rate:
300000.012
Symbols/s
Q-channel symbol rate:
1000.017
Symbols/s
Output center frequency:
0
Hz
Output amplitude:
30000
0-65535
Spectrum inversion
Modulation:
SQPN dual sources
Restore Default
Apply
Ok
Advan...
Cancel


COM1833 TDRSS modulator & channel simulator Basic Settings
Input & network
FEC encoding
DSSS modulation
PSK modulation
Channel impairments
Output signal & network
Enable PSK modulator
PSK symbol rate:
6000000
Symbols/s
Output center frequency:
0
Hz
Output amplitude:
20000
0-65535
Spectrum inversion
Modulation:
OQPSK
Channel filter:
bypass
bypass
20% rolloff
25% rolloff
30% rolloff
35% rolloff
40% rolloff
Restore Default
Apply
Ok
Advan...
Cancel


COM1833 TDRSS modulator & channel simulator Basic Settings
Input & network
FEC encoding
DSSS modulation
PSK modulation
Channel impairments
Output signal & network
AWGN
Noise amplitude:
10
0-65535
Short-Term Fading
Mode:
Auto mode
Maximum Doppler frequency:
83
Hz
Delay spread:
500
ns
Mean path amplitude:
0.067
[0 - 1.0]
Direct LOS amplitude:
1
[0-1.0], 0 for Rayleigh fading model
Restore Default
Apply
Ok
Advan...
Cancel



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Several key parameters are computed on the basis of two frequency references: the 125 MHz internal processing clock f_{clk_p} or of the 160 MHz DAC clock f_{clk_dac}

Transmitter	
Parameters	**Configuration**
Channel 1 modulator input selection	0 = disabled 1 = TCP server at port 1024 2 = PRBS11 test sequence 3 = zeros 4 = synchronous serial via left connector 5 = periodic 32-bit sequence 0x"DEADBEEF" REG1(2:0)
Channel 2 modulator input selection	0 = disabled 1 = TCP server at port 1025 2 = PRBS11 test sequence 3 = zeros REG1(5:4)
Serial tx bit rate	Set the nominal input bit rate for the synchronous serial input. A serial clock will be supplied to the data source. Must be consistent with the modulator symbol rate, modulation type, FEC rate. $f_{input\ bit\ rate\ tx} * 2^{32} / f_{clk\_p}$ REG31 (LSB) – REG34 (MSB)

FEC encoding / interleaving	
Parameters	**Configuration**
Channel 1 Reed-Solomon encoder type	5 = CCSDS(255,223,16) 6 = CCSDS(255,239,8) REG2(3:0)
Channel 2 Reed-Solomon encoder type	5 = CCSDS(255,223,16) 6 = CCSDS(255,239,8) REG2(7:4)
Channel 1 Reed-Solomon frame interleaving depth	Interleaving depth: 1 means no interleaving Valid settings: 1,2,3,4,5,8 REG3(3:0)
Channel 2 Reed-Solomon frame interleaving depth	Interleaving depth: 1 means no interleaving Valid settings: 1,2,3,4,5,8 REG3(7:4)
Reed-Solomon encoder enable	Enable(1) or bypass(0) REG4(0) channel 1 RS encoder REG4(1) channel 2 RS encoder
Convolutional encoder enable	Enable(1) or bypass(0) REG4(4) ch. 1 convolutional encoder REG4(5) ch. 2 convolutional encoder

DSSS modulator	
Parameters	**Configuration**
DSSS modulator enable	0 = disabled 1 = enabled REG30(7)
Chip rate (fchip rate)	The nominal chip rate is 3.077799479166 Mchips/s. However, the design is somewhat more flexible. Alternative chip rates can be entered here 32-bit integer expressed as fchip rate * 2^{32} / f_{clk_dac}. The maximum practical chip rate is f_{clk_p} /2. Nominal chip rate: 0x04ECAAAB REG5 (LSB) – REG8 (MSB)
I Code	Linear feedback shift register initialization. As per [1] REG9 LSB REG10(2:0) MSb
Q Code	REG11 LSB REG12(2:0) MSb
I channel symbol rate f_{symbol_rate}	The I-channel symbol rate can be set independently of the spreading code period as f_{symbol_rate} * 2^{32} / f_{clk_dac} Example: "0028F5C3" represents 100 Ksymbols/s. REG13 (LSB) – REG16 (MSB)
Q channel symbol rate f_{symbol_rate}	The Q-channel symbol rate can be set independently of the spreading code period as f_{symbol_rate} * 2^{32} / f_{clk_dac} REG17(LSB) – REG20 (MSB)
Modulated signal amplitude	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend checking for saturation when changing either the symbol rate or the signal gain. REG21 = LSB REG22 = MSB
Output center frequency (f_c)	Fixed frequency offset applied to the output samples. It is used for fine frequency corrections, for example to correct clock drifts. 32-bit signed integer (2's complement representation) expressed as f_c * 2^{32} / f_{clk_dac} In addition to this fixed value, an optional time-dependent frequency profile can be entered. See frequency profile table. REG25 (LSB) – REG28 (MSB)
Spectrum inversion	Invert Q bit 0 = off 1 = on REG30(0)
BPSK / SQPN	0 = BPSK 1 = SQPN REG30(1)
SQPN single/double source	0 = dual source: independent symbol rates on I and Q channels 1 = identical data on I and Q channels (prior to coherent sum) REG30(2)
Data formatting I-channel	0 = NRZ-L 1 = NRZ-M 2 = NRZ-S REG10(5:3)
Data formatting Q-channel	0 = NRZ-L 1 = NRZ-M 2 = NRZ-S REG10(5:3)

PSK modulator	
Parameters	**Configuration**
PSK modulator enable	0 = disabled 1 = enabled REG36(7)
PSK type	0 = BPSK 1 = QPSK 2 = OQPSK 11 = 8-PSK REG35(5:0)
Spectrum inversion	Invert Q bit 0 = off 1 = on REG35(6)
Channel filter	0 = bypassed 1 = root raised cosine filter 20% rolloff 2 = root raised cosine filter 25% rolloff 3 = root raised cosine filter 30% rolloff 4 = root raised cosine filter 35% rolloff 5 = root raised cosine filter 40% rolloff REG36(2 downto 0)
Symbol rate f_{symbol_rate}	The PSK modulator symbol rate is expressed as $f_{symbol\_rate} * 2^{32} / f_{clk\_dac}$ Example: "0028F5C3" represents 100 Ksymbols/s. REG37 (LSB) – REG40 (MSB)
Output center frequency (f_c)	Fixed frequency offset applied to the output samples. It is used for fine frequency corrections, for example to correct clock drifts. 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk\_dac}$ In addition to this fixed value, an optional time-dependent frequency profile can be entered. See frequency profile table. REG41 (LSB) – REG44 (MSB)
Modulated signal amplitude	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend checking for saturation when changing either the symbol rate or the signal gain. REG45 = LSB REG46 = MSB

Multi-Path Fading Configuration (Auto mode)	
Mode	1 = clears all paths parameters such as amplitude scaling coefficients, delays, phase offsets, frequency offsets. Only the direct path amplitude is left unchanged. 2 = manual mode. User is responsible for defining the multi-path parameters. 3 = auto mode, single draw: multi-path random parameters are generated automatically for all paths. 4 = auto mode. Multi-path random parameters are periodically updated automatically for all paths. The update rate is approximately 20ms. REG91(2:0)
Maximum Doppler f_m	Maximum Doppler frequency in Hz. REG92 (LSB) – REG94 (MSB)
Delay spread standard deviation Δ_τ	Expressed in ns. Note that, because of the exponential distribution, the mean equals the standard deviation. REG95 (LSB) – REG97 (MSB)
Multi-path amplitude mean.	Fixed-point format 0.16 REG98 (LSB) – REG99 (MSB)
Direct Path (line-of-sight) amplitude k_d	k_d is the direct, line-of-sight, component amplitude. The Rician Fading is disabled when k_d is set to zero. Fixed-point format 0.16 REG100 (LSB) – REG101 (MSB)
Multi-Path Fading Configuration (Manual mode) Because of the dynamic (frequently changing) nature of these parameters, storing values in non-volatile registers is not recommended. Instead API users should use the "SRT" Set Register Temporary command.	
Parameters	**Configuration**
Path index i	Indirect addressing for the paths parameters. This field identifies the path associated with the delay, phase rotation and frequency offset below. Path index i is in the range 0 to 15. REG102(4:0)
Coefficient W_i	Unsigned (positive) 16-bit precision coefficient. 16 coefficients are referred to by their path index i in the range 0 to 15. The amplitude scaling coefficient W_i

	are expressed as a numerical value in 0.16 fractional binary format (meaning 16 bits following the decimal point). Near unit gain is 0xFFFF. REG103 = W_i (7:0) REG104 = W_i (15:8)
Delay D_i	Delay expressed as number of input samples. Valid range 0 – 511 samples. REG105 = D_i (7:0) REG106 (0) = D_i (8)
Phase Rotation φi	Phase rotation at the start of the simulation. As this is an initial condition, changes to the phase rotation are only enacted upon software reset. Unsigned 12-bit number representing a phase rotation in the range 0 (inclusive) to 360 degrees (exclusive) by steps of approximately 0.1 deg. REG107 = φi (7:0) REG108(3:0) = φi (11:8)
Frequency offset f_i	Signed 24-bit number. Computed as f_i /decimated sampling rate $*2^{24}$ For example, since the sampling rate is f_{clk_dac} = 160 MHz, the frequency offset step size is 9.5 Hz. REG109 = f_i (7:0) REG110 = f_i (15:8) REG111 = f_i (23:16)

Channel impairments	
Parameters	**Configuration**
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation when changing this parameter. REG47 = LSB REG48 = MSB
Reset time	The simulator internal time is set to zero at power up. It can be set to the proper time/date (typically the time since January 1, 1970, 00:00:00 GMT) by writing to control register REG90(0). The reset time format depends on the SDDS or VITA49 output format selection. SDDS: Time in 250ps units since January 1, 1970, 00:00:00 GMT REG82(LSB) through REG89(MSB) VITA49: REG82 (LSB) – REG85(MSB) 32 LSBs fractional-seconds timestamp expressed in 256ps units. This real-time timestamp is reset every second. REG86 (LSB) – REG89(MSB) 32-bit integer-seconds timestamp expressed in seconds.
Set time	Writing 1 to this register sets the simulator local time as defined in control registers 82 through 89. REG90(0)

GbE LAN output	
Parameters	**Configuration**
Sampling rate ($f_{resampling}$)	The modulated baseband samples, including impairments, are resampled prior to transmission over GbE. The resampling rate is a 32-bit signed integer expressed as $f_{resampling} * 2^{32} / f_{clk\_p}$ For example 0x33333333 for 25 MSamples/s Hint: to disable the LAN output, set the sampling rate to zero. REG78 (LSB) – REG81 (MSB)
Samples format selection	The samples are sent to the receiver under test via a gigabit Ethernet LAN, using either SDDS (0) or VITA49(1) formatting. REG49(0)
Output protocol	The samples are sent to the receiver under test via a gigabit Ethernet LAN, using either UDP or TCP protocol. In the TCP case, the modulator/simulator acts as a TCP server. The receiver under test must first initiate a TCP connection with this TCP server at port 1028. Select UDP (0) or TCP server (1) REG49(4)
IP1 static address (LANxB connector on backpanel)	Local 4-byte IPv4 address used for SDDS/VITA49 output stream. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG50 (MSB) – REG53 (LSB)
IP1 destination IP address	4-byte IPv4 address Unicast or multicast destination IP address for SDDS/VITA49 output stream when selecting UDP protocol. Ignored when configured as TCP server. REG54 (MSB) – REG57(LSB)
IP1 Destination ports	UDP destination port for SDDS/VITA49 output stream when selecting UDP protocol. Ignored when configured as TCP server. REG58(LSB) – REG59(MSB)
IP2 address (LANxA connector on backpanel)	Local 4-byte IPv4 address used for modulator data input, dynamic profiles, monitoring and control. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG68 (MSB) – REG71 (LSB)
Subnet mask	REG60 (MSB) – REG63(LSB)
Gateway IP address	REG64 (MSB) – REG67(LSB)
MAC addresses LSB	Each LAN MAC address is tied to a almost unique ID embedded in each FPGA. To minimize the probability of identical hardware IDs, append the user-defined REG236 byte as MAC address LSB. Usage: defined once at initial installation.

(Re-)Writing to control register REG111 is recommended after a configuration change to enact the change.

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-9 Properly operating hardware will result in the following sequence being displayed: SREG0-SREG9 = 01 F1 1D xx 1F 93 10 22 22 03
External 10 MHz presence	1 = detected 0 = missing SREG9(7)
TCP connections	'1' when TCP connection, 0 otherwise Bit 0: monitoring & control, port 1028 Bit 1: input data channel 1, port 1024 Bit 2: input data channel 2, port 1024 Bit 3: Doppler profile, port 1280 Bit 4: Attenuation profile, port 1281 Bit 5: Delay profile, port 1282 SREG10(5:0)
MAC address1	Unique 48-bit hardware address (802.3). Add one to the last byte to get MAC address2. In the form SREG11:SREG12:SREG13:…:SREG16
Time	64-bit internal time. Two different formats depending on the selected SDDS or VITA49 output format: SDDS: SREG17 (LSB) – SREG24(MSB) 64-bits Expressed in 250ps units. VITA49: SREG17 (LSB) – SREG20(MSB) 32 LSBs fractional-seconds timestamp expressed in 256ps units. This real-time timestamp is reset every second. SREG21 (LSB) – SREG24(MSB) 32-bit integer-seconds timestamp expressed in seconds.
Output frame counter	Cumulative SDDS/VITA49 frame counter. Each frame contains 1024 bytes = 256 complex samples. This counter is different from the frame counter in the SDDS header (which only has 17 bits and skip one count every 32 frames). SREG25 (LSB) – SREG28(MSB)
Saturation	Proper operation is predicated on operating in a linear channel, i.e. one without saturation. Saturation may occur after changing the symbol rate, the signal level or the noise level. Please verify the absence of saturation by reading this status register after adjusting these controls. Saturation occurrence in the last one second window for the following signals: Bit 0: DSSS modulator output Bit 1: PSK modulator output Bit 2: noise I-channel Bit 3: noise Q-channel Bit 4: signal + noise, I channel Bit 5: signal + noise, Q channel Bit 6: multi-path, I channel Bit 7: multi-path, Q channel SREG29
Nominal center frequency	Expected center frequency: sum of the fixed center frequency and the dynamic frequency profile table. SREG41 (LSB) – SREG44 (MSB)

Built-in modulator SNR calibration	
Parameters	**Monitoring**
Measured modulated signal power	SREG61(LSB) SREG62 SREG63(MSB)
Measured AWGN power (Noise bandwidth is 6.25 MHz)	SREG64(LSB) SREG65 SREG66(MSB)

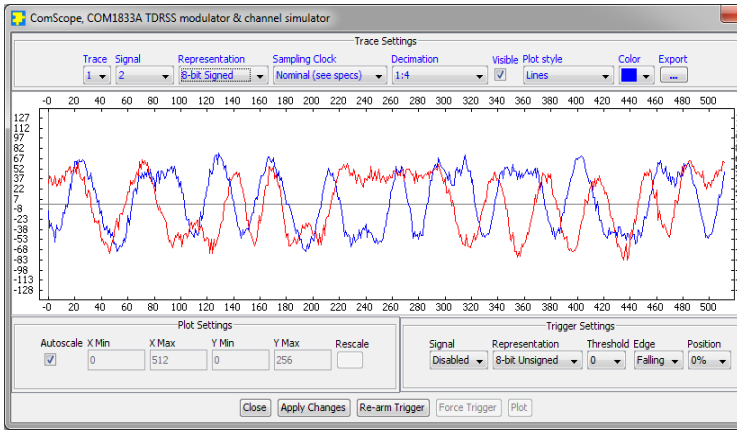
FPGA configuration options	
Parameters	**Monitoring**
DACs_EN	DAC interface instantiated (1) or not (0) SREG30(0)
LEFT_MODULE	0 = SDDS/VITA-49 GbE output enabled 1 = synchronous serial input enabled SREG30(1)

Multi-byte status variables are latched upon (re-)reading SREG7.

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. Click on the button to start, then select the signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Modulated I-channel	8-bit signed	f_{clk_dac}	512
2: I-channel after impairments and AWGN	8-bit signed	f_{clk_dac}	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Modulated Q-channel	8-bit signed	f_{clk_dac}	512
2: Q-channel after impairments and AWGN	8-bit signed	f_{clk_dac}	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Dynamic Doppler profile (bits 31:24)	8-bit signed	f_{clk_dac}	512
2: Dynamic Doppler profile (bits 26:19)	8-bit signed	f_{clk_dac}	512
3: Dynamic Doppler profile (bits 21:14)	8-bit signed	f_{clk_dac}	512
4: Dynamic Doppler profile (bits 16:9)	8-bit signed	f_{clk_dac}	512
Trigger Signal	**Format**		
1: Doppler dynamic profile playback	Binary		



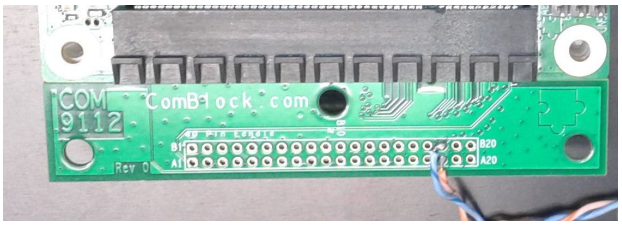
ComScope example, showing SQPN spread-spectrum modulation with very little additive white Gaussian noise. Blue = I-channel, Red = Q-channel

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk_dac} DAC sampling clock as real-time sampling clock.

In particular, selecting the f_{clk_dac} DAC sampling clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

Digital Test Points



Test Point	Definition
A1	SDDS/VITA-49 resampling clock
A2	SDDS/VITA-49 UDP frame transmit acknowledgement
A3	SDDS/VITA-49 UDP frame transmit NAK
A4	Doppler dynamic profile playback state
A5	Saturation at DSSS modulator output
A6	Saturation at PSK modulator output
A7	Saturation at the AWGN generator output
A8	Saturation while summing modulated signal and AWGN

Operation

Input data stream

The input data stream can originate from three sources:

1. Internal pseudo-random sequence generator (this facilitates measuring the transmission channel bit error rate)
2. External data stream sent to the TCP server
3. Synchronous serial data stream. The simulator provides an output clock and expects the input data bit to be stable at the clock falling edge (i.e. the source generates the data bit at the rising edge).

The synchronous serial data input feature is mutually exclusive with the SDDS/VITA-49 output [connector cannot be shared]

Monitoring & Control

M&C is possible over USB and LAN/TCP.

A pre-requisite for using USB is the prior installation of the ComBlock USB driver.

Monitoring and control is through the USB and LAN xA connectors on the back panel.

At manufacturing, the default M&C LAN address is 172.16.1.2. It can be subsequently changed via USB or LAN/TCP.

The LAN xA connector is also shared with TCP connections for modulator inputs and dynamic profiles inputs.

SDDS / VITA49 output stream

The LAN xB connectors on the back panel are reserved for SDDS or VITA49-formatted output streams.

The output stream is sent using UDP source port 1280 [destination port is user-selectable] or TCP-IP server port 1028. Control register REG49(4) selects UDP versus TCP.

Even though modulation and channel impairments are implemented at f_{clk_dac} 160 MSamples/s, the GbE LAN limits the final sampling rate to 25 MSamples/s. The sampling rate is user programmable.

The output frames are time-tagged with a 64-bit local time.

External frequency reference

A 10 MHz external frequency reference is recommended for proper operation. The electrical characteristics are as follows:

Sinewave, clipped sinewave or squarewave. AC-coupled.

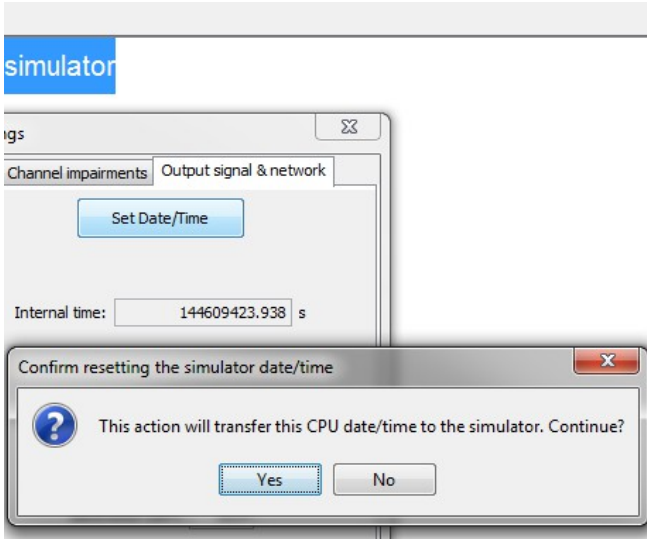
Minimum level: 2Vpp.
Maximum level: 5Vpp.

Using the same 10 MHz frequency reference at the modulator and the receiver under test eliminates the occurrence of buffer underflow or overflow conditions when UDP is the protocol used to convey samples.

When the output signal is conveyed over TCP, the use of a higher stability 10 MHz frequency reference is not required to prevent underflow or overflow conditions, as the TCP protocol informs the data source of flow-control conditions at the data sink.

Simulator time

The simulator time is reset to 0 at power up. Another way to set the simulator time is through the GUI: in the "Output signal and network" panel, click once on the "Set Date/Time" button to transfer the PC current date and time to the simulator.



Frequency profile table

A dynamic Doppler profile can be enacted by loading a time-tagged table to the simulator.

The table is entered in one TCP session whereby the user (TCP client) opens a TCP connection to port 1024 and writes the entire frequency table. The table consists of a 64-bit start time (same reference as the SDDS time tag, i.e. 250ps units) followed by up to 4096 32-bit frequency samples.
Each sample represents a nominal center frequency expressed in units of 160 MHz / 2^{32} (about 37 mHz steps), sampled at 1s intervals.

The byte order is MSB first.

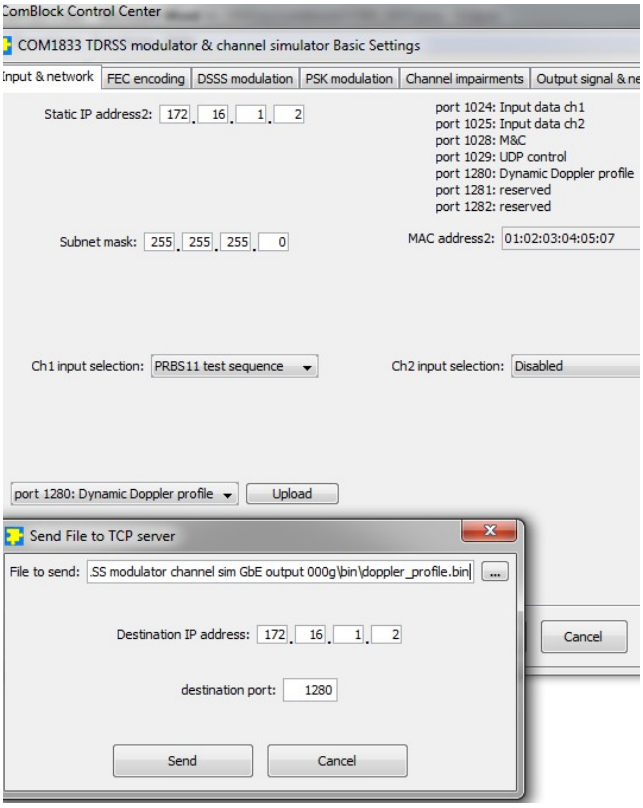
The frequency table is read (played-back) every second starting at the specified start time. The receiver interpolates linearly 64x between successive 1s samples so as to minimize discontinuities. This ensures phase and frequency

continuity. The modulator samples undergo frequency translation using this frequency bias.

Table playback is mutually exclusive with table upload. Opening a new TCP session to upload a new table will immediately stop any playback in progress.

Because the table is quite small (131Kbits max), the TCP upload time (2-5ms) is insignificant relative to the playback duration.

A utility is included in the ComBlock Control Center to upload a binary frequency profile table:

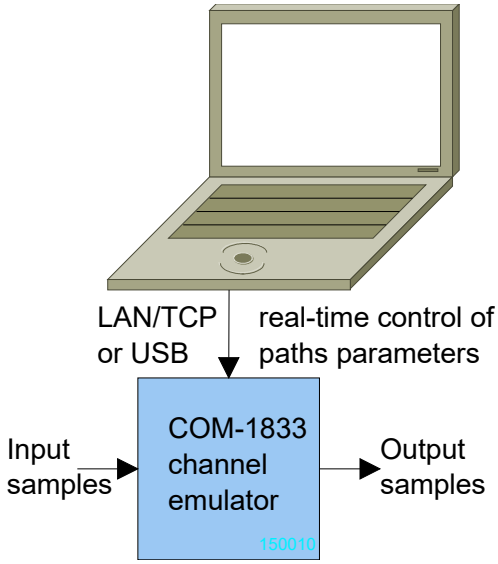


Multi-path simulator

The multi-path section of the simulator can be operated in either **auto** or **manual** mode.

In auto mode, the multi-path parameters are statistical variables generated automatically (as a one-time or periodic random draws) by the ComBlock Control Center. The random variables are drawn on the basis of user-supplied system-level parameters such as maximum Doppler, delay spread, indirect path mean amplitude, etc.

In manual mode, users can program each path parameter (delay, phase rotation, frequency offset, amplitude scaling coefficient) by running a custom program on the host computer and communicating in real-time over a LAN/TCP or USB connection. (see the code template in CD-ROM).



Short-Term Fading

The short-term fluctuation in signal amplitude is due to multi-path signals adding coherently in a constructive or destructive way. Even small changes in distance of the order of the wavelength can cause significant changes in amplitude at the receiver.

In essence, the COM-1524 is a real-time implementation of the following general multi-path equation:

$$w(t) = \sum_{k=1}^{N} \alpha_k . z(t - \tau_k) . e^{-j2\pi(f_m \cos\psi_k + \varphi_k)t}$$

where
z(t) is the complex transmitted signal,
w(t) is the complex received signal,
N the number of paths,
α_k the k^{th} path amplitude,
τ_k the k^{th} path delay,
ψ_k the angle of incidence of the k^{th} received path with respect to the receiver motion,
φ_k an initial phase condition for the k^{th} path,
f_m the maximum Doppler frequency offset.

The user-specified parameters are

(a) The maximum Doppler frequency f_m, which is related to the transmitted radio frequency f_0 and the speed v of the receiver relative to the transmitter

$$f_m(Hz) = v(m/s).\frac{f_0(MHz)}{300}$$

(b) The delay spread Δ_τ, a function of the environment type: in-building, open area, suburban area, urban area, etc.

(c) The mean path amplitude.

α_k, τ_k , ψ_k , φ_k are random variables. For simplicity, these random variables are modeled as independent.

The delay spread τ_k is modeled as an exponential distribution with a probability density function expressed as

$$f(\tau) = \frac{1}{\Delta_\tau}.e^{-\tau/\Delta_\tau}$$

where
Δ_τ is the delay spread standard deviation, as specified by the user. Physically, this distribution expresses the fact that most of the multi-path signals are grouped just after the earliest received signal. Signal with large delays are seldom received.

The initial phase condition φ_k is modeled as uniformly distributed over [0, 2π[.

The angle of incidence ψ_k is also modeled as uniformly distributed over [0, 2π[.

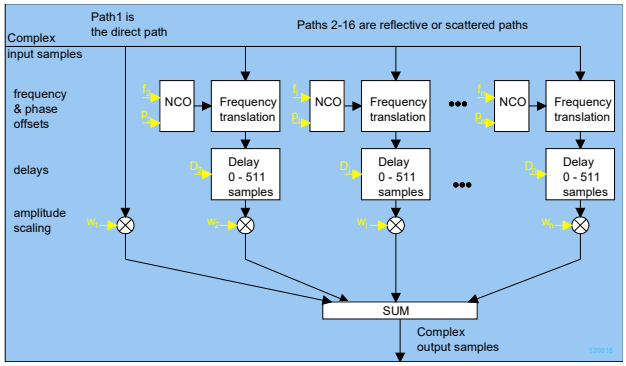
The path amplitude α_k is also modeled as an exponential distribution.

In the case when there exists a line-of-sight component (**Rician Fading**), the path index 0 represents the direct path between transmitter and receiver. The strength of the direct component $\alpha_0 = k_d$ is user-specified. To disable the LOS path, set k_d to zero.

When Rician Fading is enabled, the direct path parameters (delay τ_0, the angle of incidence ψ_0 and the initial phase offset φ_0) are set to zero.

Multi-path implementation

The modulated samples are subjected to a 16-path multi-path simulation prior to adding thermal noise. The implementation is illustrated below:



Path 1 is the direct path, and as such represents the reference against which the other paths are described in terms of relative delay and relative frequency offset. The path 1 gain can be set to zero to simulate the absence of line of sight.

The path parameters are random variables that are generated either by the GUI or by custom user-code writing control registers REG103 through REG112.

AWGN Algorithm

The Box-Muller algorithm is used to transform a uniformly distributed random variable to a Gaussian-distribution random variable. A description of the algorithm, together with an elegant FPGA implementation method can be found in reference [1].

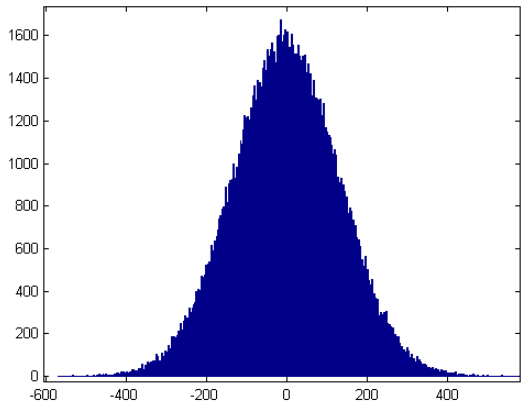
The MATLAB program below illustrates how the algorithm works:

```
% Box Muller algorithm verification
nsamples = 1000000;

% generate two independent uniform
distributed random variables
x1 = rand(nsamples,1);
x2 = rand(nsamples,1);

% transform the distributions
```

```
f = sqrt(-log(x1));
g = sqrt(2.0)*cos(2*pi*x2);

%gaussian distribution
n = f.*g;

% plot histogram
hist(n,500)

% standard deviation is 1.0
std(n)

% mean is zero
mean(n)
```

[1] "Efficient FPGA Implementation of Gaussian Noise Generator for Communication Channel Emulation". Jean-Luc Danger, Adel Ghazel, Emmanual Boutillon, Hedi Laamari. 2002.

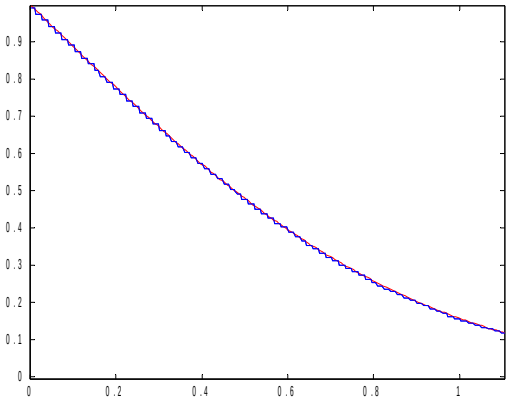
The resulting noise sample distribution is shown below:



Noise sample histogram (130K samples)

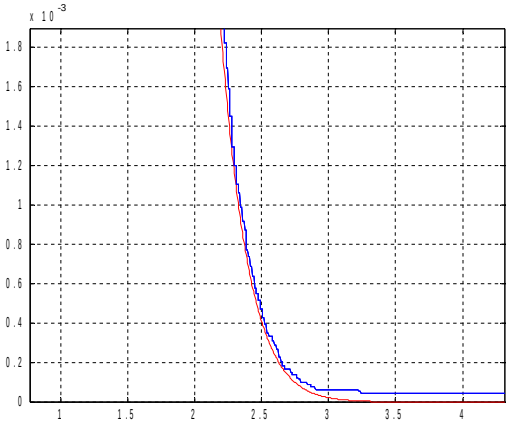
Mean = 0.
Standard deviation = 128

The plots below illustrate how accurate the noise generation is, by comparing the erfc function (red) with the AWGN normalized distribution (blue)



Theoretical erfc function (red) vs actual AWGN normalized distribution measurements (blue). Range 0 – 1, 130K samples.

The theoretical curve and the measured statistical distribution of noise samples are nearly superposed.

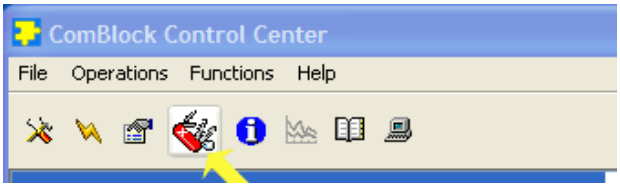


Theoretical erfc function (red) vs actual AWGN normalized distribution measurements (blue). Range 1-4, 130K samples.

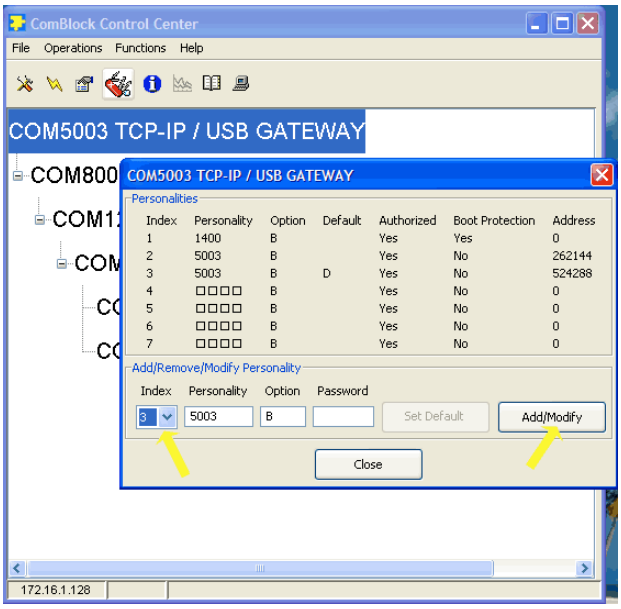
Load Software Updates

From time to time, ComBlock software updates are released.

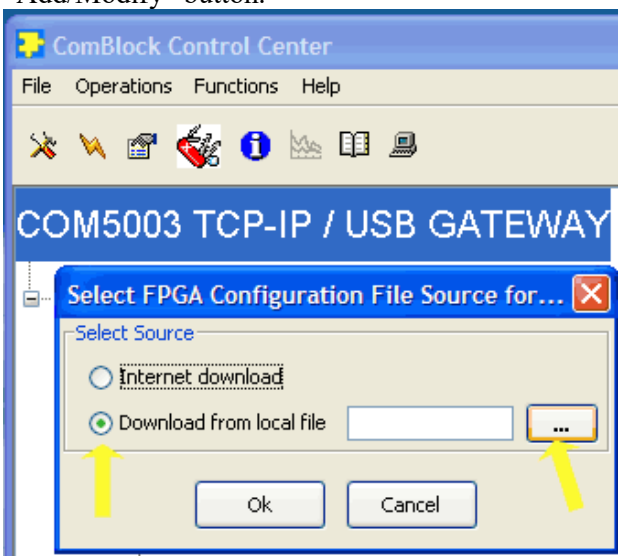
To manually update the software, highlight the ComBlock and click on the Swiss army knife button.



The receiver can store multiple personalities. The list of personalities stored within the ComBlock Flash memory will be shown upon clicking on the Swiss army knife button.



The default personality loaded at power up or after a reboot is identified by a 'D' in the Default column. Any unprotected personality can be updated while the Default personality is running. Select the personality index and click on the "Add/Modify" button.



The software configuration files are named with the .bit extension. The bit file can be downloaded via the Internet, from the ComBlock CD or any other local file.

The option and revision for the software currently running within the FPGA are listed at the bottom of the advanced settings window.

Two firmware options are available for this receiver:
-A firmware uses an internal VCTCXO frequency reference.
-B firmware option requires an external 10 MHz frequency reference.

Recovery

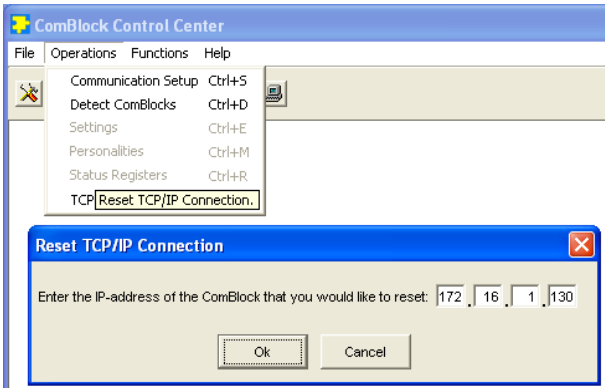
This module is protected against corruption by an invalid FPGA configuration file (during firmware upgrade for example) or an invalid user configuration. To recover from such occurrence, connect a jumper in J3 and during power-up. This prevents the FPGA configuration and restore USB communication [LAN communication is restored only if the IP address is known/defined for the personality index selected as default]. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

UDP Reset

Port 1029 is open as a UDP receive-only port. This port serves a single purpose: being able to reset the modem (and therefore the TCP-IP connection) gracefully. This feature is intended to remedy a common practical problem: it is a common occurrence for one side of a TCP-IP connection to end abnormally without the other side knowing that the connection is broken (for example when a client 'crashes'). In this case, new connections cannot be established without first closing the previous ones. The problem is particularly acute when the COM-1833 is at a remote location.

The command "@001RST<CR><LF>" sent as a UDP packet to this port will reset all TCP-IP connections within the COM-1833.

TCP-IP connections can also be cleared remotely from the ComBlock Control Center as illustrated below:



Troubleshooting Checklist

Device is not responsive after power up:

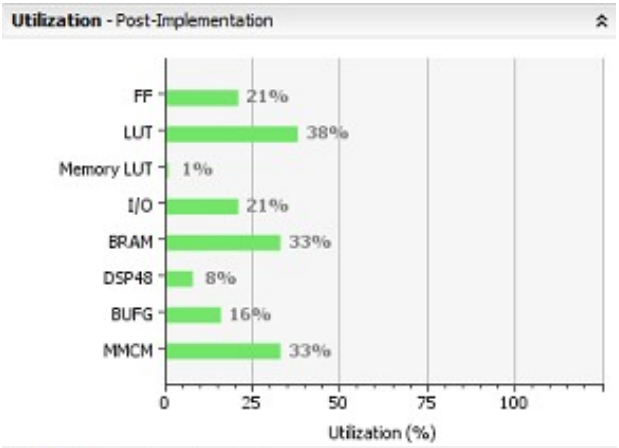
- The device typically takes up to 30 seconds to boot up after power up.
- If still not responsive after 30 seconds, recycle the power. Wait at least 15 seconds after power off to turn the power on again.

Device does not communicate with the ComBlock Control Center:

- Make sure an external 10 MHz frequency reference is present prior to powering up the receiver. This applies only when the –B firmware option (external 10 MHz frequency reference) is selected by default.

FPGA occupied space

The current VHDL code uses less than half the FPGA resources (XCA7A100T) as shown below:



Utilization - Post-Implementation

Resource	Utilization	Available	Utilization %
FF	26062	126800	20.55
LUT	24375	63400	38.45
Memory LUT	127	19000	0.67
I/O	60	285	21.05
BRAM	44	135	32.59
DSP48	18	240	7.50
BUFG	5	32	15.62
MMCM	2	6	33.33

Configuration Management

This specification is to be used in conjunction with VHDL software revision 0 and ComBlock control center revision 3.10h and above.

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1833 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

Reference Documents

[1] Space Network Interoperable PN Code Libraries 451-PN CODE-SNIP

ComBlock Ordering Information

COM-1833 TDRSS modulator & channel simulator

Configuration options:

- LAN/TCP server input, GbE SDDS/VITA-49 output
- RS-422 and LAN/TCP server inputs, RF output.

ECCN: 5A001.b.3

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