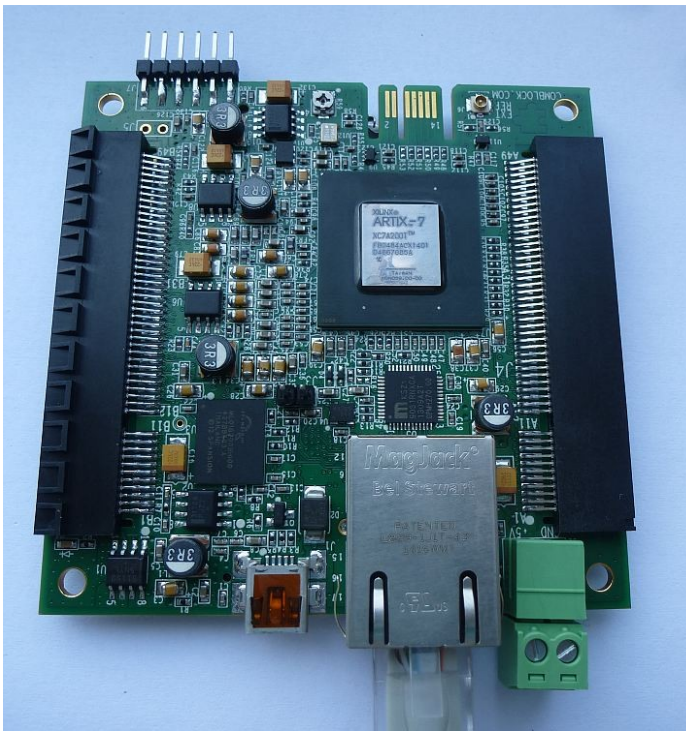
COM-1831 BURST MODE DSSS MODEM 80 Mchip/s

Key Features

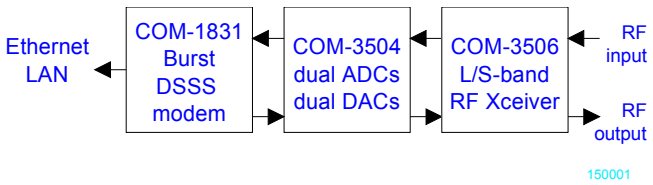
- Direct-Sequence Spread-Spectrum (DSSS) burst modulator/demodulator
- Burst mode operation:
  - fixed-length 512-bit data frames from/to LAN/UDP ports
  - Multiple frames transmitted efficiently with only 32-symbol separation.
- Acquisition: 1600-symbol preamble with no apriori knowledge of arrival time
- Large frequency acquisition range: ±(chip_rate / 64) or (1.8*symbol_rate), whichever is smaller, with no apriori knowedge.
- End-to-end latency: 2672 symbol / modulation symbol rate. For example 1.2ms at 2.5Msymbols/s.
- Programmable chip rate, up to 79.5 Mchips/s (limited by FPGA technology XC7A100T-1)
- 2047-chip Gold codes
- Data rate practical range from chip_rate/2047 to chip_rate/30
- Built-in tools: PRBS-11 pseudo-random test sequence, BER tester, AWGN generator, internal loopback mode.
- Monitoring:
  - Carrier frequency error
  - SNR
  - BER
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3.5” module for ease of prototyping. Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.



For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com1831.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

Typical assembly



MSS • 845 Quince Orchard Boulevard Ste N • Gaithersburg, Maryland 20878-1676 • U.S.A.
Telephone: (240) 631-1111 Facsimile: (240) 631-1676 www.ComBlock.com
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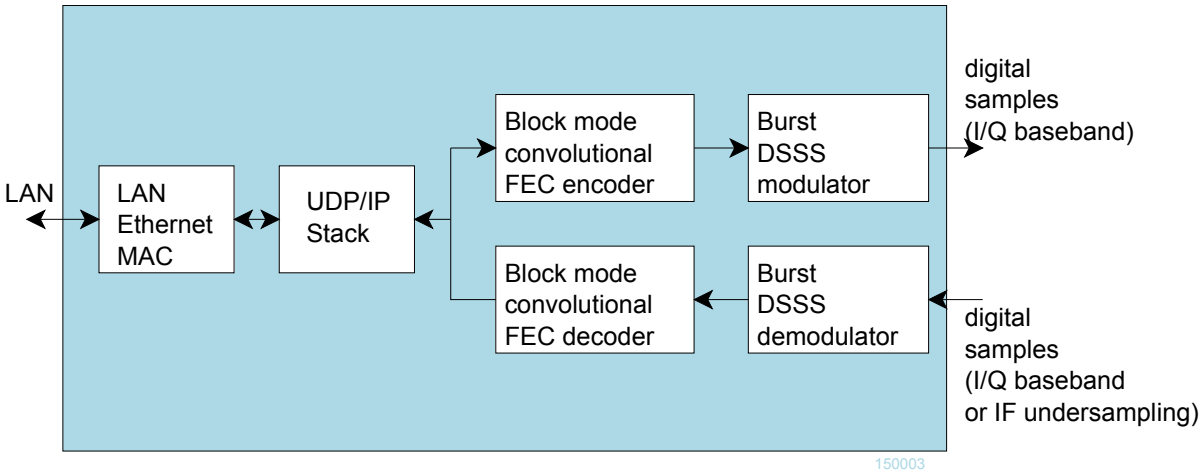
Block Diagram



Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

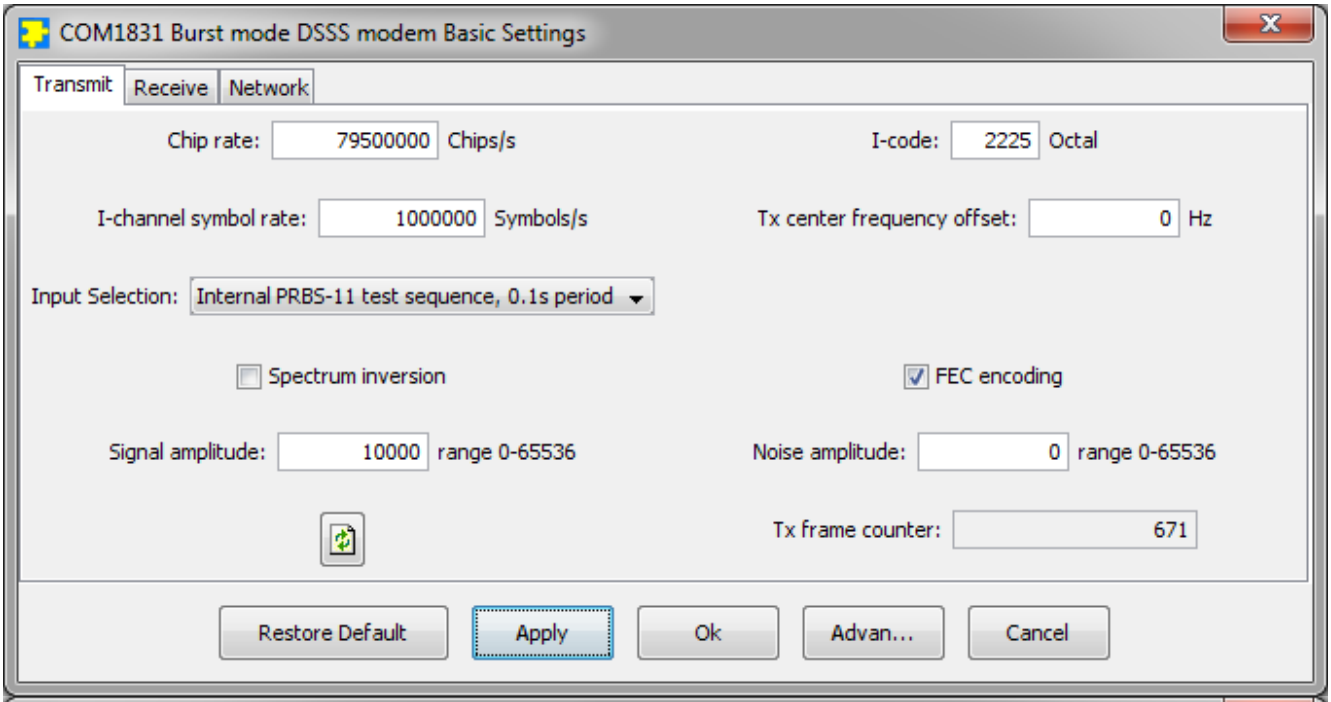
- USB, TCP-IP/LAN

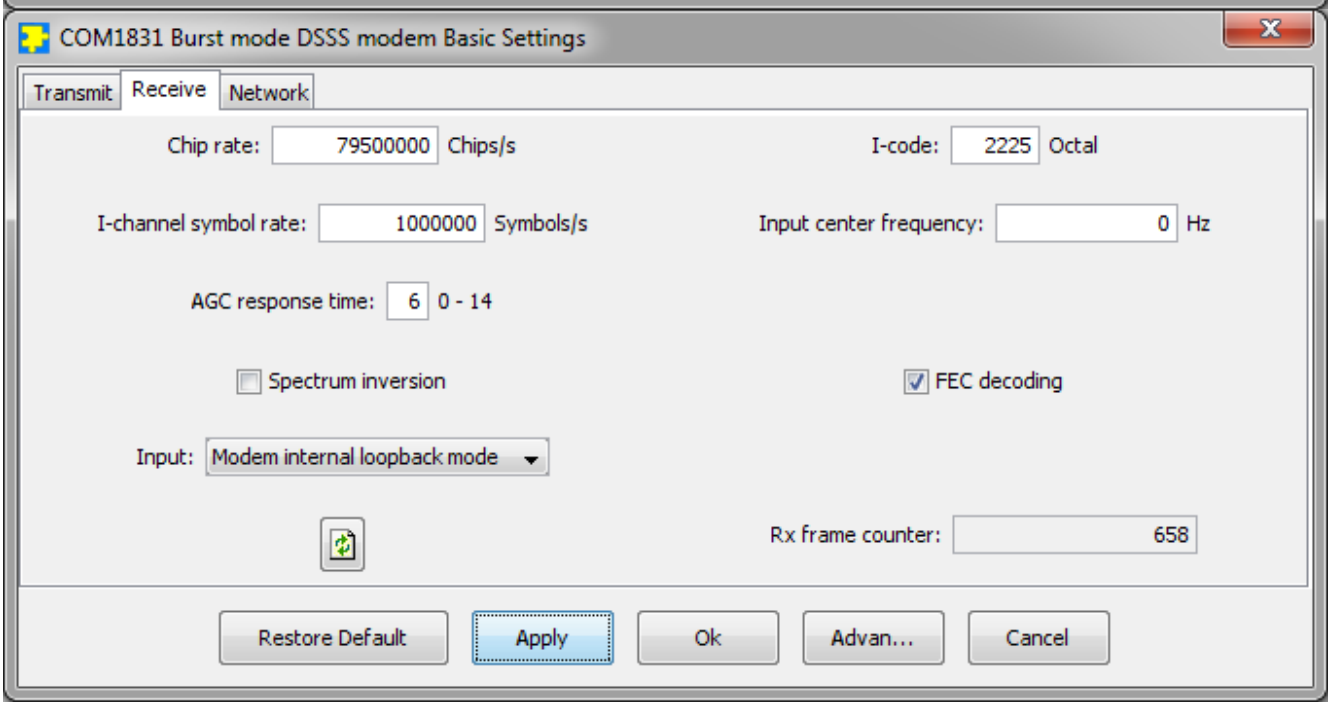
or connections via adjacent ComBlocks

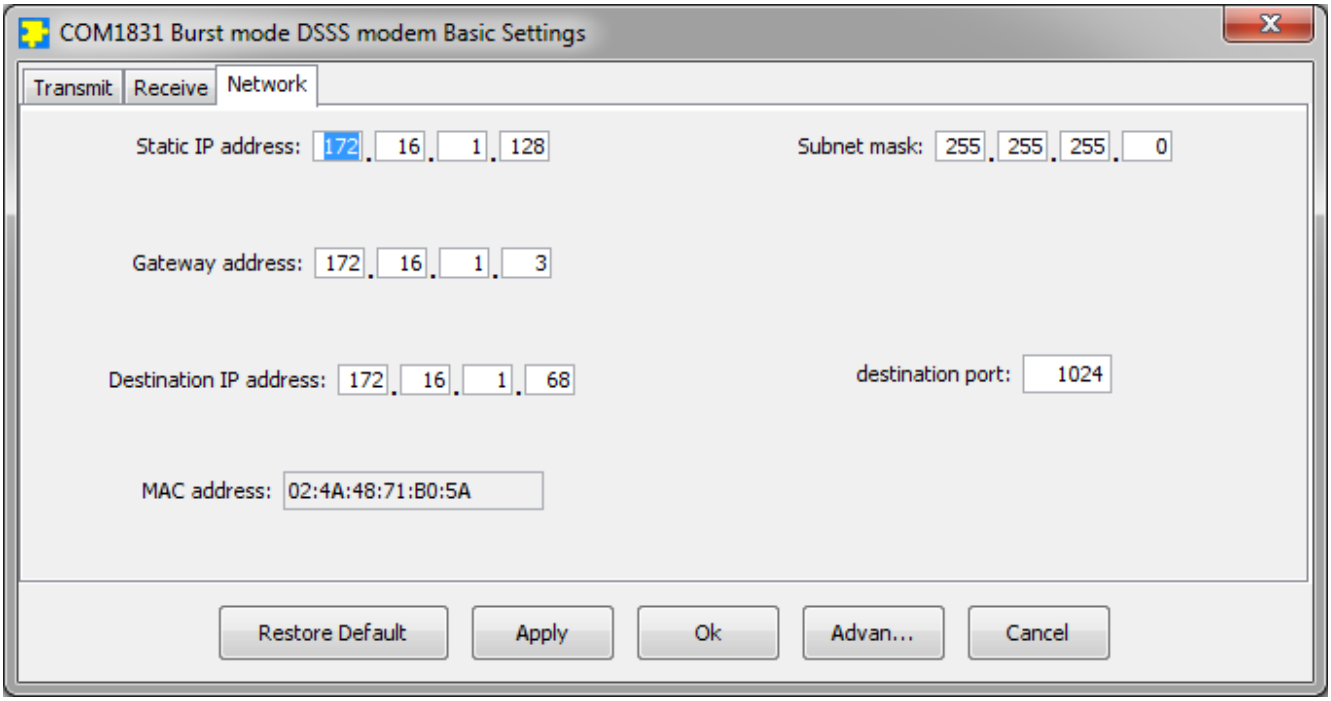
The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1831 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1831 module to be configured, next click the *Settings* button to display the *Settings* window shown below.


COM1831 Burst mode DSSS modem Basic Settings
Transmit
Receive
Network
Chip rate: 79500000 Chips/s
I-code: 2225 Octal
I-channel symbol rate: 1000000 Symbols/s
Tx center frequency offset: 0 Hz
Input Selection: Internal PRBS-11 test sequence, 0.1s period
Spectrum inversion
FEC encoding
Signal amplitude: 10000 range 0-65536
Noise amplitude: 0 range 0-65536
Tx frame counter: 671
Restore Default
Apply
Ok
Advan...
Cancel


COM1831 Burst mode DSSS modem Basic Settings
Transmit
Receive
Network
Chip rate: 79500000 Chips/s
I-code: 2225 Octal
I-channel symbol rate: 1000000 Symbols/s
Input center frequency: 0 Hz
AGC response time: 6 0 - 14
Spectrum inversion
FEC decoding
Input: Modem internal loopback mode
Rx frame counter: 658
Restore Default
Apply
Ok
Advan...
Cancel



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Several key parameters are computed on the basis of the 160 MHz ADC clock f_{clk_adc} or the 120 MHz internal processing clock f_{clk_p}.

Modulator	
Parameters	**Configuration**
Reserved	REG0
Processing clock f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock. Expressed as as $f_{clk\_tx} = f_{clk\_p} * M / (D * O))$ where D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 1.0. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 1.0. Fixed point format 7.3
	Note: the graphical use interface computes the best values for M, D and O. f_{clk_tx} recommended range 80-160 MHz. REG1(6:0) = D REG2 = M(7:0) REG3(1:0) = M(9:8) REG4 = O(7:0) REG5(2:0) = O(10:8)
Chip rate $f_{chip\_rate\_tx}$	The modulator chip rate is in the form $f_{chip\_rate\_tx} = f_{clk\_tx} / 2^n$ where n ranges from 1 (2 samples per chip) to 15 (chip rate = f_{clk_tx} / 32768). n is defined in REG6(3:0)
I Code	Linear feedback shift register initialization. As per [1] REG7 LSB REG8(2:0) MSb
Q Code	REG9 LSB REG10(2:0) MSb
Reserved	REG11-REG14

I channel symbol rate $f_{symbol\_rate\_i}$	The I-channel symbol rate can be set independently of the spreading code period as $f_{symbol\_rate} * 2^{32} / f_{clk\_tx}$ Ignored when spreading is disabled (the symbol rate is then defined by the chip rate field) REG15 (LSB) – REG18 (MSB)
Q channel symbol rate $f_{symbol\_rate\_q}$	The Q-channel symbol rate can be set independently of the spreading code period as $f_{symbol\_rate} * 2^{32} / f_{clk\_tx}$ REG19 (LSB) – REG22 (MSB)
Output center frequency (f_c)	The modulated signal center frequency can be shifted in frequency 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk\_tx}$ REG23 (LSB) – REG26 (MSB)
Digital Signal gain	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected chip rate. Please check for saturation (see test points) when changing either the chip rate or the signal gain. REG27 = LSB REG28 = MSB
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation (see test points) when changing this parameter. REG29 = LSB REG30 = MSB
Input selection	0 = from UDP port 1024 1 = internal pseudo-random test sequence. 100ms repetition 2 = internal pseudo-random test sequence continuous transmission 3 = unmodulated test mode (carrier only) REG31(1:0)
FEC encoding	K=9 rate ½ convolutional code with zero tail bits. 1 = enabled 0 = bypassed REG31(2)

Spectrum inversion	Invert Q bit 0 = off 1 = on REG31(3)
BPSK / SQPN	0 = BPSK 1 = SQPN REG31(4) Future feature. BPSK baseline
Spreading	0 = spreading disabled The symbol rate is defined as $f_{chip\_rate\_tx}$ The symbol rate field is ignored. 1 = spreading enabled REG31(5)
External transmitter gain control	When using an external transceiver such as the COM-350x family, the transmitter gain can be controlled through the TX_GAIN_CNTRL1 analog output signal. Range 0 – 3.3V. REG32: LSB, REG33(3:0): MSb
TX_ENB control	The TX_ENB signal at the interface controls the RF transmit circuit. During normal operations, the transmitter and ancillary circuits (RF LO) are muted outside of a transmit burst. REG33(4) = 0 However, during tests, the transmitter can be forced to stay ON at all times, for example when the AWGN is generated within. REG33(4) = 1

Demodulator	
Parameters	**Configuration**
Nominal chip rate $f_{chip\_rate\_rx}$	32-bit integer expressed as $f_{chip\_rate\_rx} * 2^{32} / f_{clk\_adc}$. The maximum practical chip rate is f_{clk_adc} /2. The maximum allowed error between transmitted and received chip rate is +/- 100ppm. REG35 = bits 7-0 (LSB) REG36 = bits 15 – 8 REG37 = bits 23 – 16 REG38 = bits 31 – 24 (MSB)
I Code	Linear feedback shift register A initialization. REG39 LSB REG40(2:0) MSb
Q Code	Linear feedback shift register C REG41 LSB REG42(2:0) MSb
CIC_R	Receiver decimation factor from f_{clk_adc} to 4* $f_{chip\_rate\_rx}$. Valid range 1 - 16384 REG43 LSB REG44 MSB
Reserved	REG45-REG46
Nominal I channel symbol rate $f_{symbol\_rate\_i}$	Nominal I-channel symbol rate, defined as $f_{symbol\_rate\_i} * 2^{32} / f_{clk\_adc}$ REG47 (LSB) – REG50 (MSB)
Nominal Q channel symbol rate $f_{symbol\_rate\_q}$	Nominal Q-channel symbol rate, defined as $f_{symbol\_rate\_q} * 2^{32} / f_{clk\_adc}$ REG51 (LSB) – REG54 (MSB)
I channel spreading factor (Processing gain)	Approximate (i.e rounded) ratio of chip rate / symbol rate Range: 3 – 2047 Note: to effectively achieve this processing gain, the code period must be longer than one symbol duration. REG55 (LSB) REG56(4:0) MSb
Q channel spreading factor (Processing gain)	Approximate (i.e rounded) ratio of chip rate / symbol rate REG57 (LSB) REG58(4:0) MSb
Nominal input center frequency (f_c)	The nominal center frequency is a fixed frequency offset applied to the input samples. It is used for fine frequency corrections, for example to correct clock drifts. 32-bit signed integer (2's complement representation) expressed as

	$f_c * 2^{32} / f_{clk\_adc}$ In addition to this fixed value, an optional time-dependent frequency profile can be entered. See frequency profile table. REG59 (LSB) – REG62 (MSB)
Reserved	REG63
Spectrum inversion	Invert Q bit 0 = off 1 = on REG64(0)
BPSK / SQPN	0 = BPSK 1 = SQPN Future feature. BPSK baseline. REG64(1)
Despreading	0 = despreading disabled The symbol rate is defined as $f_{chip\_rate\_rx}$ The symbol rate field is ignored. 1 = enabled REG65(3)
FEC decoding enabled	K=9 rate ½ Viterbi decoding '1' enabled, '0' bypassed REG65(1)
AGC response time	Users can to optimize AGC response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and chip rate). The AGC_DAC gain control signal is updated as follows 0 = every chip, 1 = every 2 input chips, 2 = every 4 input chips, 3 = every 8 input chips, etc…. 10 = every 1000 input chips. Valid range 0 to 14. REG66(4:0)
Demod input selection	0 = baseband input (I/Q complex samples) 1 = IF input (I as real input, Q is ignored) 7 = internal loopback REG66(7:5)
BERT measurement window	The Bit Error Rate Tester counts the number of bit errors over the window defined below: 000 = 1,000 bytes 001 = 10,000 bytes 010 = 100,000 bytes 011 = 1,000,000 bytes 100 = 10,000,000 bytes 101 = 100,000,000 bytes 110 = 1,000,000,000 bytes REG67(2:0)

Network Interface	
Parameters	**Configuration**
LAN MAC address LSB	REG70. To ensure uniqueness of MAC address. The MAC address most significant bytes are tied to the FPGA DNA ID. However, since Xilinx cannot guarantee the DNA ID uniqueness, this register can be set at the time of manufacturing to ensure uniqueness.
Static IP address	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 REG71: MSB REG72 REG73 REG74: LSB
Subnet mask	REG75 (MSB) – REG78(LSB)
Gateway IP address	REG79 (MSB) – REG82(LSB)
Destination IP address	4-byte IPv4 address Destination IP address for UDP frames with decoded data. REG83 (MSB) – REG86(LSB)
Destination ports	I-channel data is routed to this user-defined port number: REG87(LSB) – REG88(MSB) Q-channel data is routed to the incremented port number.

(Re-)Writing to the last control register REG99 is recommended after a configuration change to enact the change.

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-9 Properly operating hardware will result in the following sequence being displayed: 01 F1 1D xx 1F 93 10 00 22 07.
FEC decoder input BER measurement	The burst-mode FEC decoder computes the input BER prior to decoding. Mesasured in a frame. This method works with any bit sequence. SREG16 (LSB) - SREG18 (MSB)
BER tester synchronized	SREG19(0): 1 when the BERT is synchronized with the received PRBS-11 test sequence.
Bit error rate	Monitors the BER (number of bit errors over the BERT measurement window) when the modulator is sending a PRBS-11 test sequence. The BERT measurement window size is defined in CREG67. SREG20 (LSB) – 22 (MSB)
Number of transmitted frames	SREG23 (LSB) – 25 (MSB)
Number of received frames	SREG26 (LSB) – 28 (MSB)
Number of parallel code acquisition circuits	The number of parallel code acquisition circuits is expressed as NACQ = NACQ_DIV * NMUX SREG29: NACQ_DIV SREG30: NMUX
Non-coherent integration and dump period N_NCID	SREG31
Measured modulated signal power	SREG32(LSB) SREG33 SREG34(MSB)
Measured AWGN power	Approximation: noise power is uniform over a range of +/- f_{clk_tx} /2 Therefore, the noise density depends on the selected modulator chip rate (see f_{clk_tx} equation above) SREG35(LSB) SREG36 SREG37(MSB)
AGC	Front-end AGC gain settings. 12-bit unsigned. Inverted (0 for maximum gain) SREG38 (LSB) SREG39(3:0) (MSB)
Carrier frequency offset1	Residual frequency offset with respect to the nominal carrier frequency (i.e. after frequency profile correction). Part 1/2. 32-bit signed integer expressed as fcerror * * 2^{32} / f_{clk_p} SREG40 (LSB) – SREG43 (MSB)
Carrier frequency offset2	Residual frequency offset with respect to the nominal carrier frequency (i.e. after frequency profile correction). Part 2/2. 32-bit signed integer expressed as fcerror * * 2^{31} / f_{chip_rate} SREG44 (LSB) – SREG47 (MSB)
SNR	2*(S+N)/N ratio, valid only during code lock. Linear (not in dBs) Fixed point format 14.2 SREG48 (LSB) – SREG49 (MSB)
TCP-IP Connection Monitoring	
Parameters	**Monitoring**
LAN PHY ID	Expect 0x22 when LAN adapter is plugged in. SREG7
MAC address	Unique 48-bit hardware address (802.3). In the form SREG10:SREG11:SREG12:…:SREG15

Multi-byte status variables are latched upon (re-)reading SREG7.

ComScope Monitoring

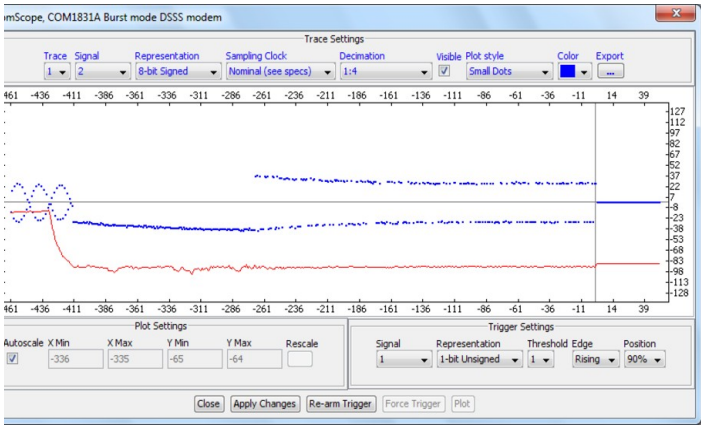
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. Click on the button to start, then select the signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: I-channel spread input, directly from ADC (could be at IF)	8-bit signed	ADC clock f_{clk_adc}	512
2: Demodulated I-channel	8-bit signed	1 sample / I-symbol	512
3: FFT magnitude	8-bit unsigned	ADC clock f_{clk_adc}	512
4: Carrier tracking phase	8-bit signed	ADC clock f_{clk_adc}	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: I-channel spread input at near-zero center frequency	8-bit signed	ADC clock f_{clk_adc}	512
2: Code replica. Compare with spread input signals	8-bit signed	2 samples/chip	512
3: last demod AGC gain (I-channel)	8-bit unsigned	1 sample / symbol	512
4: Symbol tracking phase (accumulated)	8-bit signed	1 sample / symbol	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: I-channel after FFT frequency correction, resampling and channel LPF	8-bit signed	2 samples / chip	512
2: Demodulated Q-channel	8-bit signed	1 sample / Q-symbol	512
3: Code tracking phase correction (accumulated)	8-bit signed	2 samples / symbol	512
4: 2(S+N)/N after despreading. Valid only if code is locked. Linear (i.e. not in dBs)	8-bit unsigned	Symbol rate / 2.5	512
Trigger Signal	**Format**		
1: End of demodulated burst	Binary		
2: Missed burst detection (at end of expected burst)			
3. Demod sync word detection	Binary		

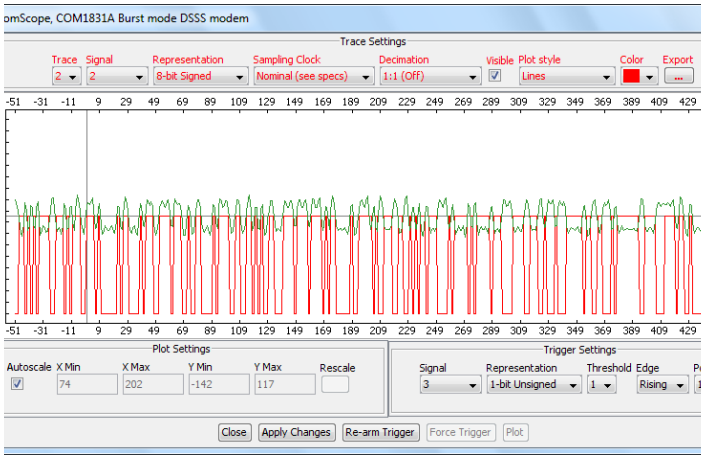
Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk_adc} demod clock as real-time sampling clock.

In particular, selecting the f_{clk_adc} demod clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope example, showing trace1 signal2 (in blue): demodulated I-bits during preamble (left) then data (right half). Trace2 signal 4 (in red) shows the I-symbol tracking phase.



ComScope example, showing code lock with aligned: received spread signal after RRC filter (green) vs code replica (red)

Digital Test Points

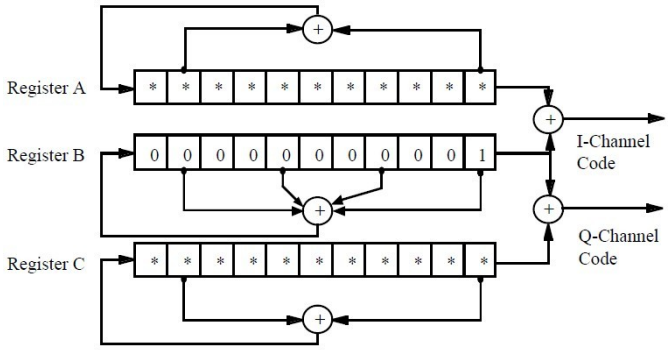
Test Point	Definition
J4/A1	Transmit frame boundaries (0 = idle)
J4/A2	Modulator saturation
J4/A3	Demod code lock
J4/A4	Demod signal presence detected at FFT
J4/A5	Demodulator recovered carrier/center frequency (coarse)
J4/A6	Demod recovered carrier/center frequency (fine)
J4/A7	Demod data field(s) [demod state = 3]
J4/A8	Start of spreading code replica (compare with start of spreading code at the modulator)
J4/A9	Demod start of I code replica
J4/A10	Demod input I channel MSB (compare with replica)
J4/A11	Demodulated I bit
J4/A12	Demod sync word detection
J4/A13	Missed burst detection
J4/A14	Demod state 0
J4/A15	Demod state 1
J4/A16	Demod state 2
J4/A17	Demod state 3
J4/B1	FEC decoder input bit error
J4/B2	BER tester synchronized
J4/B3	BER tester matched filter output (detects start of PRBS11 sequence)
J4/B4	Byte error detected by BER tester

Operation

Spreading codes

Each burst undergoes spectrum spreading with user-selected pseudo-random codes. All fields (preambles, sync word, data) are spread.

Spreading codes are user-selected among a group of 2047-period Gold codes, irrespective of the symbol rate. The codes are selected by their 11-bit A and C registers initialization.



Note
Stage contents indicate initial conditions
* indicates user-unique initial conditions

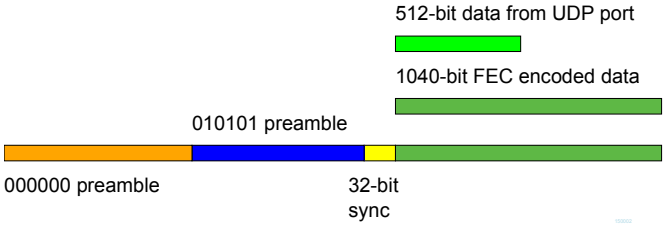
Burst format

The modulator input consists of a 512-bit fixed-length payload data frame received over LAN/UDP.

The payload data frame is encoded with a convolutional code K=9, rate ½, resulting in an encoded frame of length 1040 bits (including the 16 tail bits).

When transmitting a single frame, the frame is encapsulated in a spread-spectrum burst comprising four distinct fields:

- no data preamble
- toggling bits preamble
- 32-bit synchronization field
- 1040-bit encoded payload field



When transmitting multiple frames, follow-on frames are appended without preamble, separated only with a 32-bit sync word.

Transmission timing

A data frame received over UDP is transmitted without delay. The transmission time uncertainty is small (< TBD us). The user application is therefore fully in control of the burst scheduling, for example to prevent collisions in a multi-node network.

When the modulator is configured in PRBS11 test mode, the PRBS11 pseudo-random test sequence is generated internally, packetized in 512-bit frame and transmitted one frame every 100 ms. The UDP input is ignored while in this mode.

Input elastic buffer

When more than 512 bits of payload data is needed, multiple data frames can be queued for transmission in the elastic buffer. The modulator expects any follow-on frame to be entirely within the input elastic buffer before the previous frame transmission is complete (so as to avoid transmissing another long preamble). In this case, the modulator only inserts a 32-bit synchronization word between payload frames.

The input elastic buffer size is 8Kbit, large enough for 7 encoded frames.

Symbol rate

The symbol rate refers to the coded stream. The symbol rate can be set independently of the chip rate and code period. The demodulator includes an autonomous symbol tracking loop, separate from the code tracking loop.

Frequency acquisition & tracking

The frequency acquisition range depends on the chip rate, as defined by
±Chip_rate / 64
For example, in the case of a 35Mchips/s burst, the frequency acquisition range is ±545 KHz.

Once locked, the carrier tracking loops tracks the carrier phase over a very wide frequency range.

Modulation

Baseline: BPSK spread with I-channel code. Possible future extension: SQPN (I and Q channels spread with staggered I and Q code, Q-channel symbol rate = I-channel symbol rate / N, where N is an integer.

Code Acquisition

NACQ parallel detectors search for code aligment during the code acquisition phase. During the subsequent code tracking phase, 3 detectors track the early/center/late code while the other NACQ-3 detectors scan for false lock. The detectors are staggered ½ chip apart.

To further minimize the latency, the NACQ parallel detectors are organized into NMUX banks of NACQ_DIV detectors. NACQ = NMUX*NACQ_DIV.

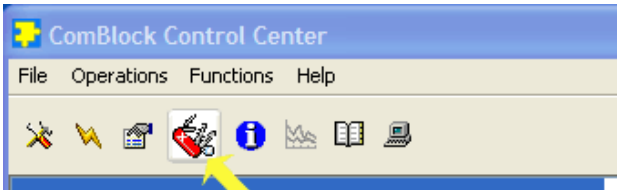
Detection is performed in two steps: first a coherent detector averages the despread signal over ½ a symbol period. The result is squared and further averaged over N_NCID symbols.

The internal implementation parameters NACQ_DIV, NMUX and N_NCID are fixed prior to FPGA synthesis. They can be read back in status registers SREG(29), SREG(30) and SREG(31) respectively.

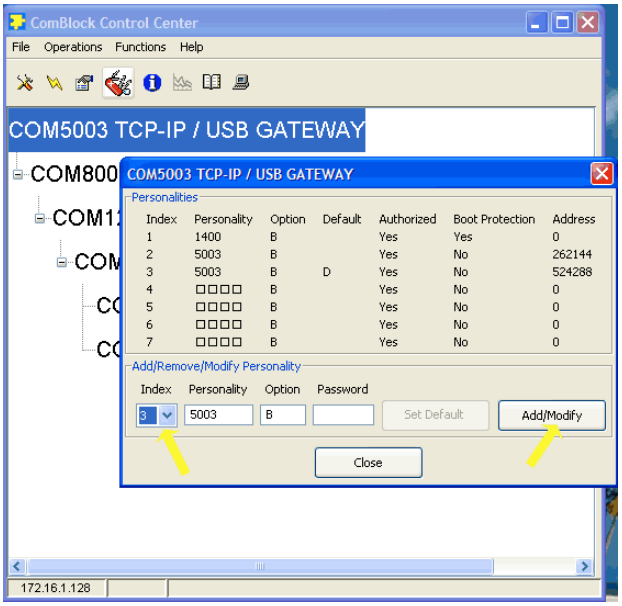
Load Software Updates

From time to time, ComBlock software updates are released.

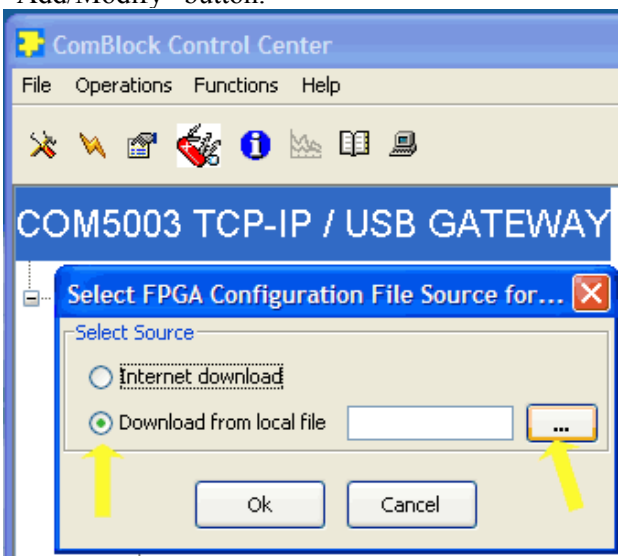
To manually update the software, highlight the ComBlock and click on the Swiss army knife button.



The receiver can store multiple personalities. The list of personalities stored within the ComBlock Flash memory will be shown upon clicking on the Swiss army knife button.



The default personality loaded at power up or after a reboot is identified by a 'D' in the Default column. Any unprotected personality can be updated while the Default personality is running. Select the personality index and click on the "Add/Modify" button.



The software configuration files are named with the .bit extension. The bit file can be downloaded via the Internet, from the ComBlock CD or any other local file.

The option and revision for the software currently running within the FPGA are listed at the bottom of the advanced settings window.

The firmware options available for this receiver are:
-A firmware uses an internal VCTCXO frequency reference. COM-3504 right connector interface.
-B firmware option requires an external 10 MHz frequency reference. COM-3504 right connector interface.
-C firmware uses an internal VCTCXO frequency reference. COM-30xx left connector interface + COM-4009 right connector interface.
-D firmware option requires an external 10 MHz frequency reference. COM-30xx left connector interface + COM-4009 right connector interface.

Recovery

This module is protected against corruption by an invalid FPGA configuration file (during firmware upgrade for example) or an invalid user configuration. To recover from such occurrence, connect a jumper in J3 and during power-up. This prevents the FPGA configuration and restore USB communication [LAN communication is restored only if the IP address is known/defined for the personality index selected as default]. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

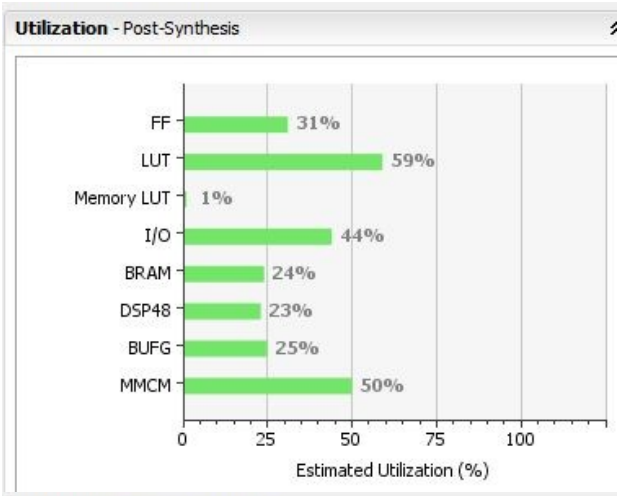
Troubleshooting Checklist

Demodulator can't achieve lock even at high signal-to-noise ratios:

- Make sure the modulator baseband I/Q signals do not saturate, as such saturation would strongly distort the modulation phase information. (this is a phase demodulator!)

VHDL code

The FPGA code is written in VHDL. It does not use any IP core or third-party software.
It occupies the following FPGA resources:



Utilization - Post-Implementation

Resource	Utilization	Available	Utilization %
FF	39284	126800	30.98
LUT	36668	63400	57.84
Memory LUT	78	19000	0.41
I/O	124	285	43.51
BRAM	32.5	135	24.07
DSP48	54	240	22.50
BUFG	7	32	21.88
MMCM	3	6	50.00

Interfaces

ADC/DAC Interface	Definition
ADC_SAMPLE_CLKOUT_P ADC_SAMPLE_CLKOUT_N	ADC sampling clock output: 160 MHz.
ADC*x*_DATA_IN[13:2]	ADC*x* digital samples input. 12-bit unsigned (also known as "offset binary") format. The two least significant bits (1:0) are unused (reserved for future use). 0x0000: lowest output level 0x3FFF: highest output level 0x1FFF or 0x2000 ≈ center level CMOS 0 – 3.3V. Read at the rising edge of ADC*x*_SAMPLE_CLK_OUT.
ADC*x*_SAMPLE_ CLK_IN	Sampling clock input. Pinpoints the center of the ADC*x*_DATA_IN bits for reclocking at the receiving end. Index *x* is 1 or 2
	CMOS 0 – 3.3V.
DAC_SAMPLE_CLKOUT_P DAC_SAMPLE_CLKOUT_N	DAC sampling clock output. Sets the DAC sampling rate. 0-3.3V LVCMOS differential signal. Depends on selected chip rate: 80-160 MHzd
DAC*x*_DATA_OUT[15:0]	DAC*x* digital samples output. 16-bit unsigned (also known as "offset binary") format. 0x0000: lowest input level 0xFFFF: highest input level 0x7FFF or 0x8000 ≈ center level CMOS 0 – 3.3V. Read at the rising edge of DAC_SAMPLE_CLK_IN
AUX_SPI[5:1]	SPI interface to control the two auxiliary DACs and ADC in real-time. See AD5621 serial 12-bit DAC specifications. See AD7276 serial 12-bit ADC specifications.

Operating input voltage range

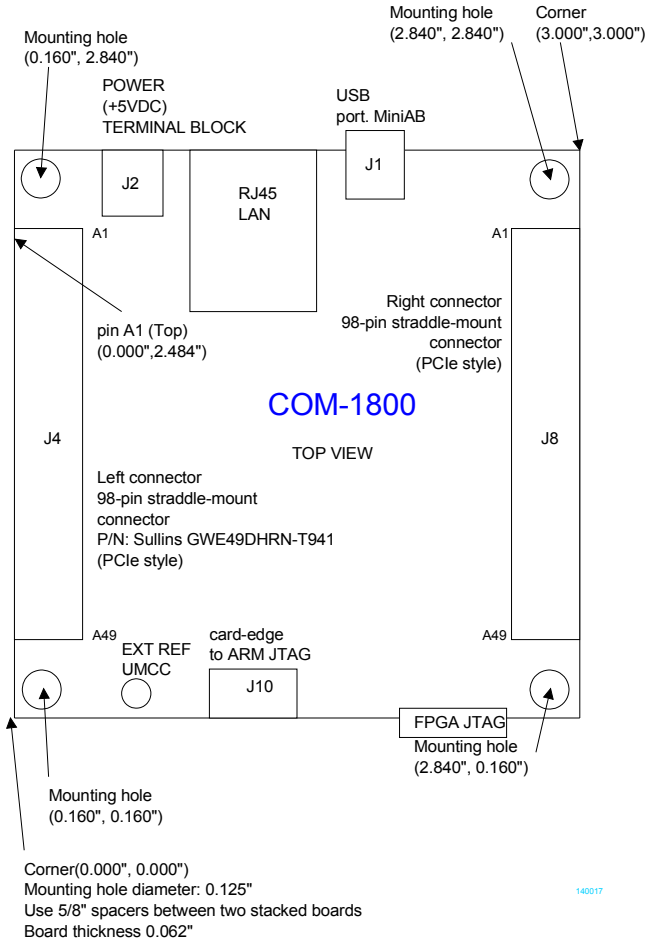
Supply voltage	+4.5V min, +12V max 650mA typ.

Absolute Maximum Ratings

Supply voltage	-0.5V min, +20V max
98-pin connector inputs	-0.5V min, +3.6V max

Important:
The I/O signals connected directly to the FPGA are NOT 5V tolerant!

Mechanical Interface



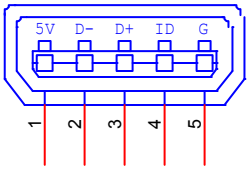
Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1800schematics.pdf

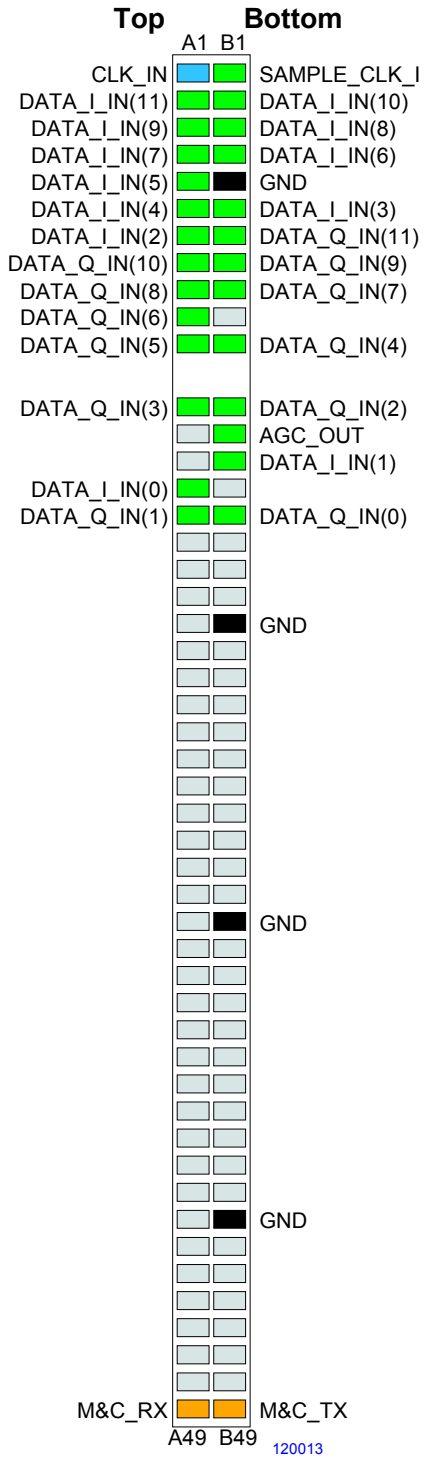
Pinout

USB

Both USB ports are equipped with mini type AB connectors. (G = GND). In both cases, the COM-1831 acts as a USB device.

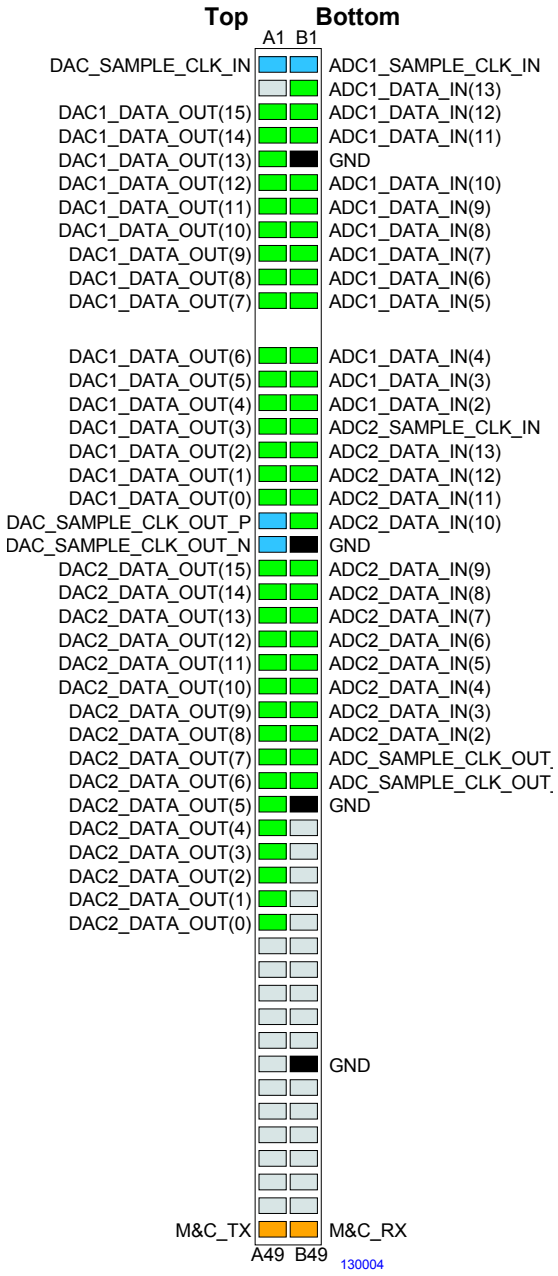


Left Connector J4



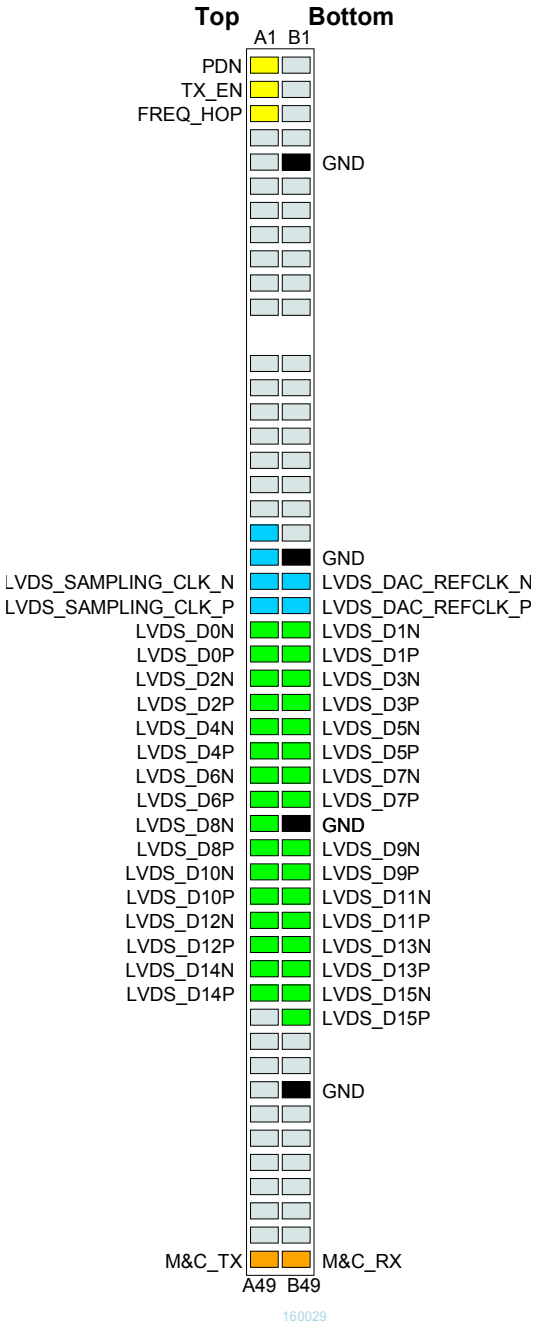
2*12-bit baseband input samples, compatible with COM-30xx receivers (**-C/-D** firmware options)

Right Connector J8



2*16-bit output samples, 2*12-bit input samples. This interface is compatible with the COM-3504 dual Analog<->Digital Conversions.
(**-A/-B** firmware options)

Right Connector J8



This interface is compatible with the COM-4009 RF modulator (**-C/-D** firmware options)

I/O Compatibility List

(not an exhaustive list)

Right connector (J8)
COM-3504 Dual Analog <-> Digital Conversions 2*16-bit 250 MSamples/s
COM-4009 400 MHz – 4.4 GHz Broadband RF modulator
Left connector (J4)
COM-30xx RF/IF/Baseband receivers for frequencies ranging from 0 to 3 GHz.

Configuration Management

This specification is to be used in conjunction with VHDL software revision 1 and ComBlock control center revision 4.0 and above.

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1831 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

ECCN: 5A001.b.3

ComBlock Ordering Information

COM-1831 Burst-mode direct sequence spread-spectrum modem. 80 Mchip/s.

MSS • 845 Quince Orchard Boulevard Ste N•
Gaithersburg, Maryland 20878-1676 • U.S.A.
Telephone: (240) 631-1111
Facsimile: (240) 631-1676
E-mail: sales@comblock.com