COM-1827SOFT_SOQPSK Modem
VHDL source code overview / IP core

Overview

The COM-1827SOFT_SOQPSK is a SOQPSK modulator and demodulator- written in generic VHDL.

The entire **VHDL source code** is deliverable. It is portable to a variety of FPGA targets.

Key features and performance:

- SOQPSK is a spectrum-efficient constant envelope modulation well suited for operation through power amplifiers near saturation.
- Flexible programmable features:
  - Symbol rate up to $\mathbf{f_{clk}}/4$, where $\mathbf{f_{clk}}$ is the processing clock frequency.
  - SOQPSK-MIL and SOQPSK-TG
- Excellent BER performance using trellis decoding (SOVA). 4-bit soft-decision demodulator output for best FEC decoder performance.
- Performance:
  - Near theoretical BER vs Eb/No
  - ±50ppm symbol timing tracking
  - Carrier frequency acquisition: ±10% of symbol rate at the threshold
  - Acquisition threshold < 2dB Eb/No
- Provided with IP core:
  - VHDL source code
  - Matlab .m file for generating stimulus files for VHDL simulation of the demodulator and for end-to-end BER performance analysis at various signal to noise ratios
  - VHDL testbenches (back-to-back modem or stimulus file input)
  - PRBS11 test sequence generator, AWGN noise generator, BER tester

Configuration

Run-time configuration parameters

The user can set and modify the following controls at run-time through the top level component interface:

Modulator Parameters	Configuration
SYMBOL_RATE_NDIV	symbol rate expressed as (modulator processing clock)/2^NDIV Range 0 to 15 for division ratios ranging from 1 to 32768
MODULATION_INDEX	modulation index h. unsigned fixed-point format 4.12. h is always 0.5 (0x0800) for SOQPSK
GAIN	output amplitude scaling factor. 15-bit unsigned
CENTER_FREQ	modulated signal center frequency. Expressed as fc/modulator processing clock * 2^32
CENTER_FREQ	modulated signal center frequency. Expressed as fc/modulator processing clock * 2^32
BURST_LENGTH	A synchronization word is inserted periodically between frames (to resolve any phase ambiguity at the receiver). This just includes the data field, not the 32-bit preamble. Constraint: BURST_LENGTH is a multiple of 8 bits. composite limit: preamble+sync+BURST_LENGTH < 8191
CONTROL	bits 2:0 modulation order M (always 3 for SOQPSK) bits 7:4 frequency shaping filter selection 5 = SOQPSK-MIL 6 = SOQPSK-TG bits 9:8 test mode: 00 no test, 01 = PRBS11, 11 = unmodulated carrier
	bit 10: always '1' to enable sync word insertion bit 11: spectrum inversion. invert Q. on (1) or off (0)

Receiver Parameters	Configuration
AGC_RESPONSE	Adjust the AGC response time. approximately log2(NSymbols).
RECEIVER_CENTER_FREQ	nominal (i.e. expected) center frequency. Expressed as fc/demodulator processing clock * 2^32 -- This frequency is subtracted from the input signal center frequency. Add -fclk/4 when used in conjunction with IF undersampling.
CIC_R	CIC Decimation ratio. The output sampling rate is thus fclk/R -- 1 to bypass. 0 is illegal, otherwise, nominal range is 1 to 16384. -- Usage: be careful not to decimate too much as the CIC decimation filter is not very sharp and thus can distort the modulated signal. -- Rule of thumb: the CIC filter output sampling rate should be >= 4 samples per symbol.
NOMINAL_SYMBOL_RATE	fsymbol rate / fclk * 2^32 = nominal symbol rate
M_SEL	modulation order M selection. Always 3 for SOQPSK -- 0: M=2
FILT_SEL	Filter selection: 5 = SOQPSK-MIL 6 = SOQPSK-TG
MODULATION_INDEX	modulation index h. unsigned fixed-point format 4.12. h is always 0.5 (0x8000) for SOQPSK

FRAME_LENGTH	Frame length, including payload + 32-bit sync word
DEMOD_CONTROL	bit 0: spectrum inversion enabled(1)/disabled(0) bit 1: AFC enabled(1)/disabled(0). bit 2: freeze AGC bit 3: sync word detection enabled (1)/disabled(0) REQUIRED WITH SOQPSK MODULATIONS bit 4: FFT enabled(1)/disabled(0) to increase the frequency acquisition range

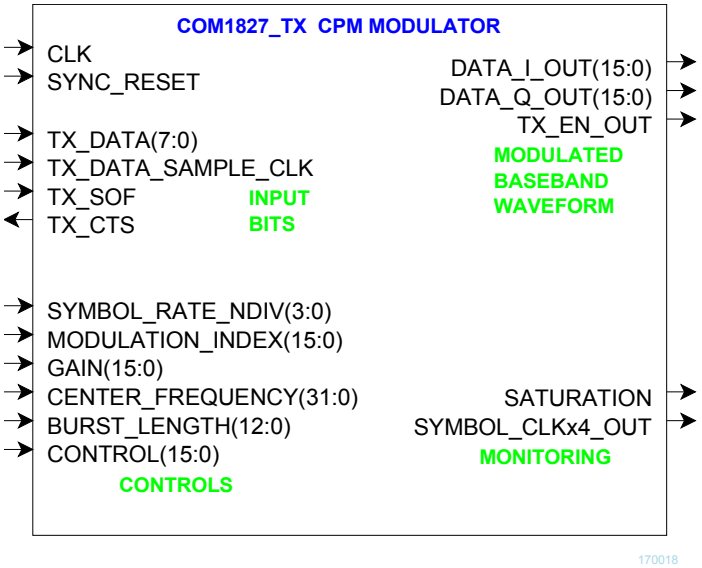
I/Os

General

CLK: input
The synchronous clock. The user must provide a global clock (use BUFG). The CLK timing period must be constrained in the .xdc file associated with the project.

SYNC_RESET: input
Synchronous reset. The reset MUST be exercised at least once to initialize the internal variables. It must be exercised whenever a control parameter is changed.

Modulator



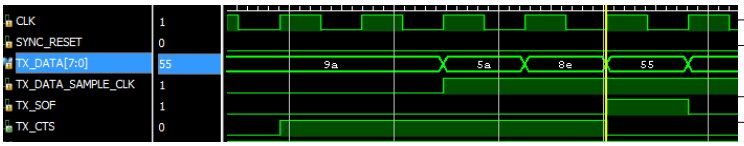
TX_DATA(7:0): Input data byte. The MSb is sent first.

TX_DATA_SAMPLE_CLK: input.
1 CLK-wide pulse indicating that TX_DATA is valid.

TX_SOF: optional input Start Of Frame. 1 CLK-wide pulse.
The SOF is aligned with **TX_DATA_SAMPLE_CLK**.

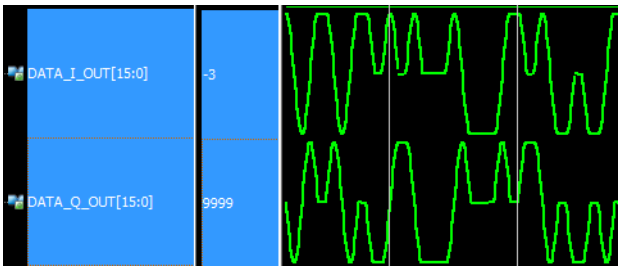
TX_CTS: output.
Clear-To-Send flow control. '1' indicates that the modulator is ready to accept another input byte.

Thanks to an input elastic buffer, the data source is allowed to send a few more bytes after TX_CTS goes low.



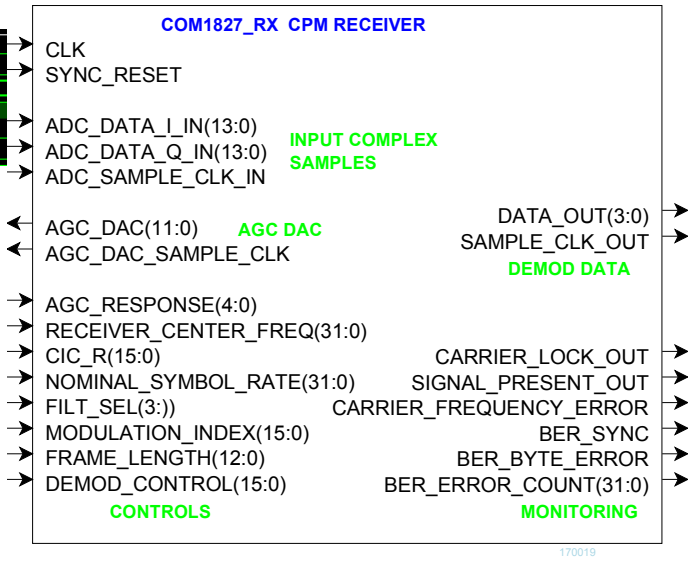
Modulator input flow control example

DATA_I/Q_OUT(15:0): Modulated baseband output samples (I = in-phase, Q = quadrature). One output sample every clock. Format: 2's complement (signed)



TX_EN_OUT: goes low to turn off an external power amplifier when the modulator is not receiving any input data.

Receiver

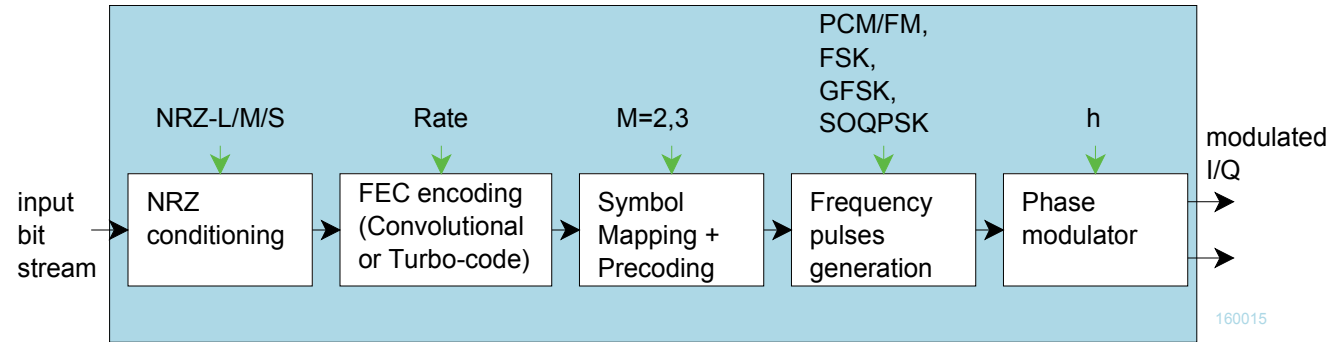


ADC_DATA_I/Q_IN(13:0): input samples from one or two external ADCs. (one in the case of IF undersampling, two for near-zero frequency complex inputs). If the ADCs have fewer than 14-bit precision, align the most significant bit with ADC_DATA_IN(13). Format: 2's complement (signed).

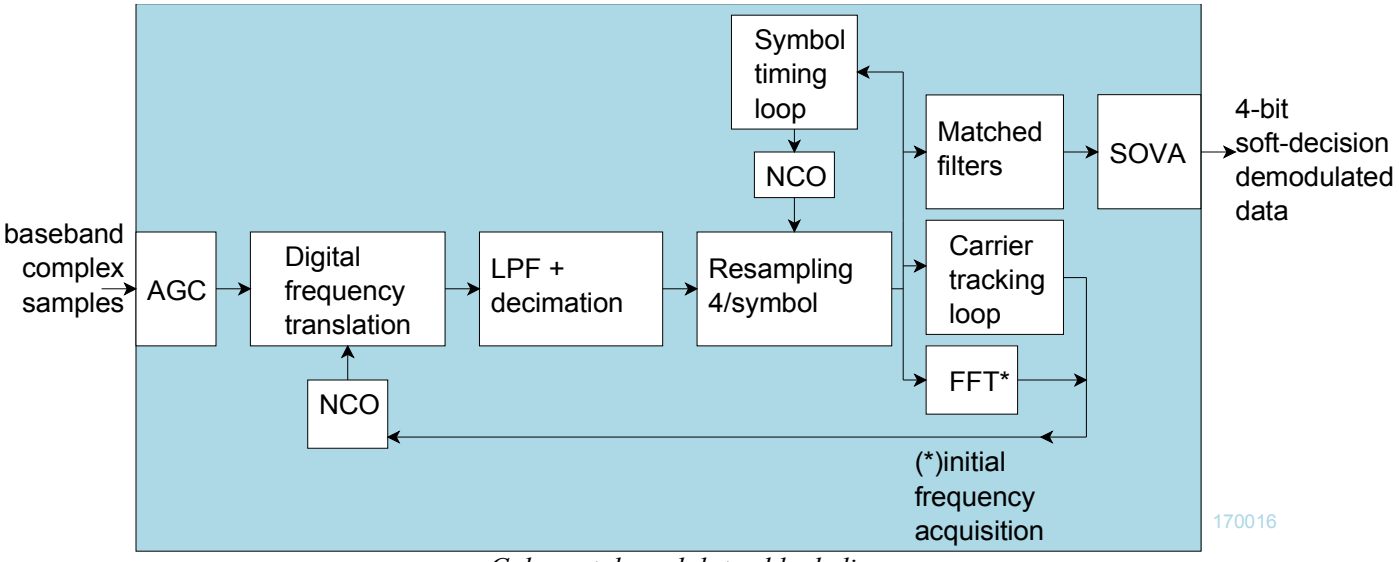
AGC_DAC(11:0): output to an external DAC to control an external AGC. Read when **AGC_DAC_SAMPLE_CLK** is '1'

DATA_OUT(3:0): soft-decision output. The demodulated bit is bit 3. The three lower bits indicate the level of confidence: "0000" for a solid '0', "1111" for a solid '1', "1000" for a '1' barely above the thresold.

Design considerations



Modulator block diagram



Coherent demodulator block diagram

Frequency pulse generation

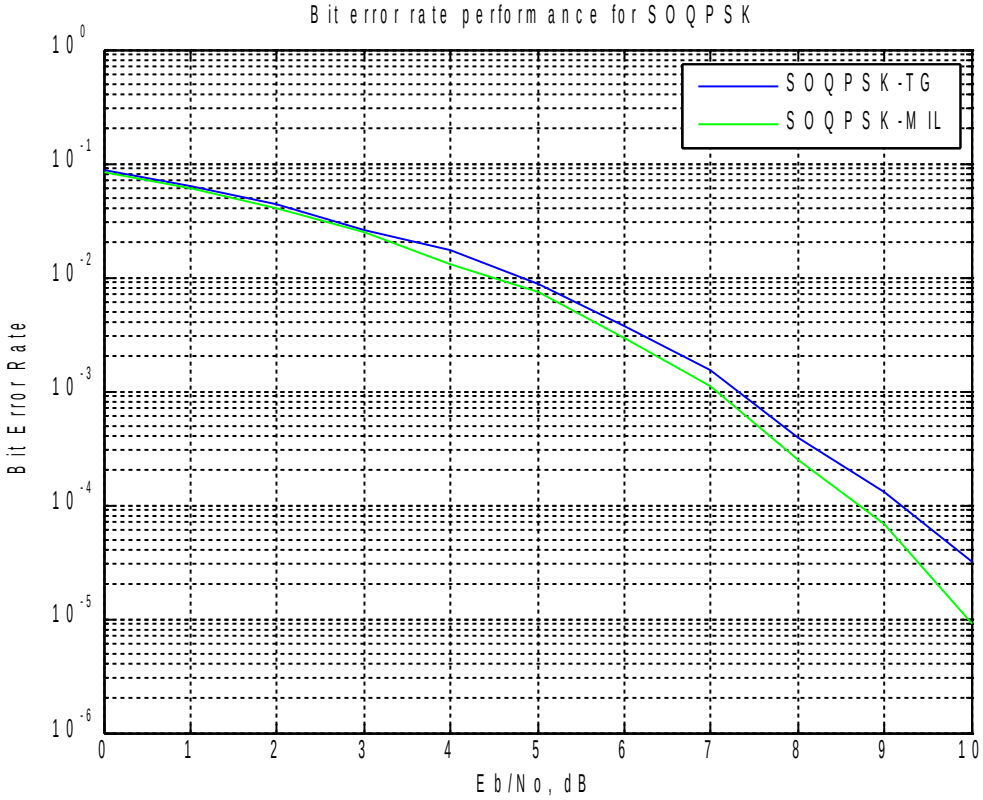
An FIR filter shapes the frequency pulses. The FIR coefficients are stored in a lookup table, sampled at 4 samples/symbol. See CPM_FILTERSx4.vhd. The table is large enough to store multiple frequency pulse shapes: rectangular pulse for MSK, Gaussian pulse for GMSK, raised cosine for PCM/FM, etc.

The Matlab program /`matlab/siggen_fsk1.m` is used to generate the FIR coefficients.

Performance

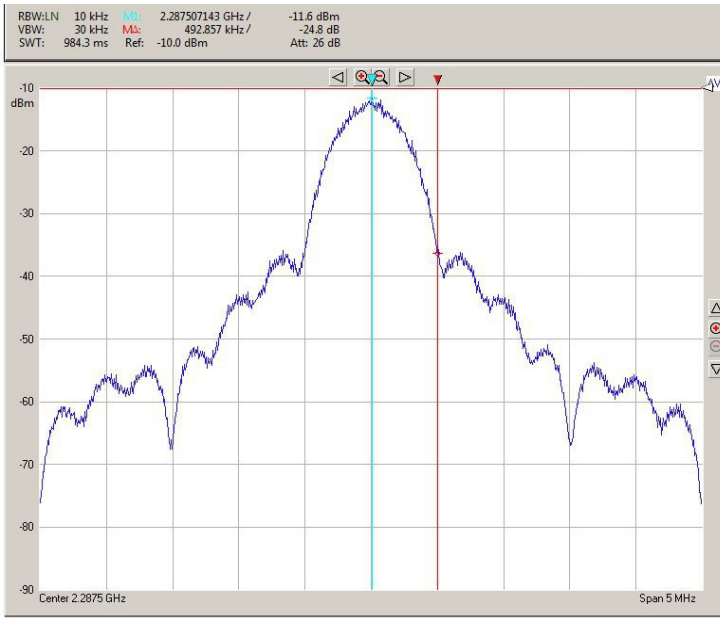
BER vs Eb/No

The plot below shows near-theoretical performance for the SOQPSK demodulator without error correction.

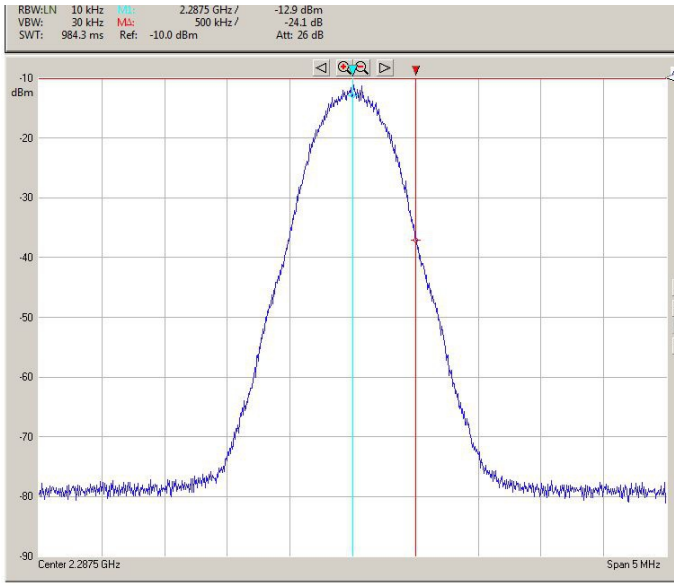


Test condition: +50ppm symbol timing error, 30deg carrier phase error

Transmitted spectrum



SOQPSK-MIL



SOQPSK-TG

Latency

The latency between received signal and demodulated bit output is approximately 20 bits.

Software Licensing

This software is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bit stream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from http://www.comblock.com/download/softwarelicense.pdf

Portability

The VHDL source code is written in generic VHDL and thus can be ported FPGAs from various vendors. See the limitation below.

Limitation

1. The modulator requires a processing and DAC clock in the form (symbol rate * 2^N), where N is an integer in the range 2-15. The COM1827SOFT includes a Xilinx primitive to program the clock frequency, allowing any target symbol rate with a precision of 1% or better. This Xilinx primitive is restricted to the Xilinx 7-series FPGAs (Artix, Kintex, Virtex, Zynq). For other target platforms, the user is responsible for generating the processing/DAC clock.

Configuration Management

The current software revision is 1a.

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code,.pkg packages, .xdc constraint files (Xilinx) One component per file.
/sim	VHDL test benches
/matlab	Matlab .m file for generating stimulus files for VHDL simulation and for end-to-end BER performance analysis at various signal to noise ratios
/bin	.bit configuration files (for use with ComBlock COM-1800 FPGA development platform)

Project files:

Xilinx ISE 14 project file: com-1827.xise
Xilinx Vivado v2015.2 project file: project_1.xpr

VHDL development environment

The VHDL software was developed using the following development environment:

(a) Xilinx ISE 14.7 for synthesis, place and route

(b) Xilinx Vivado 2015.2 for synthesis, place and route and VHDL simulation

The entire project fits easily within a Xilinx Artix7-100T. Therefore, the ISE project can be processed using the free Xilinx WebPack tools.

Device Utilization Summary

The modulator size is fixed (not parameterized).

Device: Xilinx Artix7-100T

Modulator		% of Xilinx Artix7-100T
Registers	1868	1%
LUTs	2078	3%
Block RAM/FIFO	10	7%
DSP48	11	4%
GCLKs	1	3.1%

The receiver size is fixed (not parameterized).

Receiver **4-bit soft-quantization**		% of Xilinx Artix7-100T
Registers	9587	7%
LUTs	11522	18%
Block RAM/FIFO	9	6%
DSP48	61	25%
GCLKs	3	9%

Clock and decoding speed

The entire design uses a single global clock CLK. Typical maximum clock frequencies for various FPGA families are listed below:

Device family	**Modulator**	**Demodulator**
Xilinx Artix 7 -1 speed grade	160 MHz	150 MHz
Xilinx Kintex-7 -2 speed grade		

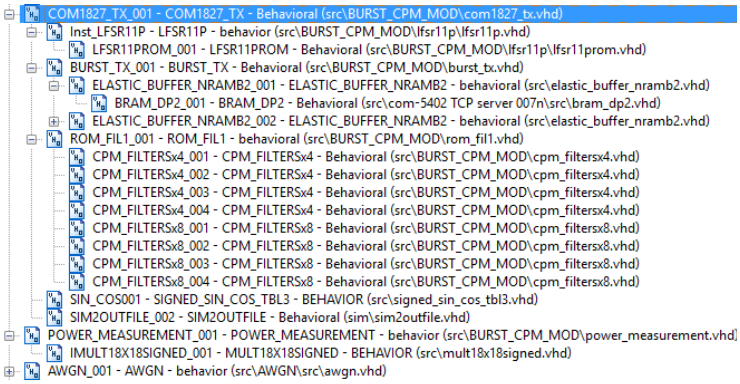
Ready-to-use Hardware

The COM-1827SOFT was developed on, and therefore ready to use on the following commercial off-the-shelf hardware platform:

FPGA development platform
COM-1800 FPGA (XC7A100T) + ARM + DDR3 SODIMM socket + GbE LAN development platform

VHDL components overview

Modulator top level



COM1827_TX.vhd generates complex baseband continuous phase-modulated samples from byte-size input data.

The *BURST_TX.vhd* component stores input data in an elastic input buffer, then packs input bits into symbols (1,2,3 bits/symbol) at the specified symbol rate. It also stops the transmitter when the input elastic buffer is empty.

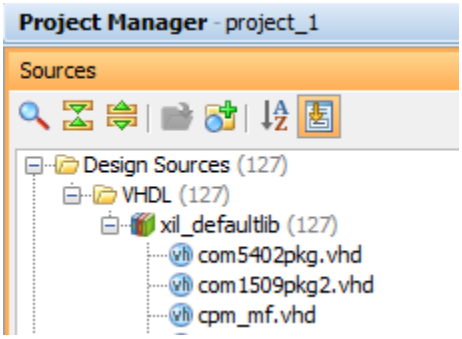
BRAM_DP2.vhd is a generic dual-port memory, used as input and output elastic buffers. Memory is inferred (no Xilinx primitive is used).

ROM_FIL1.vhd implements an FIR filter to shape the frequency pulses. The FIR filter coefficients for various modulation schemes (Gaussian, raised cosine, etc) are stored in the *CPM_FILTERSx4.vhd* ROM.

SIGNED_SIN_COS_TBL3.vhd stores sine and cosine functions in ROM. It is used to convert phase to complex I/Q baseband output samples.

COM1827_TOP.vhd: is mostly a use example when the SOQPSK modem is implemented on a ComBlock COM-1800 FPGA development platform. Please note that this top component can't be simulated as it makes many references to other components outside the scope of the modem proper (TCP stack, turbo codec, etc)

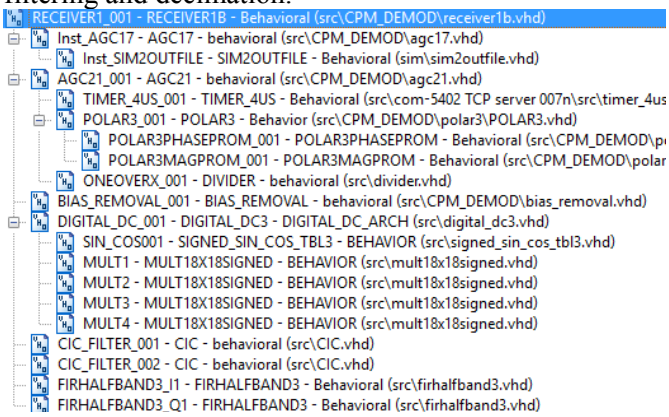
Note for Xilinx Vivado: when creating the project, the file priority order is unimportant, except for the three packages below which must be placed with a higher priority order:



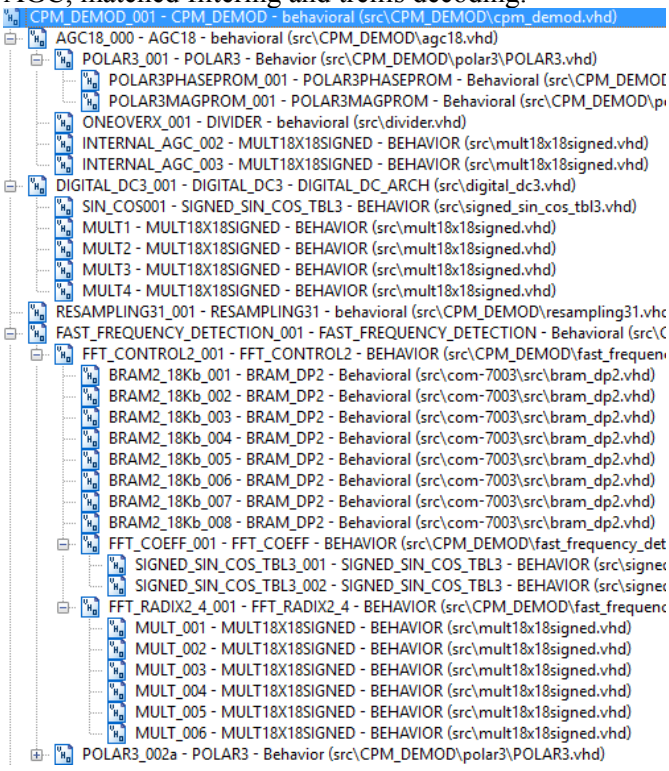
Receiver top level

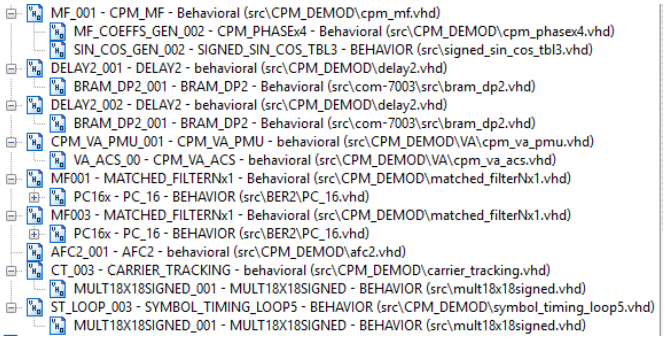
The receiver is comprised of two high-level components:

RECEIVER1.vhd performs non modulation-specific tasks such as AGC, DC bias removal, frequency translation to baseband, anti-aliasing filtering and decimation.



CPM_DEMOD.vhd performs the continuous phase demodulation, including carrier tracking (for coherent demodulation), symbol timing tracking, AGC, matched filtering and trellis decoding.

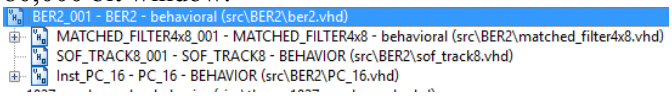




Ancillary components

LFSR11P.vhd is a pseudo-random sequence generator used for test purposes. It generates a PRBS11 test sequence commonly used for bit error rate testing at the receiving end of a transmission channel.

BER2.vhd is a bit error rate tester expecting to receive a PRBS11 test sequence. It synchronizes with the received bit stream and count errors over a 80,000 bit window.



AWGN.vhd generates a precise Additive White Gaussian Noise. The noise bandwidth is 2*symbol rate.

INFILE2SIM.vhd reads an input file. This component is used by the testbench to read a modulated samples file generated by the `siggen_fsk1.m` Matlab program for various Eb/No and frequency offset cases.

SIM2OUTFILE.vhd writes three 12-bit data variables to a tab delimited file which can be subsequently read by Matlab (load command) for plotting or analysis.

VHDL simulation

VHDL testbenches are located in the /sim directory.

The `tbcom1827_modemonly.vhd` connects the modulator and demodulator back to back. End-to-end BER tests can be performed as the `com1827_tx.vhd` transmitter includes a built-in pseudo-random sequence generator and the

com1827_rx.vhd receiver includes a built-in Bit Error Rate Tester.

The tbcom1827_demodonly.vhd testbench reads a tab-delimited stimulus files of modulated I/Q baseband complex input samples.

Matlab simulation

Matlab programs are located in the /matlab directory.

The siggen_fsk1.m program generates a stimulus file input.txt for use as input to either the demodulator VHDL simulation (tbcom1827_demodonly.vhd) or the demod_soqpsktg.m Matlab program. The stimulus file includes a continuous stream of pseudo-random (PRBS11) data bits, convolutional code encoding, SOQPSK modulation, additive white Gaussian noise, channel filtering, frequency translation and quantization.

Care must be taken to match the modulator configuration in siggen_fsk1.m and the demodulator configuration in tbcom1827_demodonly.vhd.

This setup allows end-to-end BER testing, as the demodulator com1827_rx.vhd includes a built-in bit error rate tester.

The demod_soqpsktg.m program applies key demodulation techniques to the stimulus file input.txt and computes the BER. It does not include AFC, AGC nor carrier and symbol timing tracking loops.

Specifications

[1] IRIG-106 “Telemetry Standard RCC Document 106-07, Chapter 2”, for SOQPSK TG

[2] MIL-STD-188-181B for SOQPSK-MIL

Reference documents

[3] "Comparison of Noncoherent detectors for SOQPSK and GMSK in Phase Noise Channels", Afzal Syed, MS thesis, University of Kansas, 2007

[4] "A Hardware Implementation of a Coherent SOQPSK-TG Demodulator for FEC Applications", Gino Pedro Enrique Rea Zanabria, MS thesis, University of Kansas, 2011

ComBlock Ordering Information

COM-1827SOFT_SOQPSK modem, VHDL source code / IP core

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