COM-1827SOFT GMSK DEMODULATOR
VHDL source code overview / IP core

Overview

The COM-1827SOFT GMSK DEMOD is a continuous phase demodulator written in generic VHDL.

The entire **VHDL source code** is deliverable. It is portable to a variety of FPGA targets.

Key features and performance:

- Supports FSK, MSK, GFSK, GMSK modulations. These are constant amplitude modulation well suited for operation through power amplifiers near saturation.
- Flexible programmable features:
  - Modulation index h. (0.5 for MSK and GMSK).
  - Multiple BT products for Gaussian filters: 0.7, 0.5, 0.3, 0.25
  - Symbol rate up to $f_{clk}/4$, where f_{clk} is the processing clock frequency.
- MSK, GMSK: coherent demodulation with excellent BER performance using trellis decoding (SOVA).
- FSK, GFSK: non-coherent demodulation with excellent BER performance using multi-symbol detection and trellis decoding (SOVA).
- 4-bit soft-decision demodulator output for best FEC decoder performance.
- Performance:
  - BER < 10^{-5} at 9.2dB Eb/No
  - ±50ppm symbol timing tracking
  - Carrier frequency acquisition of 10% of symbol rate
  - Acquisition threshold < 2dB Eb/No
- Provided with IP core:
  - VHDL source code
  - Matlab .m file for generating stimulus files for VHDL simulation of the demodulator and for end-to-end BER performance analysis at various signal to noise ratios
  - VHDL testbench (stimulus file input, or back-to-back modem when used in conjunction with the CPM modulator IP core)
  - BER tester

Configuration

Run-time configuration parameters

The user can set and modify the following controls at run-time through the top level component interface:

Receiver Parameters	Configuration
AGC_RESPONSE	Adjust the AGC response time. approximately log2(NSymbols).
RECEIVER_CENTER_FREQ	nominal (i.e. expected) center frequency. Expressed as fc/demodulator processing clock * 2^32 -- This frequency is subtracted from the input signal center frequency. Add -fclk/4 when used in conjunction with IF undersampling.
CIC_R	CIC Decimation ratio. The output sampling rate is thus fclk/R -- 1 to bypass. 0 is illegal, otherwise, nominal range is 1 to 16384. -- Usage: be careful not to decimate too much as the CIC decimation filter is not very sharp and thus can distort the modulated signal. -- Rule of thumb: the CIC

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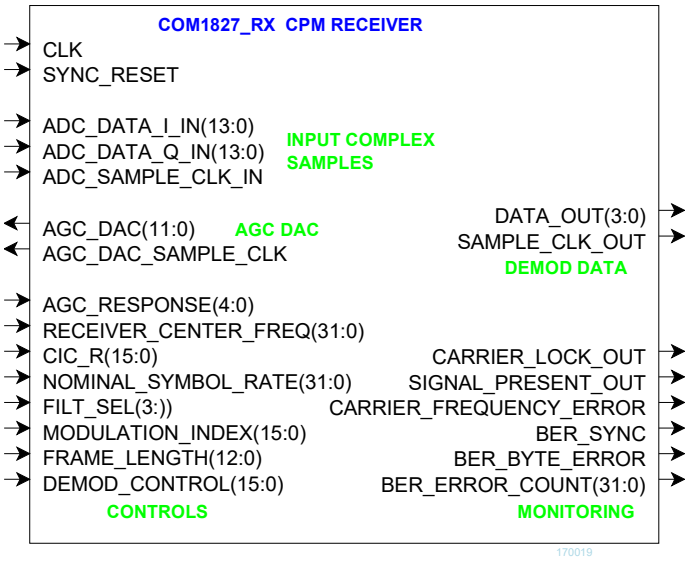
	filter output sampling rate should be > 4 samples per symbol.
NOMINAL_SYMBOL_RATE	fsymbol rate / fclk * 2^32 = nominal symbol rate
M_SEL	modulation order M selection. Always 0 for FSK/MSK/GFSK/GMSK -- 0: M=2
FILT_SEL	Filter selection: 0 = FSK 2 = GMSK/GFSK BT=0.7 3 = GMSK/GFSK BT=0.5 4 = GMSK/GFSK BT=0.3 8 = GMSK/GFSK BT=0.25
MODULATION_INDEX	modulation index h. unsigned fixed-point format 4.12. h must be 0.5 (0x0800) for MSK and GMSK.
FRAME_LENGTH	Optional frame length, including payload + 32-bit sync word
DEMOD_CONTROL	bit 0: spectrum inversion enabled(1)/disabled(0) bit 1: AFC enabled(1)/disabled(0). Use only for FKS and GPSK. bit 2: freeze AGC bit 3: optional sync word detection enabled (1)/disabled(0) bit 4: FFT : enabled (1) for MSK and GMSK, disabled (0) otherwise bit 5: enable(1)/disable(0) sync word removal at output. Generally remove, except when another sync detection follows after the demod

I/Os

General

CLK: input
The synchronous clock. The user must provide a global clock (use BUFG). The CLK timing period must be constrained in the .xdc file associated with the project.

SYNC_RESET: input
Synchronous reset. The reset MUST be exercised at least once to initialize the internal variables. It must be exercised whenever a control parameter is changed.Receiver

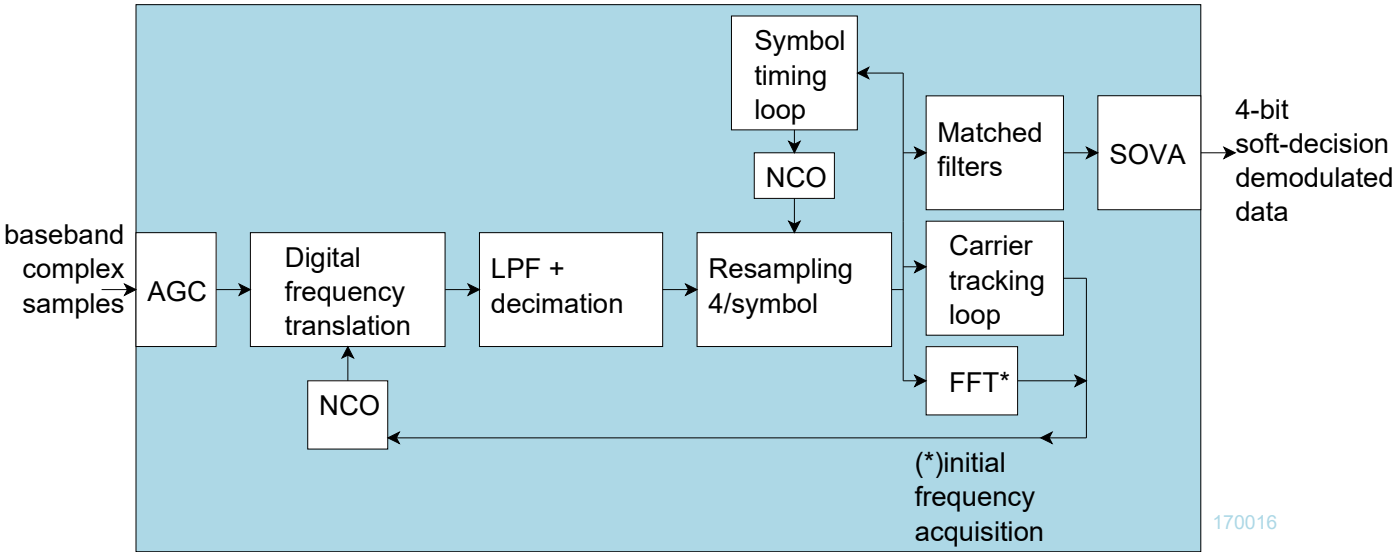


ADC_DATA_I/Q_IN(13:0): input samples from one or two external ADCs. (one in the case of IF undersampling, two for near-zero frequency complex inputs). If the ADCs have fewer than 14-bit precision, align the most significant bit with ADC_DATA_IN(13). Format: 2's complement (signed).

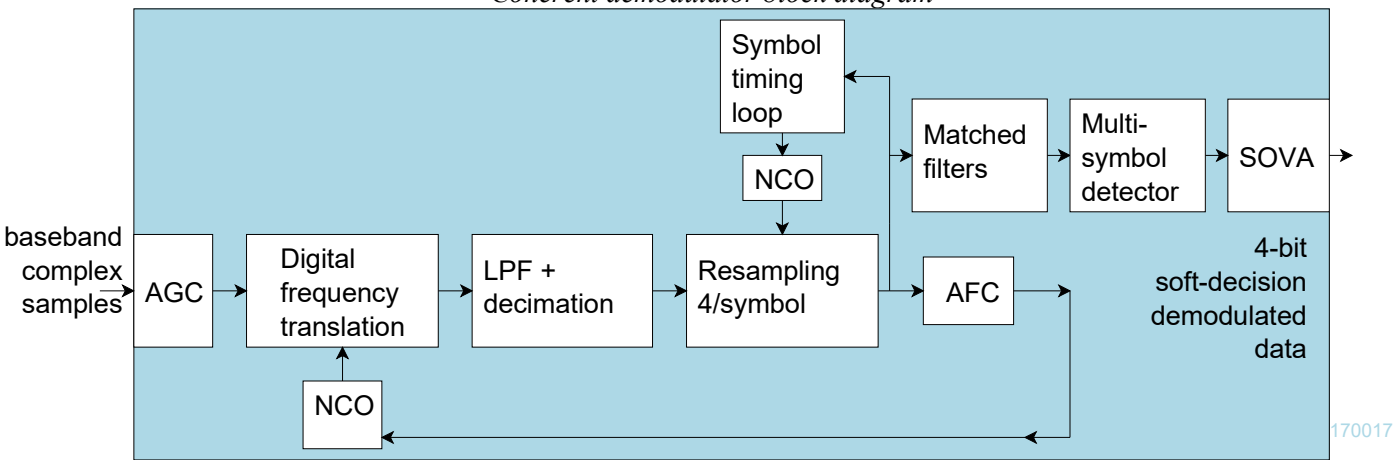
AGC_DAC(11:0): output to an external DAC to control an external AGC. Read when **AGC_DAC_SAMPLE_CLK** is '1'

DATA_OUT(3:0): soft-decision output. The demodulated bit is bit 3. The three lower bits indicate the level of confidence: "0000" for a solid '0', "1111" for a solid '1', "1000" for a '1' barely above the thresold.

Design considerations



Coherent demodulator block diagram

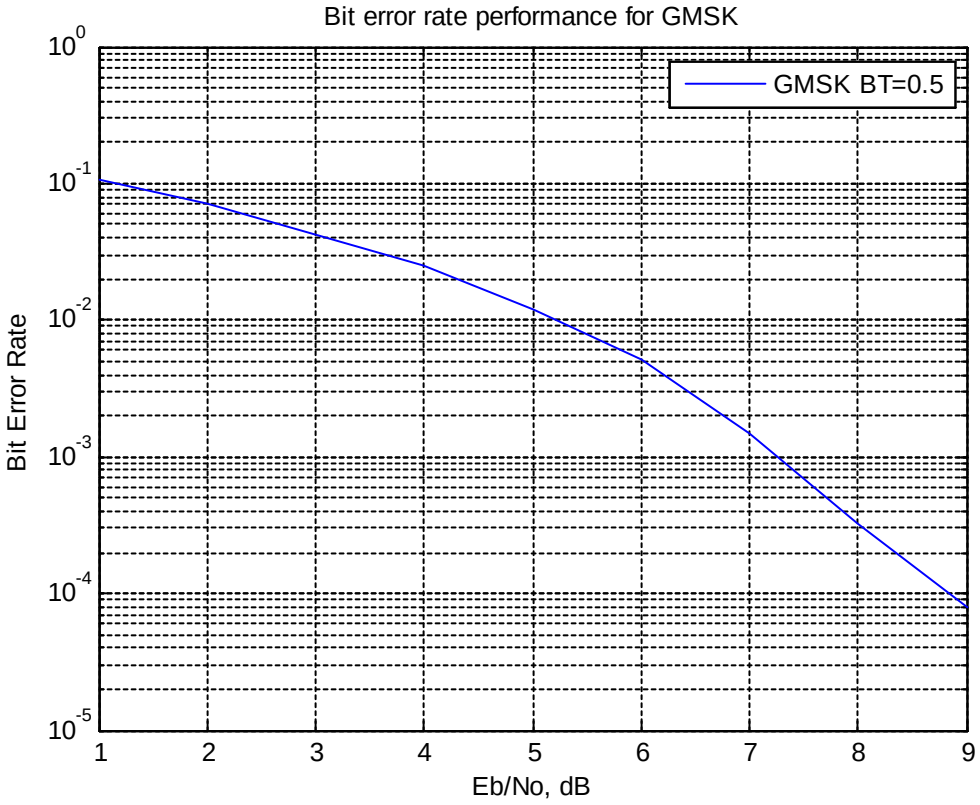


Non-coherent demodulator block diagram

Performance

BER vs Eb/No

The plot below shows near-theoretical performance for the GMSK (BT = 0.5) demodulator without error correction.



Software Licensing

This software is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bit stream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from http://www.comblock.com/download/softwarelicense.pdf

Portability

The VHDL source code is written in generic VHDL and thus can be ported FPGAs from various vendors.

Configuration Management

The current software revision is 1c.

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code,.pkg packages, .xdc constraint files (Xilinx) One component per file.
/sim	VHDL test benches
/matlab	Matlab .m file for generating stimulus files for VHDL simulation and for end-to-end BER performance analysis at various signal to noise ratios
/bin	.bit configuration files (for use with ComBlock COM-1800 FPGA development platform)

Project files:

Xilinx ISE 14 project file: com-1827.xise
Xilinx Vivado v2015.2 project file: project_1.xpr

VHDL development environment

The VHDL software was developed using the following development environment:

(a) Xilinx ISE 14.7 for synthesis, place and route

(b) Xilinx Vivado 2015.2 for synthesis, place and route and VHDL simulation

The entire project fits easily within a Xilinx Artix7-100T. Therefore, the ISE project can be processed using the free Xilinx WebPack tools.

Device Utilization Summary

The encoder size is fixed (not parameterized).

Device: Xilinx Artix7-100T

Receiver **4-bit soft-quantization**		% of Xilinx Artix7-100T
Registers	10171	8%
LUTs	13614	21%
Block RAM/FIFO	9	6%
DSP48	69	28%
GCLKs	3	9%

Clock and decoding speed

The entire design uses a single global clock CLK. Typical maximum clock frequencies for various FPGA families are listed below:

Device family	**Demodulator**
Xilinx Artix 7 -1 speed grade	160 MHz
Xilinx Kintex-7 -2 speed grade	

Ready-to-use Hardware

The COM-1827SOFT was developed on, and therefore ready to use on the following commercial off-the-shelf hardware platform:

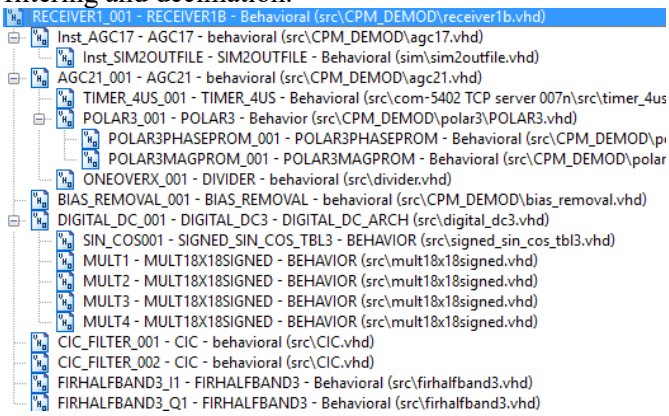
FPGA development platform
COM-1800 FPGA (XC7A100T) + ARM + DDR3 SODIMM socket + GbE LAN development platform

VHDL components overview

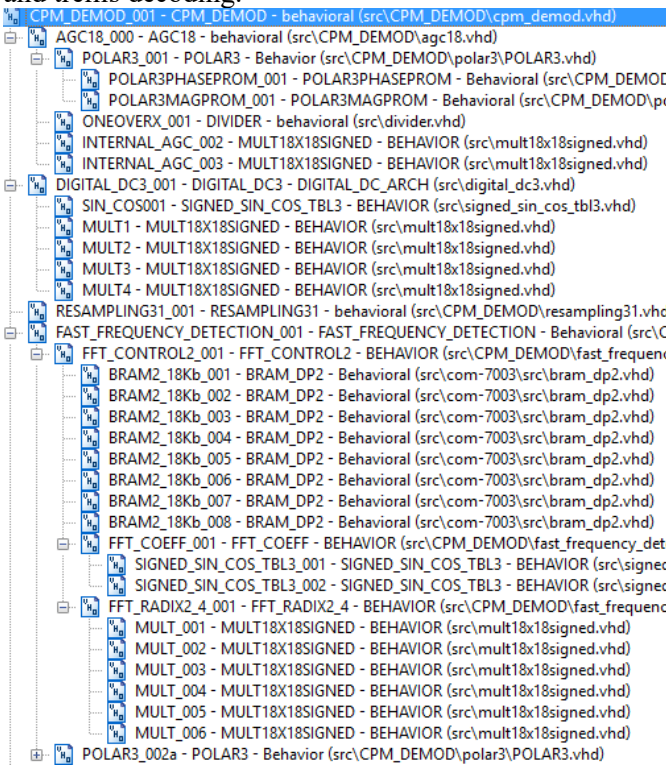
Receiver top level

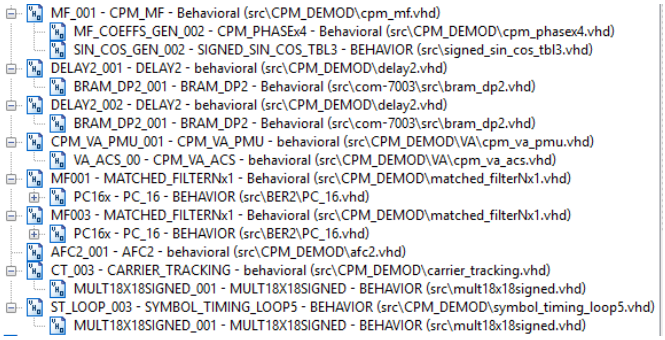
The receiver is comprised of two high-level components:

RECEIVER1.vhd performs non modulation-specific tasks such as AGC, DC bias removal, frequency translation to baseband, anti-aliasing filtering and decimation.



CPM_DEMOD.vhd performs the continuous phase demodulation, including symbol timing tracking, AGC, matched filtering, multi-symbol detection and trellis decoding.

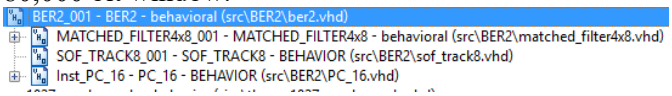




Ancillary components

LFSR11P.vhd is a pseudo-random sequence generator used for test purposes. It generates a PRBS11 test sequence commonly used for bit error rate testing at the receiving end of a transmission channel.

BER2.vhd is a bit error rate tester expecting to receive a PRBS11 test sequence. It synchronizes with the received bit stream and count errors over a 80,000 bit window.



AWGN.vhd generates a precise Additive White Gaussian Noise. The noise bandwidth is 2*symbol rate.

INFILE2SIM.vhd reads an input file. This component is used by the testbench to read a modulated samples file generated by the `siggen_fsk1.m` Matlab program for various Eb/No and frequency offset cases.

SIM2OUTFILE.vhd writes three 12-bit data variables to a tab delimited file which can be subsequently read by Matlab (load command) for plotting or analysis.

VHDL simulation

VHDL testbenches are located in the /sim directory.

com1827_rx.vhd receiver includes a built-in Bit Error Rate Tester.

The tbcom1827_demodonly.vhd testbench reads a tab-delimited stimulus files of modulated I/Q baseband complex input samples.

Matlab simulation

Matlab programs are located in the /matlab directory.

The siggen_fsk1.m program generates a stimulus file input.txt for use as input to either the demodulator VHDL simulation (tbcom1827_demodonly.vhd) or the demod_gmsk.m Matlab program. The stimulus file includes a continuous stream of pseudo-random (PRBS11) data bits, convolutional code encoding, FSK,MSK,GFSK,GMSK modulations, additive white Gaussian noise, channel filtering, frequency translation and quantization.

Care must be taken to match the modulator configuration in siggen_fsk1.m and the demodulator configuration in tbcom1827_demodonly.vhd.

This setup allows end-to-end BER testing, as the demodulator com1827_rx.vhd includes a built-in bit error rate tester.

The demod_gmsk.m program applies key demodulation techniques to the stimulus file input.txt and computes the BER. It does not include AFC, AGC and symbol timing tracking loops.

Reference documents

[1] http://www.ijeeee.org/Papers/307-A0021.pdf

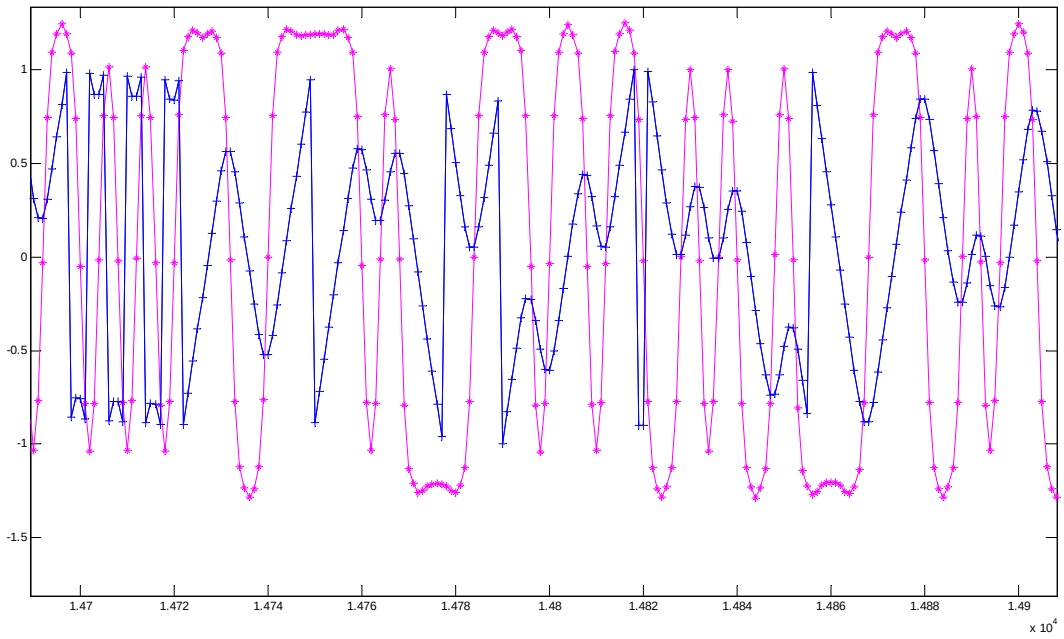
Implementation Overview

Symbol tracking loop (non-coherent)

The loop is designed to acquire and track symbol timing errors of +/-50ppm for SNR of 0dB or above.

The algorithm first computes the phase difference between two successive complex samples at 4 x the sampling rate. The phase difference is analoguous to a frequency. One sample is used to de-rotate the following sample. The resulting I value (FREQ2 in the code) is proportional to the phase difference between these two complex samples.

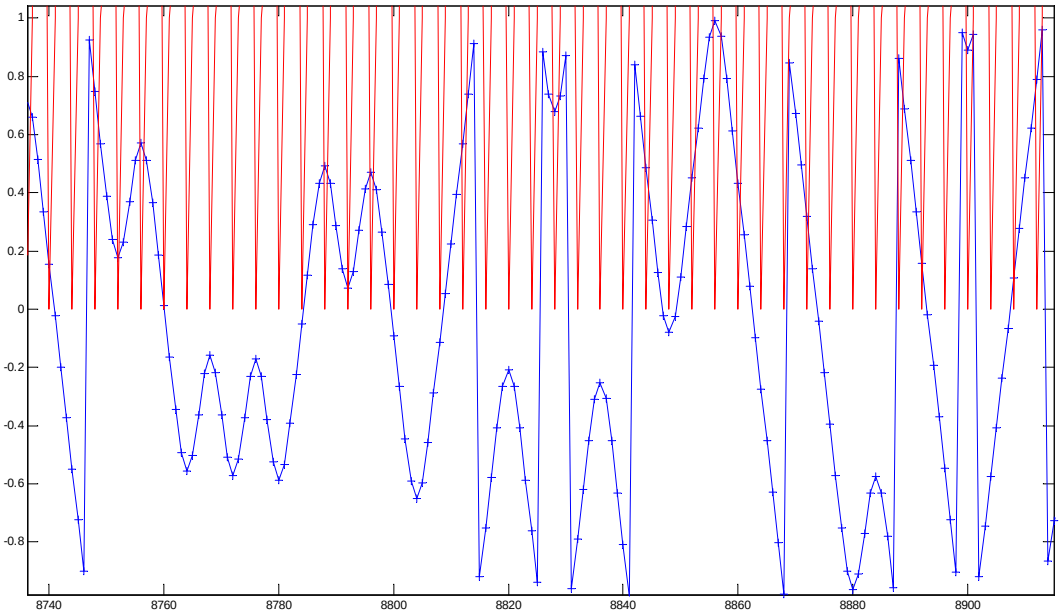
The symbol tracking loop is a first order Gardner loop. It finds the center of the FREQ2 symbols, and by way of consequence the zero crossing point as well.



Blue trace = phase of received complex baseband samples (in radians). h=0.7, noiseless.
Y axis scale: 1 = pi
Purple trace = FREQ2.

There are several delays between the *RESAMPLING3.vhd* and *the SYMBOL_TIMING_LOOP5.vhd* components worth noting:
1. the FREQ2 signal lags the actual received baseband signal by 1.5/4 symbol. This is clearly visible in the above plot.
2. the FREQ3 signal seen by the symbol tracking loop lags the actual received baseband signal by 1/2 symbol.
3. the *FIRHALFBAND3.vhd* filters used to reduce the noise power prior to symbol tracking, introduce a group delay of 10 samples = 2.5 symbols.
Both delays are compensated for in the code.

Verification: when the symbol timing loop is tracking properly, the SYMBOL3_CLK is aligned with the peak phase of the complex DATA3_X baseband signal.



Blue trace: phase/pi of complex DATA3_I/DATA3_Q signal after frequency down-conversion and resampling at 4x symbol rate.
Red trace: SYMBOL3_CLK

Matched filter

A partial correlation over one symbol period is computed: the received complex baseband signal is correlated with the conjugate of the expected (ideal) signal over one symbol period. The phase of the expected signal over one symbol period is stored in a lookup table CPM_PHASEx4.vhd. The stored phase is sampled at four samples/symbol, just like the received signal. Two different phase waveforms are stored, one for each received symbol hypothesis.

Multi-Symbol detection (non-coherent)

A multi-symbol detector extends the correlation over multiple symbols. Over a period of 3 symbols, there are 16 possible symbol hypothesis. The partial correlations are rotated and summed accordingly. The highest magnitude indicates the most likely symbols sequence. The 16 magnitude values are used as branch metrics for the subsequent 8-state trellis decoding.

Matched filter phases are stored in CPM_PHASEx4.vhd

Partial matched filter is computed in CPM_MF.vhd

The multi-symbol detection: CPM_MSD3.vhd

FFT (coherent)

In the case of MSK and GMSK, an FFT is used to acquire the initial frequency error over a window of at least +/- 10% of the symbol rate. Since the modulation index h is 0.5, the phase difference between successive symbols is 90 degrees. A power of 4 is applied to the complex input samples to remove the 90deg modulation.

The power-of-4 samples are then processed by a 2048-point FFT. If an FFT peak exceeds a threshold, signal presence is declared and the frequency error is corrected. The threshold is a function of the average noise level.

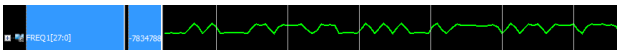
AFC (non-coherent)

The demodulator comprises an automatic frequency control (AFC) loop to acquire and track the residual frequency offset of the modulated signal. See *afc2.vhd* component.

The algorithm follows the one described in document [1].

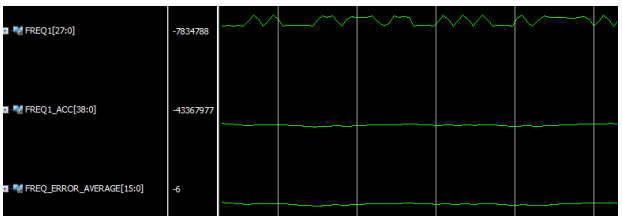
1. take two complex baseband samples separated by one symbol. These samples are taken after frequency correction.

2. One sample is used to de-rotate the other sample. The resulting I value (FREQ1 in the code) is proportional to the phase difference between these two samples.

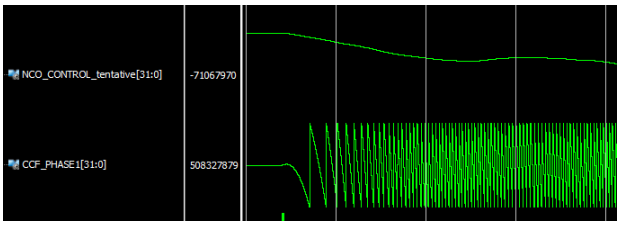


Most of the changes are due to the actual modulation. However, any frequency error will generate a bias.

3. Average FREQ1 over 1024 symbols, as a way to remove most of the modulation since bits are expected to be randomly distributed between 0s and 1s.



4. The average is accumulated to create the NCO control value, after appropriate scaling. The AFC rate of convergence depends on the scaling.



Some ripple is expected in the NCO control value because of imbalances in the data stream (show is a PRBS11 test sequence with slightly unequal numbers of 0s and 1s.)

ComBlock Ordering Information

COM-1827SOFT GMSK DEMOD, VHDL source code / IP core

Contact Information

MSS • 845-N Quince Orchard Boulevard •
Gaithersburg, Maryland 20878-1676 • U.S.A.

Telephone: (240) 631-1111
E-mail: info@comblock.com