COM-1826SOFT_RX TDRSS DSSS Receiver VHDL source code overview / IP core

Overview

The COM-1826SOFT_RX is a NASA/TDRSS-compliant Direct Sequence Spread-Spectrum (DSSS) receiver written in generic VHDL.

The entire **VHDL source code** is deliverable. It is portable to a variety of FPGA targets.

Key features and performance:

- TDRSS spread-spectrum digital receiver
  - Accepts 3 types of input waveforms:
    - complex I/Q input samples from an external ADC.
    - IF samples received over 1GbE LAN using NASA SDDS-formatted UDP-IP packets.
    - tab-delimited text file (during VHDL simulation)
  - BPSK and SQPN spread-spectrum demodulation. 120-bin parallel code search for fast code acquisition. False code lock prevention.
  - Demodulation performances: within 1.5 dB from theory at threshold Eb/No of 2 dB.
  - Programmable 1023- (forward command link) or 2047-chip (return mode 2 link) periodic I and Q Gold codes
  - Programmable bit rates from 1 to 150 Kbits/s independent on each channel.
  - Frequency table to dynamically correct the receiver expected center frequency and expected chip rate, by steps of 1/64s.
  - Viterbi error correction: K=7 Rate ½
  - NRZ conversion
  - 3 output types are supported:
    - Demodulated bits encapsulated in UDP frames are sent out to the GbE LAN. Support for IGMPv2 multicast addressing.
    - simply sent to the application via the component interface
    - written to a file (during VHDL simulation)
- Provided with IP core:
  - VHDL source code
  - Matlab signal generation .m program for generating baseband waveforms.
  - Built-in Bit Error Rate measurement for PRBS-11 test sequences.

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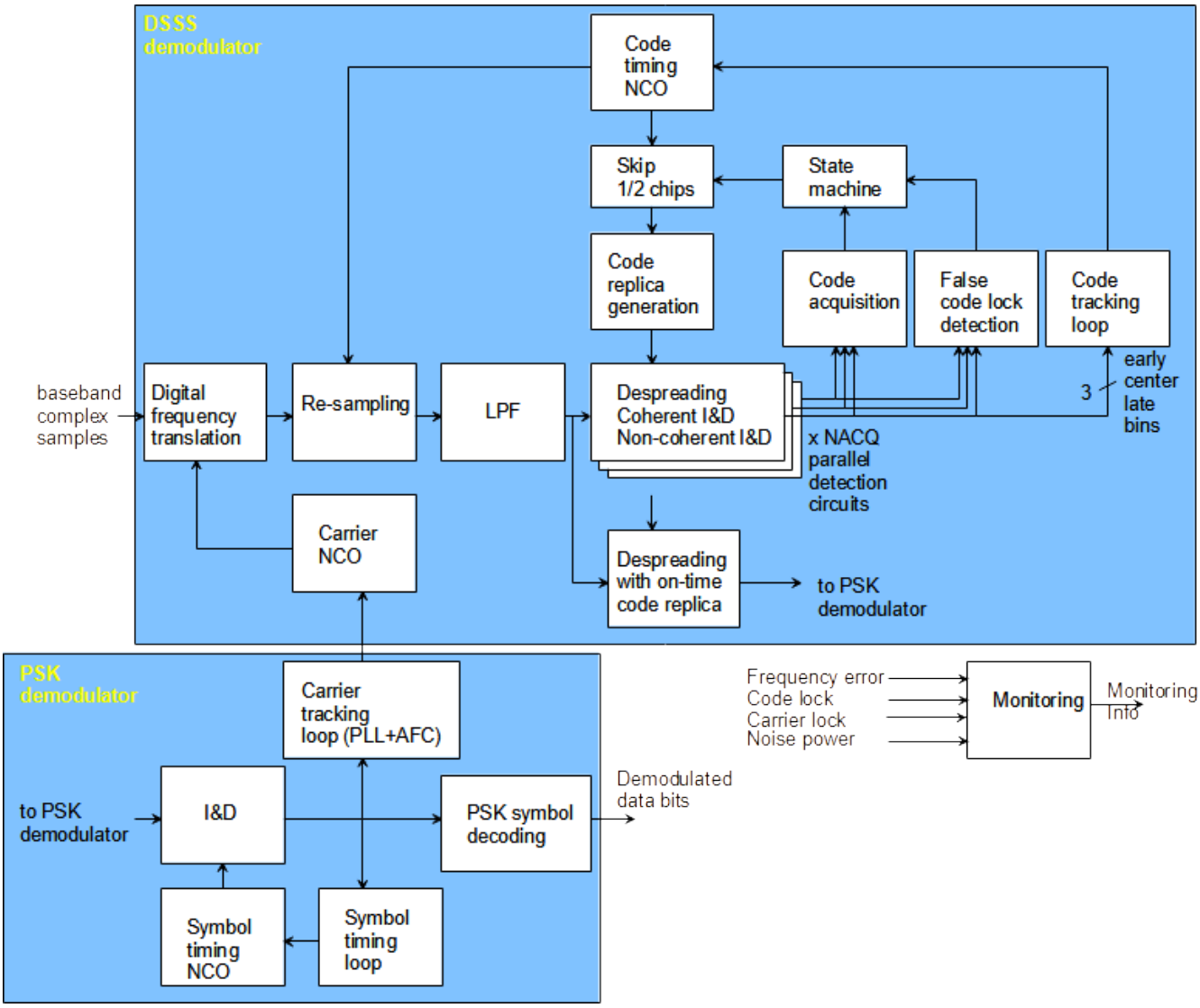
Block Diagram



Demodulator block diagram

Configuration

Synthesis-time configuration parameters

The following constants are user-defined in the *COM1826_RX.vhd* component generic section prior to synthesis.

Synthesis-time configuration parameters	Configuration
SIMULATION	(1) during VHDL simulation (0) during deployment

Run-time configuration parameters

The user can set and modify the following controls at run-time through the top level component interface:

Rx Parameters	Configuration
AGC RESPONSE TIME(4:0)	Adjust the AGC response time. approximately log2(NSymbols)
RECEIVER_CENTER_FREQ(31:0)	Expected received signal center frequency. Typically 0 for a complex baseband input. Expressed as 2^32 * fc/ f_{CLK}
NOMINAL_CHIP_RATE (32:0)	Expected chip rate expressed as 2^32* chip rate / f_{CLK} Chip rate must be strictly less than $f_{CLK}/2$. Typically 3.077799479166 Mchips/s for TDRSS SMA
CIC_R(15:0)	CIC Decimation ratio. The output sampling rate is thus fclk/R: 1 to bypass. 0 is illegal, otherwise, nominal range is 1 to 16384. Usage: be careful not to decimate too much as the CIC decimation filter is not very sharp and thus can distort the modulated signal. Rule of thumb: the CIC filter output sampling rate should be >= 8 samples per chip.
SPREADING_FACTOR1(12:0) SPREADING_FACTOR2(12:0)	Spreading factor. Valid range 3 - 8191 = nominal chip rate / nominal symbol rate. Not necessarily equal to the spreading code period. Channel1/I spreading factor is always less than channel2/Q.
LFSRA_INIT(10:0) LFSRC_INIT(10:0)	Gold code selection as spreading sequence. LFSR initialization. see definition in Space network interoperable pn

	code libraries, Appendix A
NOMINAL_SYMBOL_ RATE1(31:0) NOMINAL_SYMBOL_ RATE2(31:0)	Expected symbol rates, for I and Q channels respectively. Symbol rate expressed as 2^32* symbol rate / f_{CLK}
CODE_MODE	0 = forward command link Gold codes 1 = return mode 2 link Gold codes
FREQ_SCAN_N_ COARSE_STEPS(7:0)	number of frequency acquisition steps in each direction. Total number of frequencies is thus 2*N_STEPS+1 Coarse scan step size is (symbol rate/4)
FEC_DECODER_ ENABLED (1:0)	Independent Viterbi decoder control for each I/Q channels Bit 0: I-channel Bit 1: Q-channel (0) disabled/bypassed, (1) enabled
NRZ1_RX_CONTROL (2:0) NRZ2_RX_CONTROL (2:0)	Converts NRZ-L to NRZ-L/M/S Two converters, for I and Q channels respectively 000 = NRZ-L unchanged 001 = NRZ-L to NRZ_M 010 = NRZ-L to NRZ_S
MOD_CONTROL(15:0)	bit 0: spectrum inversion enabled (1) or not (0) bit 1: BPSK (0) vs SQPN(1) bit 2: dual source (0), or identical data on I/Q (1) bits 3-5: biphase or NRZ decoding 000: NRZ-L 001: NRZ-M ..010: NRZ-S 100: Biphase-L bit 6: (1) when 1/2 symbol delay added on Q bit bit 7: When enabled, demodulated I and Q data are multiplexed into a single output stream. The symbol rate must be identical on both I and Q channels.

I/Os

General

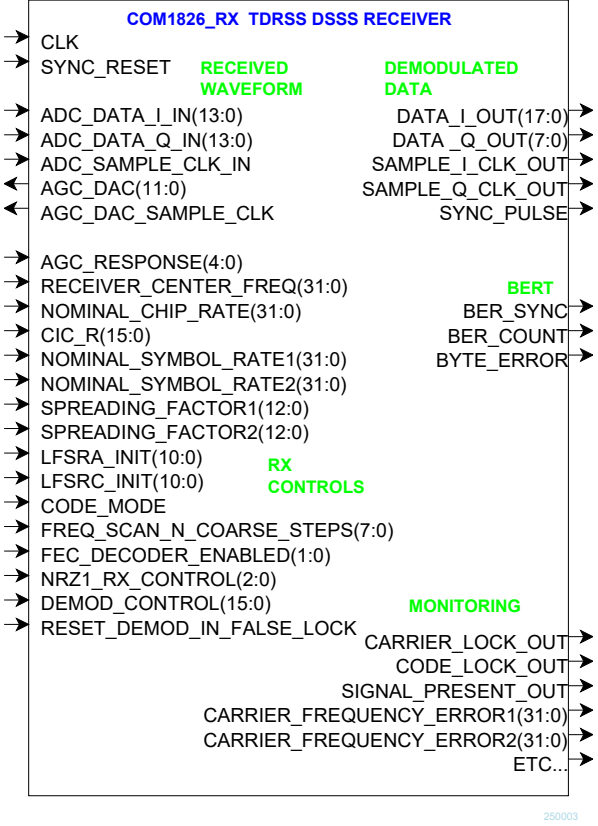
All signals are synchronous with a single input clock **CLK** which also serves as ADC sampling clock for the baseband input waveform.

The clock period must be constrained in the constraint file (.xdc for Xilinx Vivado) associated with the project.

This clock must be global clocks (i.e. use BUFG before supplying the clock to the transmitter).

A synchronous reset **SYNC_RESET** must be supplied. The recommended use is to keep the reset high until the input clock is stable (i.e. PLL or MMCM locked).

Receiver



Data Path

ADC_DATA_I_IN(13:0)
ADC_DATA_Q_IN(13:0)
input ADC samples, in-phase(I) and quadrature (Q)
Use both I and Q in the case of near-zero center frequency input signal
Use I only (force Q to zero) in the case of IF input signal, IF undersampling for example.
Samples are read at the rising edge of the ADC sampling clock CLK when the valid signal **ADC_SAMPLE_CLK_IN** is high.
In the case of lower precision ADCs, align the samples to the left (MSb) and fill the least significant bits with zeros.

After undergoing demodulation, error correction and NRZ conversion, the bits are packed into Bytes, Msb first.
DATA_I_OUT(7:0)
DATA_Q_OUT(7:0)
Read the data at the rising edge of CLK when the associated valid signal **SAMPLE_x_CLK_OUT** is high.
Two output formats are selected by **DEMOD_CONTROL(9)**:
4-bit soft-quantized, or
8 demodulated bits packed in a byte hard-quantization

Operations

Spreading codes

The demodulator is designed to acquire two types of Gold codes:

- All forward command link codes (1023-chip Gold codes)
- All return mode 2 link codes (2047-chip Gold codes)

The Gold codes selection is performed by entering 10 or 11-bit initialization vectors for the linear feedback shift registers. Appendix A of document 451-PN CODE-SNIP lists these initialization vectors as ‘I-code’ and ‘Q-code”.

For example, NASA return mode 2 link code 40 is selected by entering 2225o (octal) and 1337o in the appropriate control registers.

Symbol Rate

The demodulation symbol rates on the I and Q channels are independent of the chip rate and code period. The demodulator includes two autonomous symbol tracking loops, separate from the code tracking loop.

However, the full spread-spectrum processing gain can only be achieved if the symbol period is less than the 2047-chip code period.

Frequency Tracking

The DSSS demodulator is capable of acquiring signals with a maximum center frequency error of +/- 5 KHz remaining after fixed and dynamic (frequency profile table) compensation.

Two features assist the demodulator in extending this natural frequency acquisition range:

1. a fixed user-defined frequency offset, **RECEIVER_CENTER_FREQ(31:0)** is applied to the received signal.
2. a frequency profile table can be sent to the receiver. It consists of a start time followed by 32-bit frequency offset samples read at 1 second intervals. To prevent sudden frequency jumps, the table entries are interpolated linearly.

Once the demodulator has confirmed carrier and code lock, the above frequency offsets are frozen. Once locked, the carrier tracking loops tracks the carrier phase over a very wide frequency range.

Frequency profile table

Users can declare the expected Doppler variation with time in the form of a frequency profile table. The Doppler is used to correct the demodulator expected center frequency. It is also used to correct the demodulator expected chip rate, after scaling the frequency by the 3.0777995 Mchips/s / 2.2875 GHz frequency ratio.

The table is entered in one TCP session whereby the user (TCP client) opens a TCP connection to port 1024 and writes the entire frequency table. The table consists of a 64-bit start time (same reference as the SDDS time tag, i.e. 250ps units) followed by up to 4096 32-bit frequency samples. Each sample represents a nominal center frequency expressed in units of 125 MHz / 2^{32} (about 29 mHz steps), sampled at 1s intervals.

The byte order is MSB first.

The frequency table is read (played-back) every second starting at the specified SDDS start time. The receiver interpolates linearly 64x between successive 1s samples so as to minimize discontinuities. This ensures phase and frequency continuity. This frequency bias is removed from the SDDS input samples for the playback duration, irrespective of the demodulator lock status.

Table playback is mutually exclusive with table upload. Opening a new TCP session to upload a new table will immediately stop any playback in progress.

Because the table is quite small (131Kbits max), the TCP upload time (2-5ms) is insignificant relative to the playback duration.

Code Tracking Loop

The code tracking loop is a coherent delay lock loop (DLL) of the 1st order.

Code Acquisition

120 parallel detectors search for code aligment during the code acquisition phase. During the subsequent code tracking phase, 3 detectors track the early/center/late code while the other 117 detectors scan for false lock. The detectors are staggered ½ chip apart.

Detection is performed in two steps: first a coherent detector averages the despread signal over ½ a symbol period. The result is squared and further averaged over 100 symbols.

The received chip rate must be within +/- 4ppm of the nominal 3.077799479166 Mchips/s value.

Demodulated data output

Demodulated data is encapsulated within variable-length UDP frames and send to the specified destination IP/Port.

The output format is as follows:

- fixed-length preamble consisting of (in the order of transmission)

  - 2-byte length of payload data (excluding preamble). In the range 1 to 1024 bytes.

  - 2-byte frame counter, modulo 2^{16}

  - 4-byte currently undefined

  - 8-byte timestamp (last timestamp read from the SDDS input frames, latched at the first demodulated byte in the transmit frame).

The output frames are sent when one of two trigger conditions is met:

- at least 1024 demodulated data bytes are waiting in the transmit queue, or

- at least 0.5second has elapsed since the last output frame and at least one demodulated data byte is waiting in the transmit queue.

The payload data size is thus variable in the range 1 through 1024 bytes.

Bytes are packed MSb first. Only full bytes are transmitted (no partially filled bytes).

Software Licensing

This software is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bit stream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from
http://www.comblock.com/download/softwarelicense.pdf

Portability

The VHDL source code is written in generic VHDL and thus can be ported FPGAs from various vendors.

Configuration Management

The current software revision is 070625.

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code,.pkg packages, .xdc constraint files (Xilinx) One component per file.
/sim	VHDL test benches
/matlab	Matlab .m program generating stimulus files for VHDL simulation and for end-to-end BER performance analysis at various signal to noise ratios

Project files:

Xilinx Vivado v2020 project files:
project_1/project_1rxvivado2020.xpr
project_1/project_1rxvivado2020.tcl

VHDL development environment

The VHDL software was developed using the following development environment:
Xilinx Vivado 2020 for synthesis, place and route and VHDL simulation

Device Utilization Summary

Receiver device utilization
Device: Xilinx xc7a100tfgg484-1

Resource	Estimation	Available	Utilization...
LUT	39583	63400	62.43
LUTRAM	36	19000	0.19
FF	43246	126800	34.11
BRAM	13	135	9.63
DSP	46	240	19.17
IO	608	285	213.33
BUFG	1	32	3.13

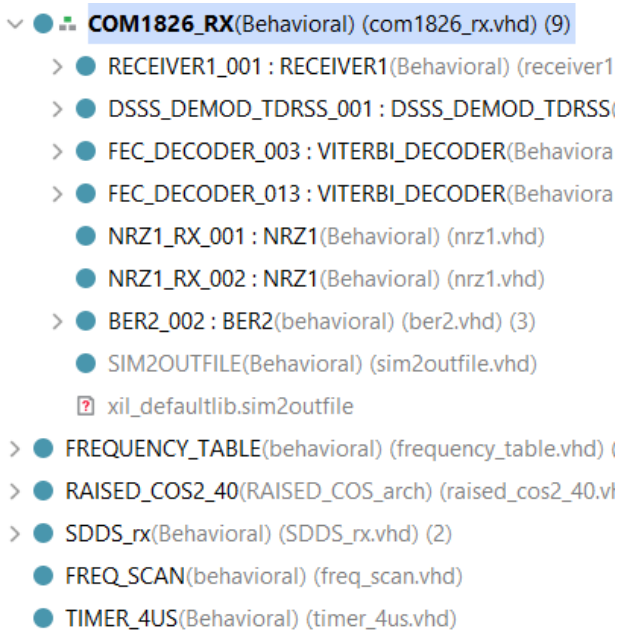
Clock and decoding speed

The entire design is synchronous with the CLK input clock (must be a global clock). A low speed grade Artix7 is sufficient.
Typical maximum clock frequencies for representative FPGA families are listed below:

Device family	**Transmitter**
AMD Artix7 200T -1 speed grade	145.8 MHz
AMD Kintex7 ultrascale+ -1 speed grade	316 MHz

VHDL components overview

Top level



COM1826_RX.vhd is the receiver top level component.

The input waveform can stem directly from ADCs (as complex baseband signals, or IF undersampling signal).

Alternatively, the receiver can process the input waveform formatted as NASA/SDDS on an GbE Ethernet LAN using the *SDDS_RX.vhd* component.

During simulation, the receiver can read and process waveform files using the *INFILE2SIM.vhd* component. See the receiver testbench `tbcom1826_rx.vhd`.

RECEIVER1.vhd is the front-end digital receiver, including AGC, frequency translation to baseband, variable decimation (cic), one half-band filter for image rejection. It is a generic signal processing component which does not depend on the modulation type.

The DSSS_DEMOD_TDRSS.vhd component performs TDRSS spread-spectrum demodulation

FIRHALFBAND3.vhd are half-band interpolation filters used to double the sampling rate. Implemented as a 20-tap FIR filter.

FIRRCOS20.vhd is a 20-tap root raised cosine filter operating at 2 samples/chip. It is currently commented out to minimize despreading losses but can be easily re-instated if adjacent channel interference becomes a problem.

The *FREQUENCY_TABLE.vhd* component can be used to store the dynamic profile of the receiver frequency based on known orbital information. The table is played back at 1/64s increments to adjust the nominal center frequency. The chip rate is also corrected proportionally.

The *VITERBI_DECODER.vhd* component performs Viterbi error correction decoding. Two such components can be used for the I and Q channel independently.

The *NRZ1.vhd* component is useful in converting NRZ-M/L/S formats to NRZ-M/L/S.

Ancillary components

BRAM_DP2x.vhd is a generic dual-port memory, used as input and output elastic buffers. Memory is inferred (no Xilinx primitive is used).

SDDS_rx.vhd received a sampled IF input waveform over a GbE LAN using the UDP-IP protocol. The input UDP stream is formatted according to the NASA/SDDS specifications.

BER2.vhd is a bit error rate tester expecting to receive a PRBS11 test sequence. It synchronizes with the received bit stream and count errors over a 80,000 bit window.

INFILE2SIM.vhd reads an input file (sampled waveform) to test the receiver. This component is used by the receiver testbench `tbcom1826_rx.vhd`

SIM2OUTFILE.vhd writes three 12-bit data variables to a tab delimited file which can be subsequently read by Matlab (load command) for plotting or analysis.

VHDL simulation

VHDL testbenches are located in the /sim directory.

The `/sim/tbcom1826_rx.vhd` reads an input complex waveform file and sends it to the receiver for TDRSS spread-spectrum demodulation, error correction and NRZ conversion. It can also measure the BER when the transmitted payload data is a PRBS11 test sequence.

Matlab simulation

Matlab files are located in the /matlab directory.

The `siggen_tdrss.m` is a matlab program to generate a TDRSS spread-spectrum modulation waveform, saved into a file which can serve as a stimulus input to a receiver. It is functionally equivalent to the `tbcom1826_tx.vhd` VHDL testbed.

Reference documents

[1]] Space Network Users Guide; Rev 10

Acronyms

Acronym	Definition
ADC	Analog to Digital Converter
AWGN	Additive White Gaussian Noise
CTS	Clear-To-Send flow control flag
DAS	Demand Access System
DSSS	Direct Sequence Spread Spectrum (modulation)
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
IF	Intermediate Frequency
IP	Internet Protocol
LFSR	Linear Feedback Shift Register
LSb	Least Significant bit in a word
MSb	Most Significant bit in a word
RF	Radio Frequency
rx	Receive
SDDS	Signal Data Distribution Standard
SQPN	Staggered Quadriphase PN (spread-spectrum modulation)
SRRC	Square Root Raised Cosine (filter)
TDRSS	Tracking and Data Relay Satellite System
tx	Transmit
UDP	User Datagram Protocol

ComBlock Ordering Information

COM-1826SOFT_RX TDRSS DSSS receiver, VHDL source code / IP core

ECCN: EAR99

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