COM-1826 TDRSS SPREAD-SPECTRUM MODEM

Key Features

- TDRSS spread-spectrum modem comprising
  - Demodulator with two input types: GbE LAN/SDDS-formatted input stream or RF input.
  - Modulator with baseband or RF output.
- BPSK and SQPN spread-spectrum modulation
- Convolutional/Viterbi error correction: K=7 Rate ½
- Programmable 1023- (forward command link) or 2047-chip (return mode 2 link) periodic I and Q Gold codes
- Programmable bit rates from 1 to 150 Kbits/s on each channel. Two independent bit synchronizers to acquire and track each channel bit stream.
- 120-bin parallel code search for fast code acquisition. False code lock prevention.
- Built-in Bit Error Rate measurement for PRBS-11 test sequences.
- Demodulation performances: within 1.5 dB from theory at threshold Eb/No of 2 dB.
- Demodulated bits encapsulated in UDP frames and sent out to the LAN. Support for IGMPv2 multicast addressing.
- Monitoring:
  - Receiver lock, Carrier frequency error, SNR
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- 90VAC – 264VAC power supply
- Options:
  - 1-3 receivers per 1 RU chassis
  - Modulator with RF output
  - Demodulator RF input

For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com1826.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

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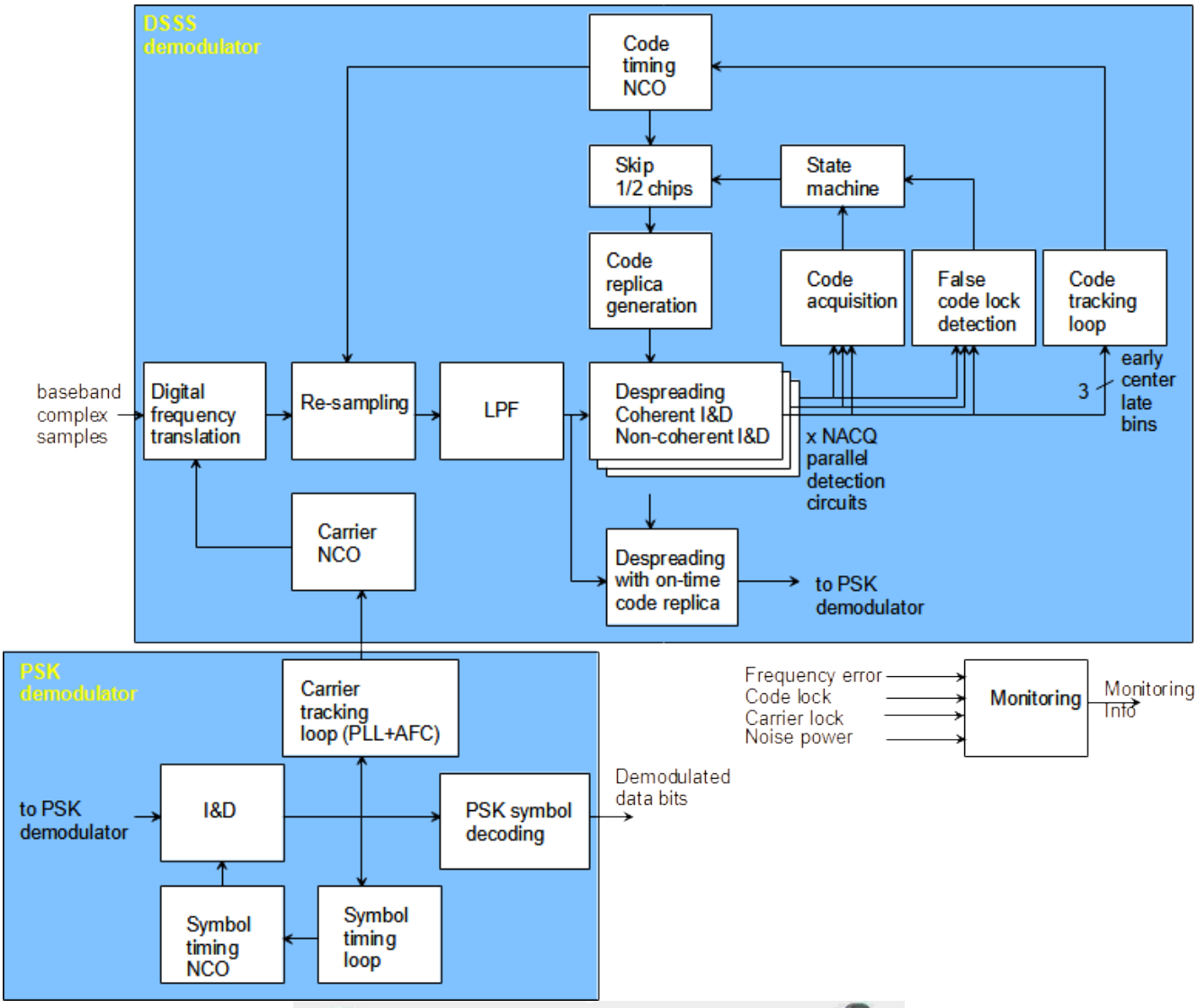
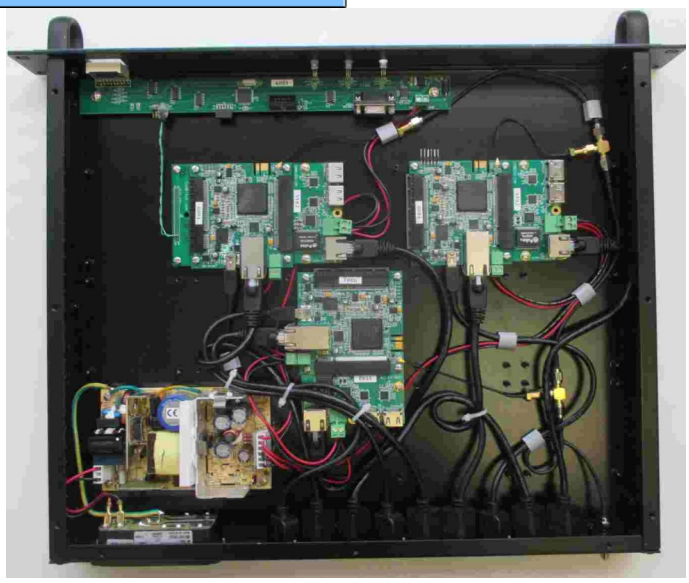
Block Diagram





3-channel receiver

Configuration

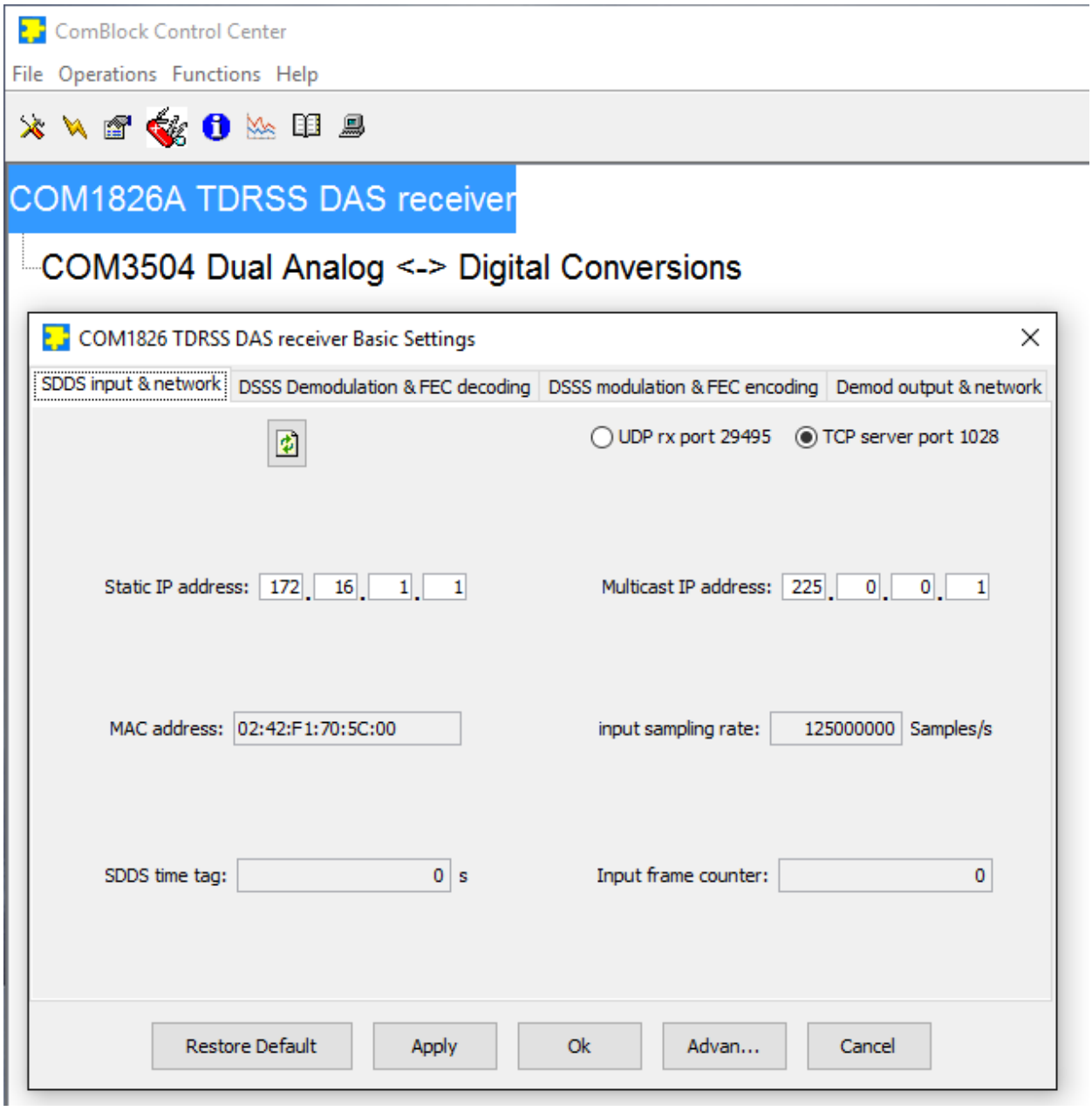
This ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

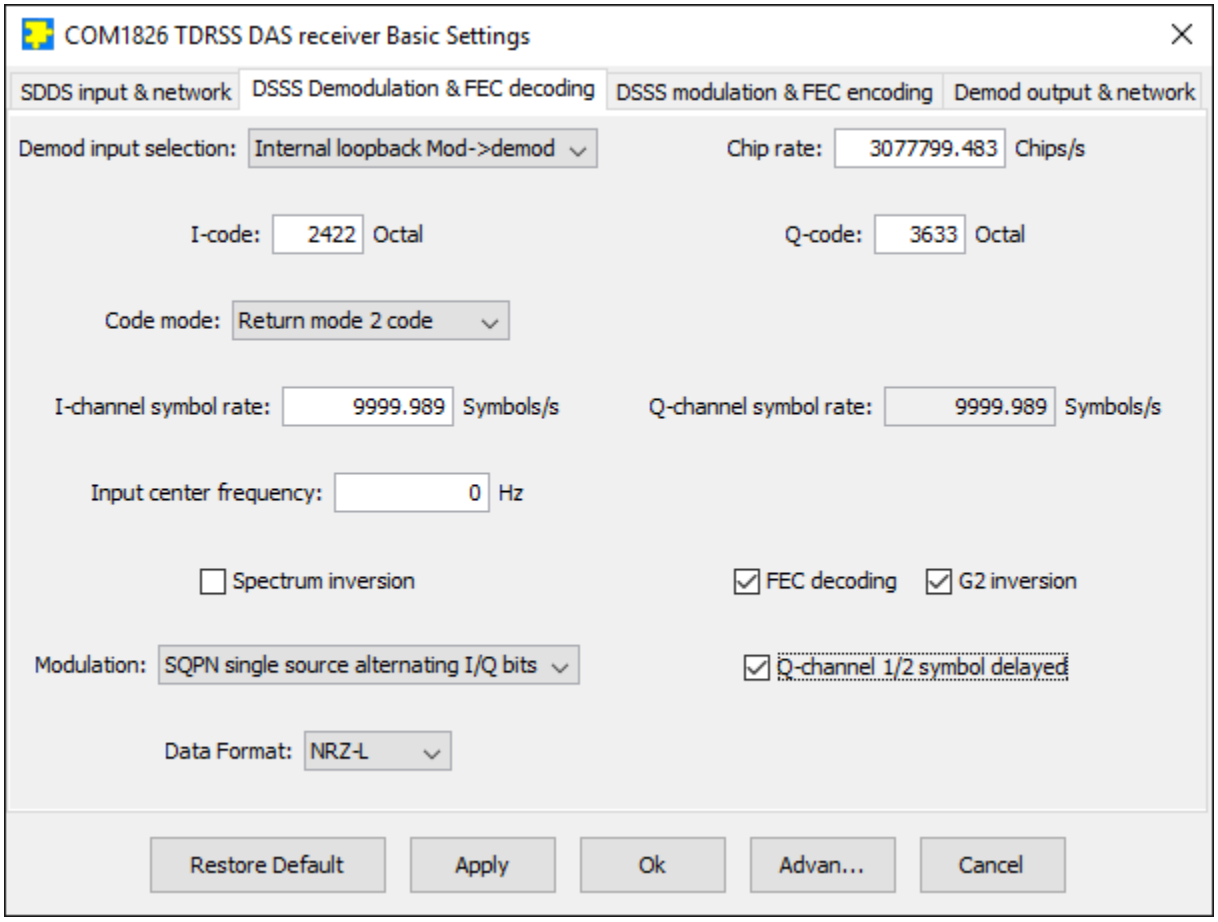
- USB
- TCP-IP/LAN

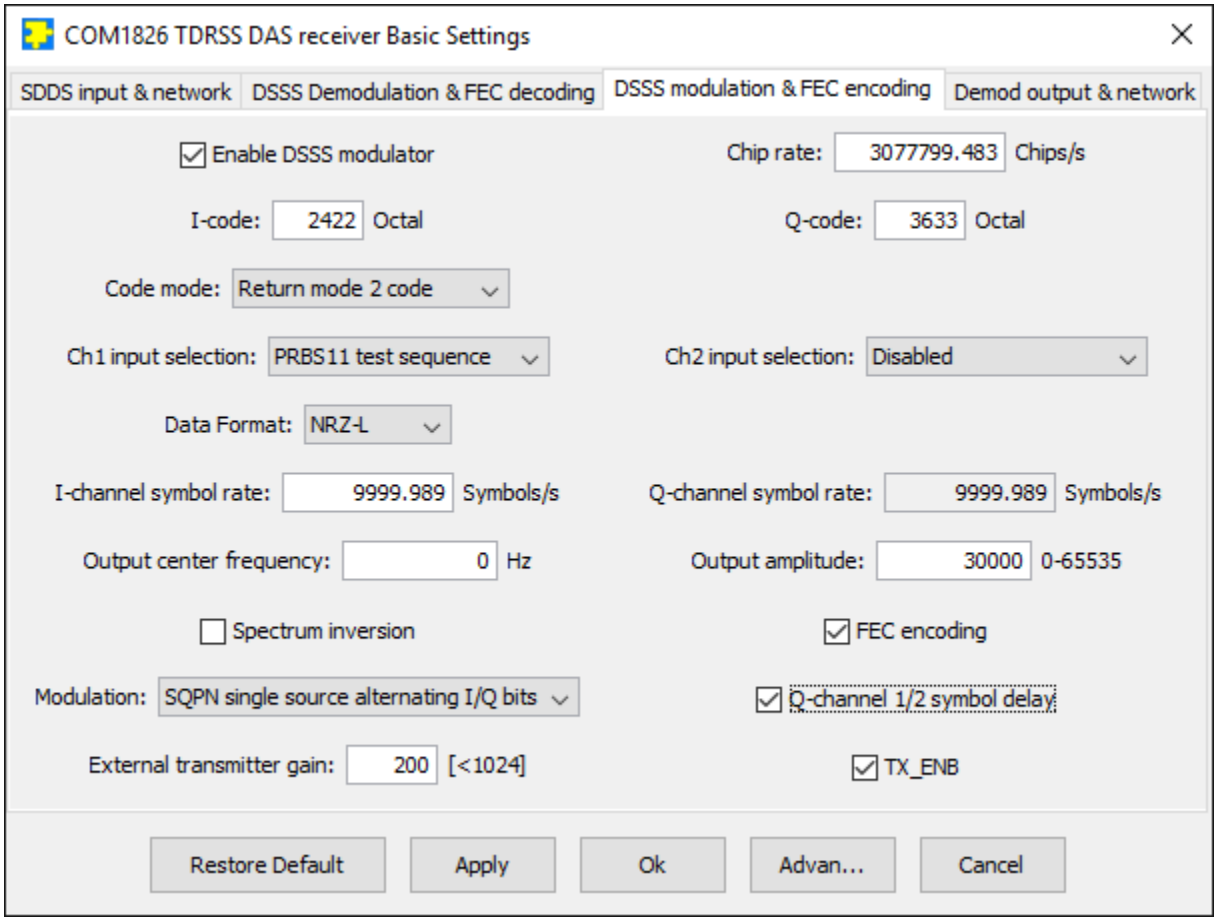
The module configuration is stored in non-volatile memory.

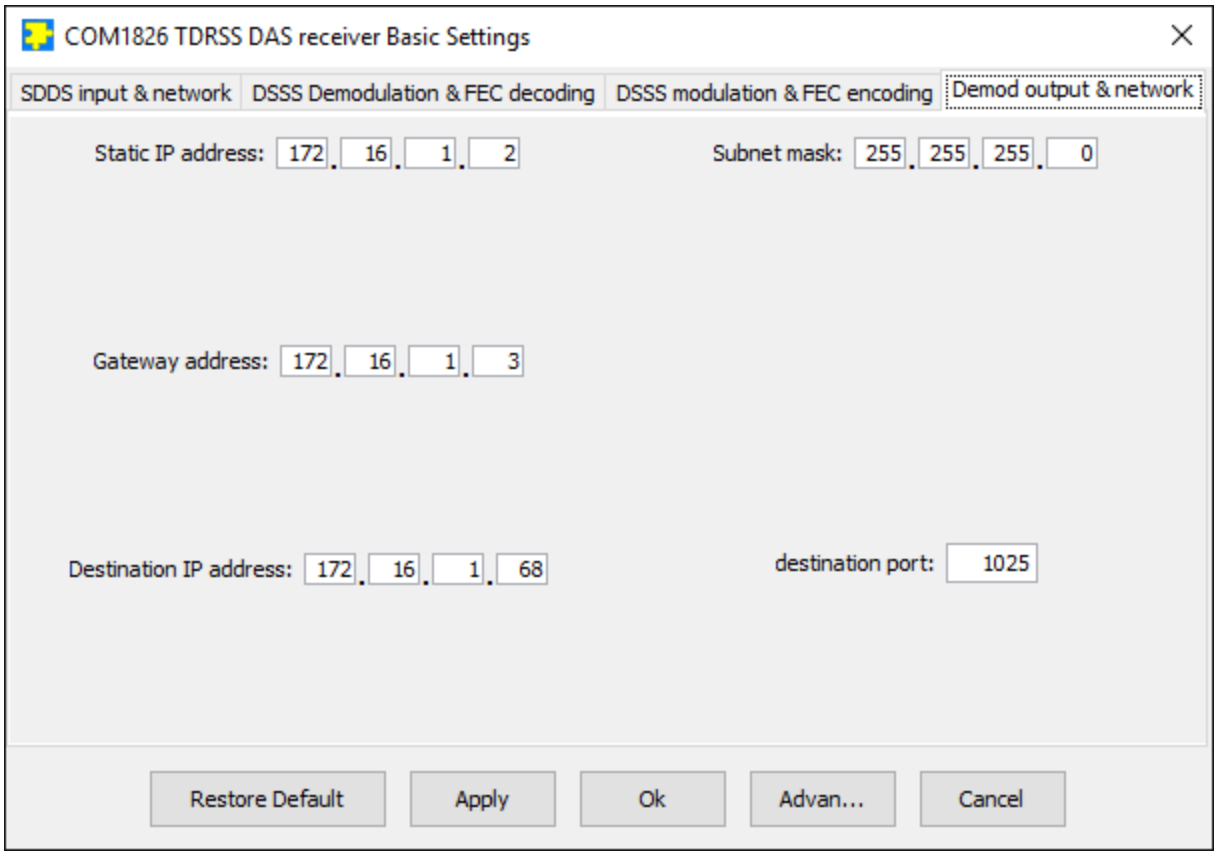
Configuration (Basic)

The easiest way to configure the COM-1826 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1826 module to be configured, next click the *Settings* button to display the *Settings* window shown below.




COM1826 TDRSS DAS receiver Basic Settings
SDDS input & network
DSSS Demodulation & FEC decoding
DSSS modulation & FEC encoding
Demod output & network
Demod input selection:
Internal loopback Mod->demod
Chip rate:
3077799.483
Chips/s
I-code:
2422
Octal
Q-code:
3633
Octal
Code mode:
Return mode 2 code
I-channel symbol rate:
9999.989
Symbols/s
Q-channel symbol rate:
9999.989
Symbols/s
Input center frequency:
0
Hz
Spectrum inversion
FEC decoding
G2 inversion
Modulation:
SQPN single source alternating I/Q bits
Q-channel 1/2 symbol delayed
Data Format:
NRZ-L
Restore Default
Apply
Ok
Advan...
Cancel


COM1826 TDRSS DAS receiver Basic Settings
SDDS input & network
DSSS Demodulation & FEC decoding
DSSS modulation & FEC encoding
Demod output & network
Enable DSSS modulator
Chip rate: 3077799.483 Chips/s
I-code: 2422 Octal
Q-code: 3633 Octal
Code mode: Return mode 2 code
Ch1 input selection: PRBS11 test sequence
Ch2 input selection: Disabled
Data Format: NRZ-L
I-channel symbol rate: 9999.989 Symbols/s
Q-channel symbol rate: 9999.989 Symbols/s
Output center frequency: 0 Hz
Output amplitude: 30000 0-65535
Spectrum inversion
FEC encoding
Modulation: SQPN single source alternating I/Q bits
Q-channel 1/2 symbol delay
External transmitter gain: 200 [<1024]
TX_ENB
Restore Default
Apply
Ok
Advan...
Cancel


COM1826 TDRSS DAS receiver Basic Settings
SDDS input & network
DSSS Demodulation & FEC decoding
DSSS modulation & FEC encoding
Demod output & network
Static IP address: 172 . 16 . 1 . 2
Subnet mask: 255 . 255 . 255 . 0
Gateway address: 172 . 16 . 1 . 3
Destination IP address: 172 . 16 . 1 . 68
destination port: 1025
Restore Default
Apply
Ok
Advan...
Cancel

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Several key parameters are computed on the basis of the 125 MHz internal processing clock f_{clk_p}: frequency translation, chip rate, etc.

Built-in DSSS demodulator	
Parameters	**Configuration**
SDDS-formatted stream input selection	1 = UDP port 29495 0 = TCP port 1028 REG0(0)
Demod input selection	0 = SDDS / LAN 2 = A/D converters baseband 3 = A/D converters IF undersampling 4 = internal modulator loopback REG28(7:5)
I Code	Linear feedback shift register initialization. As per [1] REG1 LSB REG2(2:0) MSb
Q Code	REG3 LSB REG4(2:0) MSb
Code mode	0 = forward command link 1 = return mode 2 link See SNIP for details REG27(4)
reserved	REG27(7:5) = "000"
CIC_R	Decimation ratio. Largest integer less than input sampling rate / 4*chip rate REG2(7:3): lsbs REG4(7:3): msbs
Chip rate (fchip rate)	The nominal chip rate is 3.077799479166 Mchips/s. However, the design is somewhat more flexible. Alternative chip rates can be entered here 32-bit integer expressed as fchip rate * 2^{32} / f_{clk_p}. The maximum practical chip rate is f_{clk_p} /2. Nominal chip rate: 0x064DA741 The maximum allowed error between transmitted and received chip rate is +/- 100ppm. REG5 (LSB) – REG8 (MSB)
I channel symbol rate f_{symbol_rate}	The I-channel symbol rate can be set independently of the spreading code period as f_{symbol_rate} * 2^{32} / f_{clk_p} Example: "00346DC6" represents 100 Ksymbols/s. REG9 (LSB) – REG12 (MSB)
Q channel symbol rate f_{symbol_rate}	The Q-channel symbol rate can be set independently of the spreading code period as f_{symbol_rate} * 2^{32} / f_{clk_p} REG13 (LSB) – REG16 (MSB)
I channel spreading factor (Processing gain)	Approximate (i.e rounded) ratio of chip rate / symbol rate REG17 (LSB) REG18(4:0) MSb
Q channel spreading factor (Processing gain)	Approximate (i.e rounded) ratio of chip rate / symbol rate REG19 (LSB) REG20(4:0) MSb
Nominal input center frequency (f_c)	The nominal center frequency is a fixed frequency offset applied to the SDDS input samples. It is used for fine frequency corrections, for example to correct clock drifts. 32-bit signed integer (2's complement representation) expressed as f_c * 2^{32} / f_{clk_p} In addition to this fixed value, an optional time-dependent frequency profile can be entered. See frequency profile table. REG21 (LSB) – REG24 (MSB)
Reserved	REG25
Spectrum inversion	Invert Q bit 0 = off 1 = on REG26(0)
BPSK / SQPN	0 = BPSK 1 = SQPN REG26(1)
SQPN single/double source	0 = different data on I and Q channels (including the case when bits of a single input bit stream are sent alternatively to the I/Q channels). Independent symbol rates on I/Q channels. Uses two FEC decoders. 1 = identical data on I and Q channels (prior to coherent sum). Uses one FEC decoder.

	REG26(2)
Alternating I/Q bits	Alternating bits are sent on the I and Q channels. The symbol rate must be identical on both I and Q channels. Two independent FEC decoders are used on the I and Q paths respectively. Enabled(1)/Disabled(0) REG26(7)
½ symbol delay on the Q path	The Q bits received with a ½ symbol delay with respect to the I bits. Enabled(1)/Disabled(0) REG26(6)
Encoding	0 = NRZ-L 1 = NRZ-M 2 = NRZ-S 4 = Biphase-L REG26(5:3)
AGC response time	Users can to optimize AGC response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and chip rate). The AGC_DAC gain control signal is updated as follows 0 = every chip, 1 = every 2 input chips, 2 = every 4 input chips, 3 = every 8 input chips, etc…. 10 = every 1000 input chips. Valid range 0 to 14. REG28(4:0)
Viterbi decoding	Disable (0) / Enable (1) REG27(1)
Viterbi decoder G2 parity bit inversion	No (0) / Yes (1) REG27(2)
Select BER tester input	0 = I, 1 = Q REG27(3)

Built-in DSSS modulator (when instantiated)	
Parameters	**Configuration**
DSSS modulator enable	0 = disabled 1 = enabled REG61(7)
Channel 1 modulator input selection	0 = disabled 1 = TCP server at port 1280 2 = PRBS11 test sequence 3 = zeros REG63(5:4)
Channel 2 modulator input selection	0 = disabled 1 = TCP server at port 1281 2 = PRBS11 test sequence 3 = zeros REG65(5:4)
I Code	Linear feedback shift register initialization. As per [1] REG62 LSB REG63(2:0) MSb
Q Code	REG64 LSB REG65(2:0) MSb
Code mode	0 = forward command link (see SNIP) 1 = return mode 2 link See SNIP for details REG65(3)
Chip rate (fchip rate)	The nominal chip rate is 3.077799479166 Mchips/s. However, the design is somewhat more flexible. Alternative chip rates can be entered here 32-bit integer expressed as fchip rate * 2^{32} / f_{clk_p}. The maximum practical chip rate is f_{clk_p} /2. Nominal chip rate: 0x064DA730 REG66 (LSB) – REG69 (MSB)
I channel symbol rate f_{symbol_rate}	The I-channel symbol rate can be set independently of the spreading code period as f_{symbol_rate} * 2^{32} / f_{clk_p} Example: 0x0346DC5 represents 100 Ksymbols/s. REG70 (LSB) – REG73 (MSB)
Q channel symbol rate f_{symbol_rate}	The Q-channel symbol rate can be set independently of the spreading code period as f_{symbol_rate} * 2^{32} / f_{clk_p} REG74(LSB) – REG77 (MSB)

Modulated signal amplitude	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. Saturation can easily be checked by visualizing the input signal using ComScope. REG29 = LSB REG30 = MSB
Output center frequency (f_c)	Fixed frequency offset applied to the output samples. 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk\_p}$ REG81 (LSB) – REG78 (MSB)
Spectrum inversion	Invert Q bit 0 = off 1 = on REG61(0)
BPSK / SQPN	0 = BPSK 1 = SQPN REG61(1)
SQPN single/double source	0 = different data on I and Q channels (including the case when bits of a single input bit stream are sent alternatively to the I/Q channels). Independent symbol rates on I/Q channels. Uses two FEC encoders. 1 = identical data on I and Q channels. Uses one FEC encoder REG61(2)
Alternating I/Q bits	When enabled, the input data stream is demultiplexed into the I and Q paths. The symbol rate must be identical on both I and Q channels. Two independent FEC encoders are used on the I and Q paths respectively. Enabled(1)/Disabled(0) REG60(7)
½ symbol delay on the Q path	A ½ symbol delay can be added to the Q modulator path Enabled(1)/Disabled(0) REG60(6)
Data format converter	Data format conversion from the NRZ-L input to NRZ-L/M/S format prior to the FEC encoder. 0 = NRZ-L to NRZ-L 1 = NRZ-L to NRZ-M 2 = NRZ-L to NRZ-S REG61(5:3)
Convolutional FEC encoding	Disable (0) / Enable (1) REG61(6)

Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation when changing this parameter. Saturation can easily be checked by visualizing the input signal using ComScope. REG31 = LSB REG32 = MSB
External transmitter gain control	When using an external transceiver such as the COM-350x family, the transmitter gain can be controlled through the TX_GAIN_CNTRL1 analog output signal. Range 0 – 3.3V. REG59: LSB, REG60(3:0): MSb
TX_ENB control	The TX_ENB signal at the interface controls the RF transmit circuit. 0 = off 1 = on REG60(4)
Network Interface	
Parameters	**Configuration**
MAC addresses LSB	In order to ensure the uniqueness of MAC addresses, users can define bits 7:1 through REG236(7:1). The MAC addresses upper bits are automatically tied to the nearly unique FPGA DNA_ID. MAC address bit 0 is either 0 (LAN1) or 1 (LAN2). REG236(7:1).
IP1 multicast address (LAN xB connector on backpanel)	4-byte IPv4 address used for SDDS input stream. Example : 0x E1 00 00 01 designates address 225.0.0.1 Use 0.0.0.0 to signify that multicasting is not supported. REG33 (MSB) – REG36 (LSB)
IP1 static address (LAN xB connector on backpanel)	4-byte IPv4 address used for SDDS input stream. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG37 (MSB) - REG40 (LSB)
IP2 address (LAN xA connector on backpanel)	4-byte IPv4 address used for receiver output, modulator inputs and monitoring and control. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG41 (MSB) - REG44 (LSB)
Destination IP address	4-byte IPv4 address Destination IP address for UDP frames

	with decoded data. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG45 (MSB) – REG48(LSB)
Destination ports	I-channel data is routed to this user-defined port number: REG49(LSB) – REG50(MSB) Q-channel data is routed to the incremented port number.
Subnet mask	REG51 (MSB) – REG54(LSB)
Gateway IP address	REG55 (MSB) – REG58(LSB)

(Re-)Writing to the last control register REG81 is recommended after a configuration change to enact the change.

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-9 Properly operating hardware will result in the following sequence being displayed: SREG0-SREG9 = 01 F1 1D xx 1F 93 10 22 22 03
TCXO reference clock presence	1 = detected 0 = missing SREG9(0)
125 MHz internal clock PLL lock	Indirectly confirms the presence of the frequency reference (TCXO for firmware options –A/C, external 10 MHz for firmware options –B/D) 1 = locked 0 = unlocked SREG9(1)
Input sampling rate	The sampling rate, as read from the SDDS input stream. Format: sampling_rate/fclk *2^32 SREG10 = bit 7-0 (LSB) SREG11 = bit 15 – 8 SREG12 = bit 23 – 16 SREG13(3:0) = bit 27 – 24 (MSB)
Time tag	Last valid timetag read from the SDDS input header. Expressed in 250ps units. SREG14 (LSB) – SREG21(MSB)
Input frame counter	Cumulative SDDS frame counter. Each frame contains 1024 bytes = 256 complex samples. SREG22 (LSB) – SREG25(MSB)
Missing input frame counter	Cumulative number of missing SDDS frames. Should be zero. SREG26 (LSB) – SREG27(MSB)
LAN1 MAC bad CRC counter	SREG28 (LSB) – SREG29(MSB)
MAC address	Unique 48-bit hardware address (802.3). In the form SREG30:SREG31:SREG32:….:SREG35
Demodulator carrier lock status	SREG36(0) 0 = unlocked or no input 1 = locked
Code lock status	SREG36(1) 0 = unlocked or no input 1 = locked (1 s hysteresis)
Viterbi decoder1 synchronized	SREG36(2) 0 = not synchronized or no input 1 = synchronized

Viterbi decoder2 synchronized	SREG36(3) 0 = not synchronized or no input 1 = synchronized
Signal presence	SREG36(4) 0 = no carrier detected in FFT 1 = carrier detected in FFT
Decoder1 built-in BER	The Viterbi decoder computes the BER on the received (encoded) data stream irrespective of the transmitted bit stream. Encoded stream bit errors detected over a 1000-bit measurement window. SREG37 LSB SREG38 MSB
Decoder2 built-in BER	The Viterbi decoder computes the BER on the received (encoded) data stream irrespective of the transmitted bit stream. Encoded stream bit errors detected over a 1000-bit measurement window. SREG39 LSB SREG40 MSB
Nominal center frequency	Expected center frequency: sum of the fixed center frequency and the dynamic frequency profile table. SREG41 (LSB) – SREG44 (MSB)
Carrier frequency offset1	Residual frequency offset with respect to the nominal carrier frequency (i.e. after frequency profile correction). Part 1/2. 32-bit signed integer expressed as fcerror * * 2^{32} / f_{clk_p} SREG45 (LSB) – SREG48 (MSB)
Carrier frequency offset2	Residual frequency offset with respect to the nominal carrier frequency (i.e. after frequency profile correction). Part 2/2. 32-bit signed integer expressed as fcerror * * 2^{31} / f_{chip_rate} SREG49 (LSB) – SREG52 (MSB)
Despread signal power S	Average signal power after despreading. Compute the signal to noise ratio after despreading as S/N. The absolute value is meaningless because of multiple agcs. SREG53 (LSB) – SREG54 (MSB)
Noise power N	Average noise power. Used to compute the SNR after despreading. The absolute value is meaningless because of multiple agcs. SREG55 (LSB) – SREG56 (MSB)
SNR	2*(S+N)/N ratio, valid only during code lock. Linear (not in dBs) Fixed point format 14.2 SREG57 (LSB) – SREG58 (MSB)

Bit error rate	Monitors the BER (number of bit errors on the I- or Q-channel at the demodulator output, counted over 80,000 received bits) when the modulator is sending a PRBS-11 test sequence. Note: because the demodulator inherent phase ambiguity, a zero BER can be displayed as 0 or 80000 (x13880) SREG59: LSB SREG60: MSB
BER tester synchronized	SREG36(5): 1 when the BER tester is synchronized with the received PRBS-11 test sequence.
Built-in modulator SNR calibration	
Parameters	**Monitoring**
Measured modulated signal power	SREG61(LSB) SREG62 SREG63(MSB)
Measured AWGN power (Noise bandwidth is 6.25 MHz)	SREG64(LSB) SREG65 SREG66(MSB)
FPGA configuration options	
Parameters	**Monitoring**
MODULATOR_EN	Indicates whether the modulator is instantiated (1) or not (0) in the current active FPGA configuration. SREG67(0)
ADCs_EN	Demodulator ADC interface instantiated (1) or not (0) SREG67(1)
DACs_EN	Modulator DAC interface instantiated (1) or not (0) SREG67(2)
AWGN_EN	Additive white Gaussian noise instantiated (1) or not (0) SREG67(3)
DEMODULATOR_EN	Indicates whether the demodulator is instantiated (1) or not (0) in the current active FPGA configuration. SREG67(4)

Multi-byte status variables are latched upon (re-)reading SREG7.

ComScope Monitoring

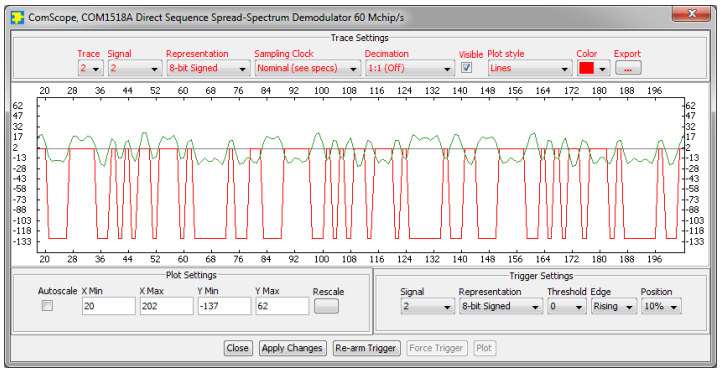
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. Click on the button to start, then select the signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input signal I-channel	8-bit signed	Input sampling rate	512
2: Demodulated Q-channel	8-bit signed	1 sample / symbol	512
3: Parallel correlator output	8-bit unsigned	1 sample/code epoch	512
4: 2(S+N)/N after despreading. Valid only if code is locked. Linear (i.e. not in dBs)	8-bit unsigned	f_{clk}	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input signal Q-channel	8-bit signed	Input sampling rate	512
2: Code replica. Compare with spread input signals	8-bit signed	2 samples/chip	512
3: Demodulated I-channel	8-bit signed	1 sample / symbol	512
4: Averaged signal power (valid only during code tracking)	8-bit signed	f_{clk}	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Code tracking phase correction (accumulated)	8-bit signed	2 samples / symbol	512
2: Carrier fine tracking phase	8-bit signed	f_{clk}	512
3: I-Symbol tracking phase (accumulated)	8-bit signed	1 sample / symbol	512
4: Averaged noise power (valid only during code tracking)	8-bit signed	f_{clk}	512
Trigger Signal	**Format**		
1: Start of code replica	Binary		
2. Code Lock	Binary		

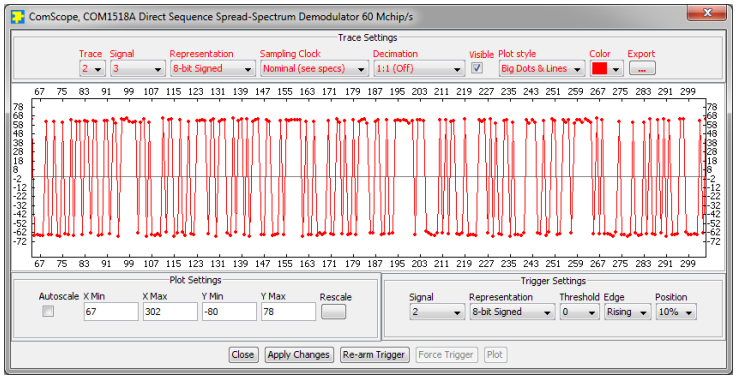
Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk} processing clock as real-time sampling clock.

In particular, selecting the f_{clk} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



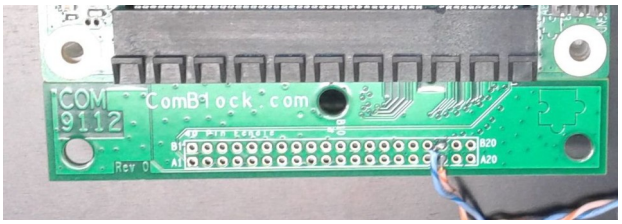
ComScope example, showing code lock with aligned: received spread signal (green) vs code replica (red)



ComScope example: showing demodulated I-channel

Digital Test Points

The digital test points below are only available when no ADCs/DACs are installed.



Test Point	Definition
A1	UDP/TCP input data activity. SDDS receive data valid flag from UDP or TCP. (8ns per input byte)
A2	SDDS input buffer underflow condition. '1' when the sender is not fast enough.
A3	Recovered carrier/center frequency (coarse)
A4	Carrier lock
A5	Code lock
A6	Signal present
A7	Recovered chip clock
A8	Recovered I-channel symbol clock
A9	I-code start
A10	I-code replica
A11	I-channel before despreading (compare with code replica)
A12	Demodulated bit (I)
A13	Demodulated bit (Q)
A14	BER tester synchronized (I or Q depending on REG27(3))
A15	Byte error detected by BER tester (I or Q depending on REG27(3))
A16	Viterbi decoder (I) synchronized (pulse every 1K bits)
A17	Viterbi decoder (Q) synchronized (pulse every 1K bits)
A19	Periodic pulses every 2047 bits when receiving a PRBS-11 test sequence

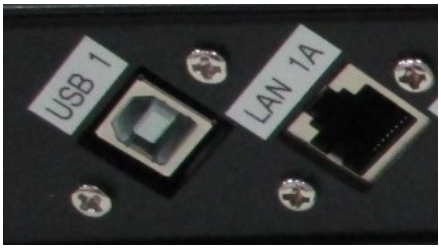
Operation

Monitoring & Control

M&C is possible over USB and LAN/TCP.

A pre-requisite for using USB is the prior installation of the ComBlock USB driver.

Monitoring and control is through the USB and LAN xA connectors on the back panel.



At manufacturing, the default M&C LAN address is 172.16.1.2. It can be subsequently changed via USB or LAN/TCP.

The LAN xA connector is also shared with TCP connections for modulator inputs and dynamic profiles inputs.

SDDS input stream

The LAN xB connectors on the back panel are reserved for SDDS-formatted input streams.

The input stream can be received on UDP port 29495 or TCP-IP port 1028. Control register REG0(0) selects UDP versus TCP.

The static IP address is defined in control registers REG37-40.

Note: It is important to ensure that the data source is fast enough to send 200 Mbits/s of UDP or TCP data with latency less than 2.5ms (the receiver input elastic buffer depth). When in doubt, please check the test point A2 with an oscilloscope.

The input sampling rate is read from the SDDS preamble. The receiver design was verified at an input sampling rate of 6.25 MSamples/s, but the design should work similarly at other sampling rates.

The 64-bit receiver time is read from each SDDS frame preamble. It is used to time-tag the output frames containing the demodulated bits.

External frequency reference

A 10 MHz external frequency reference is required for proper operation. The electrical characteristics are as follows:

Sinewave, clipped sinewave or squarewave. AC-coupled.

Minimum level: 2Vpp.
Maximum level: 5Vpp.

When the SDDS input stream is transmitted as UDP, it is essential that the same 10 MHz be used at both ends of the UDP link, otherwise buffer underflow or overflow conditions may occur.

When the SDDS input stream is transmitted as TCP, the 10 MHz frequency stability requirements are not as stringent as the TCP protocol informs the data source of flow-control conditions at the data sink. In this case, the data source is responsible for timing adjustments in the data throughput.

Modulator input stream

The modulator has two independent external inputs for the I and Q channels. Inputs are through the LAN xA connectors on the back panel.

Two TCP servers await connections from remote TCP clients on ports 1280 and 1281 for the I and Q channels respectively.

The TCP clients must send input data as fast as allowed by the TCP flow control in order to prevent an underflow condition at the modulator.

Spreading codes

The demodulator is designed to acquire two types of Gold codes:

- All forward command link codes (1023-chip Gold codes)
- All return mode 2 link codes (2047-chip Gold codes)

The Gold codes selection is performed by entering 10 or 11-bit initialization vectors for the linear feedback shift registers. Appendix A of document 451-PN CODE-SNIP lists these initialization vectors as ‘I-code’ and ‘Q-code”.

For example, NASA return mode 2 link code 40 is selected by entering 2225o (octal) and 1337o in the appropriate control registers.

Symbol Rate

The demodulation symbol rates on the I and Q channels are independent of the chip rate and code period. The demodulator includes two autonomous symbol tracking loops, separate from the code tracking loop.

However, the full spread-spectrum processing gain can only be achieved if the symbol period is less than the 2047-chip code period.

Frequency Tracking

The DSSS demodulator is capable of acquiring signals with a maximum center frequency error of +/- 5 KHz remaining after fixed and dynamic (frequency profile table) compensation.

Two features assist the demodulator in extending this natural frequency acquisition range:

1. a fixed user-defined frequency offset, entered through the GUI, is applied to the received signal.

2. a frequency profile table can be sent to the receiver. It consists of a start time followed by 32-bit frequency offset samples read at 1 second intervals. To prevent sudden frequency jumps, the table entries are interpolated linearly.

Once the demodulator has confirmed carrier and code lock, the above frequency offsets are frozen. Once locked, the carrier tracking loops tracks the carrier phase over a very wide frequency range.

Frequency profile table

Users can declare the expected Doppler variation with time in the form of a frequency profile table. The Doppler is used to correct the demodulator expected center frequency. It is also used to correct the demodulator expected chip rate, after scaling the frequency by the 3.0777995 Mchips/s / 2.2875 GHz frequency ratio.

The table is entered in one TCP session whereby the user (TCP client) opens a TCP connection to port 1024 and writes the entire frequency table. The table consists of a 64-bit start time (same reference as the SDDS time tag, i.e. 250ps units) followed by up to 4096 32-bit frequency samples. Each sample represents a nominal center frequency expressed in units of 125 MHz / 2^{32} (about 29 mHz steps), sampled at 1s intervals.

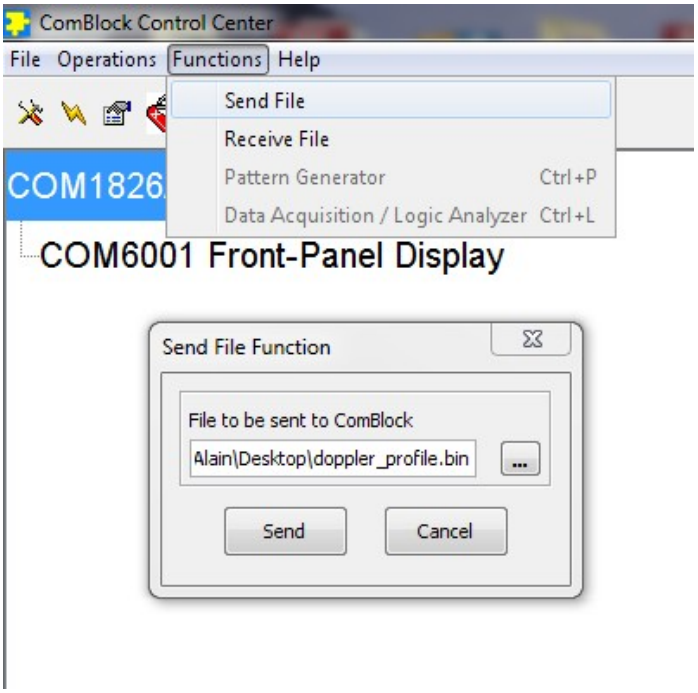
The byte order is MSB first.

The frequency table is read (played-back) every second starting at the specified SDDS start time. The receiver interpolates linearly 64x between successive 1s samples so as to minimize discontinuities. This ensures phase and frequency continuity. This frequency bias is removed from the SDDS input samples for the playback duration, irrespective of the demodulator lock status.

Table playback is mutually exclusive with table upload. Opening a new TCP session to upload a new table will immediately stop any playback in progress.

Because the table is quite small (131Kbits max), the TCP upload time (2-5ms) is insignificant relative to the playback duration.

A utility is included in the ComBlock Control Center to upload a binary frequency profile table:



Code Tracking Loop

The code tracking loop is a coherent delay lock loop (DLL) of the 1st order.

Code Acquisition

120 parallel detectors search for code aligment during the code acquisition phase. During the subsequent code tracking phase, 3 detectors track the early/center/late code while the other 117 detectors scan for false lock. The detectors are staggered ½ chip apart.

Detection is performed in two steps: first a coherent detector averages the despread signal over ½ a symbol period. The result is squared and further averaged over 100 symbols.

The received chip rate must be within +/- 4ppm of the nominal 3.077799479166 Mchips/s value.

Demodulated data output

Demodulated data is encapsulated within variable-length UDP frames and send to the specified destination IP/Port.

The output format is as follows:

- fixed-length preamble consisting of (in the order of transmission)

  - 2-byte length of payload data (excluding preamble). In the range 1 to 1024 bytes.

  - 2-byte frame counter, modulo 2^{16}

  - 4-byte currently undefined

  - 8-byte timestamp (last timestamp read from the SDDS input frames, latched at the first demodulated byte in the transmit frame).

The output frames are sent when one of two trigger conditions is met:

- at least 1024 demodulated data bytes are waiting in the transmit queue, or

- at least 0.5second has elapsed since the last output frame and at least one demodulated data byte is waiting in the transmit queue.

The payload data size is thus variable in the range 1 through 1024 bytes.

Bytes are packed MSb first. Only full bytes are transmitted (no partially filled bytes).

Modulator

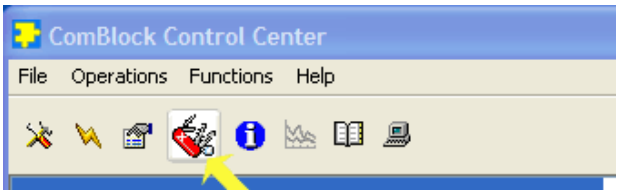
The built-in modulator includes the FEC encoding and DSSS baseband modulation functions. The modulator output can be directed to the internal demodulator when the loopback control is enabled.

Depending on the ordering option, the modulator output can also be directed to analog baseband or RF.

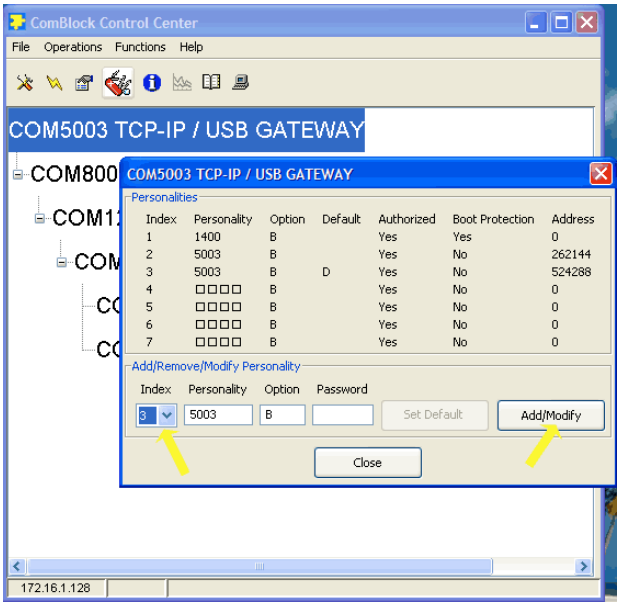
Load Software Updates

From time to time, ComBlock software updates are released.

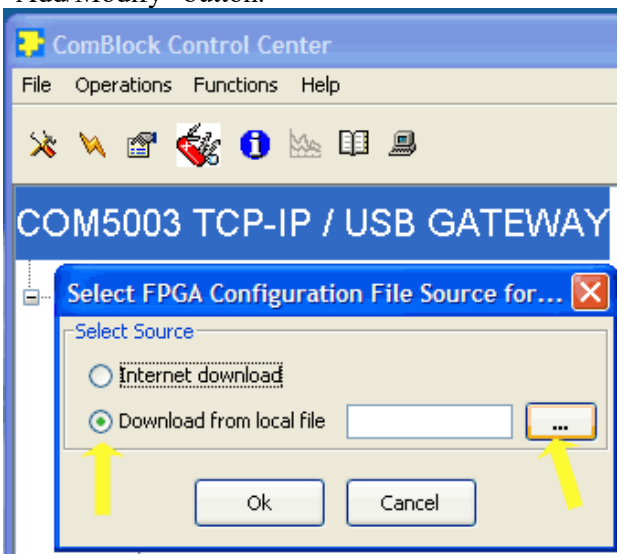
To manually update the software, highlight the ComBlock and click on the Swiss army knife button.



The receiver can store multiple personalities. The list of personalities stored within the ComBlock Flash memory will be shown upon clicking on the Swiss army knife button.



The default personality loaded at power up or after a reboot is identified by a ‘D’ in the Default column. Any unprotected personality can be updated while the Default personality is running. Select the personality index and click on the “Add/Modify” button.



The software configuration files are named with the .bit extension. The bit file can be downloaded via the Internet, from the ComBlock CD or any other local file.

The option and revision for the software currently running within the FPGA are listed at the bottom of the advanced settings window.

The available firmware options are:

-A COM-5102/1826/3504 assembly, internal VCTCXO frequency reference.

-B COM-5102/1826/3504 assembly, external 10 MHz frequency reference.

-C COM-30xx/1826/4009 assembly, internal VCTCXO frequency reference.

-D COM-30xx/1826/4009 assembly, external 10 MHz frequency reference.

Recovery

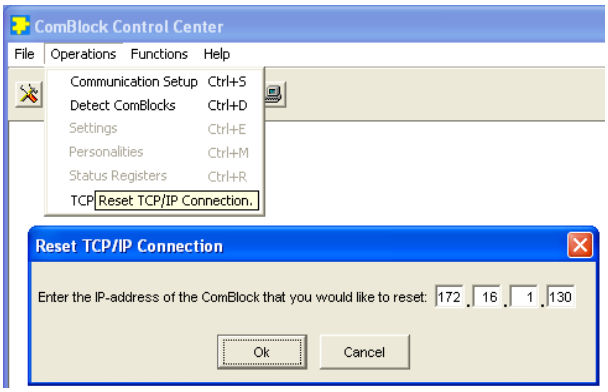
This module is protected against corruption by an invalid FPGA configuration file (during firmware upgrade for example) or an invalid user configuration. To recover from such occurrence, connect a jumper in J3 and during power-up. This prevents the FPGA configuration and restore USB communication [LAN communication is restored only if the IP address is known/defined for the personality index selected as default]. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

UDP Reset

Port 1029 is open as a UDP receive-only port. This port serves a single purpose: being able to reset the modem (and therefore the TCP-IP connection) gracefully. This feature is intended to remedy a common practical problem: it is a common occurrence for one side of a TCP-IP connection to end abnormally without the other side knowing that the connection is broken (for example when a client 'crashes'). In this case, new connections cannot be established without first closing the previous ones. The problem is particularly acute when the COM-1826 is at a remote location.

The command "@001RST<CR><LF>" sent as a UDP packet to this port will reset all TCP-IP connections within the COM-1826.

TCP-IP connections can also be cleared remotely from the ComBlock Control Center as illustrated below:



Troubleshooting Checklist

Receiver is not responsive after power up:

- The device typically takes up to 30 seconds to boot up after power up.
- If still not responsive after 30 seconds, recycle the power. Wait at least 15 seconds after power off to turn the power on again.

Receiver does not communicate with the ComBlock Control Center:

- Make sure an external 10 MHz frequency reference is present prior to powering up the receiver. This applies only when the –B firmware option (external 10 MHz frequency reference) is selected by default.

Demodulator can't achieve lock even at high signal-to-noise ratios:

- Make sure the modulator baseband I/Q signals do not saturate, as such saturation would strongly distort the modulation phase information. (this is a phase demodulator!)

Demodulator can demodulate BPSK but not QPSK:

- A spectrum inversion may have occurred in the RF transmission chain. If so, invert the spectrum inversion flag at the demodulator.

Configuration Management

This specification is to be used in conjunction with VHDL software revision 0 and ComBlock control center revision 3.10g and above.

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1826 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

FPGA utilization

Resource	Estimation	Available	Utilization...
LUT	52728	63400	83.17
LUTRAM	90	19000	0.47
FF	60291	126800	47.55
BRAM	54.50	135	40.37
DSP	59	240	24.58
IO	89	285	31.23
BUFG	7	32	21.88
MMCM	1	6	16.67
PLL	1	6	16.67

(shown for Artix7-100T)

Reference Documents

[1] Space Network Interoperable PN Code Libraries 451-PN CODE-SNIP

ComBlock Ordering Information

COM-1826 TDRSS Spread-Spectrum modem

Options:

- 1,2 or 3 baseband receivers per 1RU chassis
- RF modulator output
- TCP-IP modulator input

ECCN: 5A001.b.3

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