COM-1808_TX
DVB-S2 DIGITAL TRANSMITTER

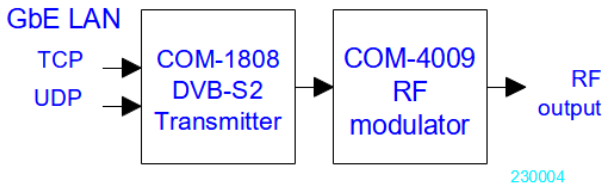
Key Features

- Digital DVB-S2 transmitter. Compliant with [1].
- Up to 4 concurrent input streams:
  - stream0 GbE TCP port 1024
  - stream1 GbE UDP port 1025
  - stream2 internal PRBS11 test sequence
  - stream3 internal Byte counter test sequence
- Stream 0 flexible user-defined configuration: stream type (transport stream, generic stream packetized, generic bit stream), user packet length, input stream synchronization, null packet detection, frame length, FEC encoding rate, modulation type.
- Other three input streams have fixed configurations.
- User-defined modulation attributes: symbol rate, frequency offset, SRRC filter roll-off, common to all input streams.

Supported features

Feature	Supported
Input stream synchronizer	Yes
Null packet deletion	Yes
Error correction encoding	LDPC + BCH
Encoding rate	1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
Coding and modulation	CCM, VCM, ACM
FEC frame	normal (64800 bits) short (16200 bits)
Modulation	QPSK, 8-PSK, 16APSK, 32APSK
Maximum modulation symbol rate	80 Msymbols/s
SRRC filter roll-off	0.35, 0.25 and 0.20
Output	complex (I,Q) baseband samples, 16-bit precision.

Typical assembly



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Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

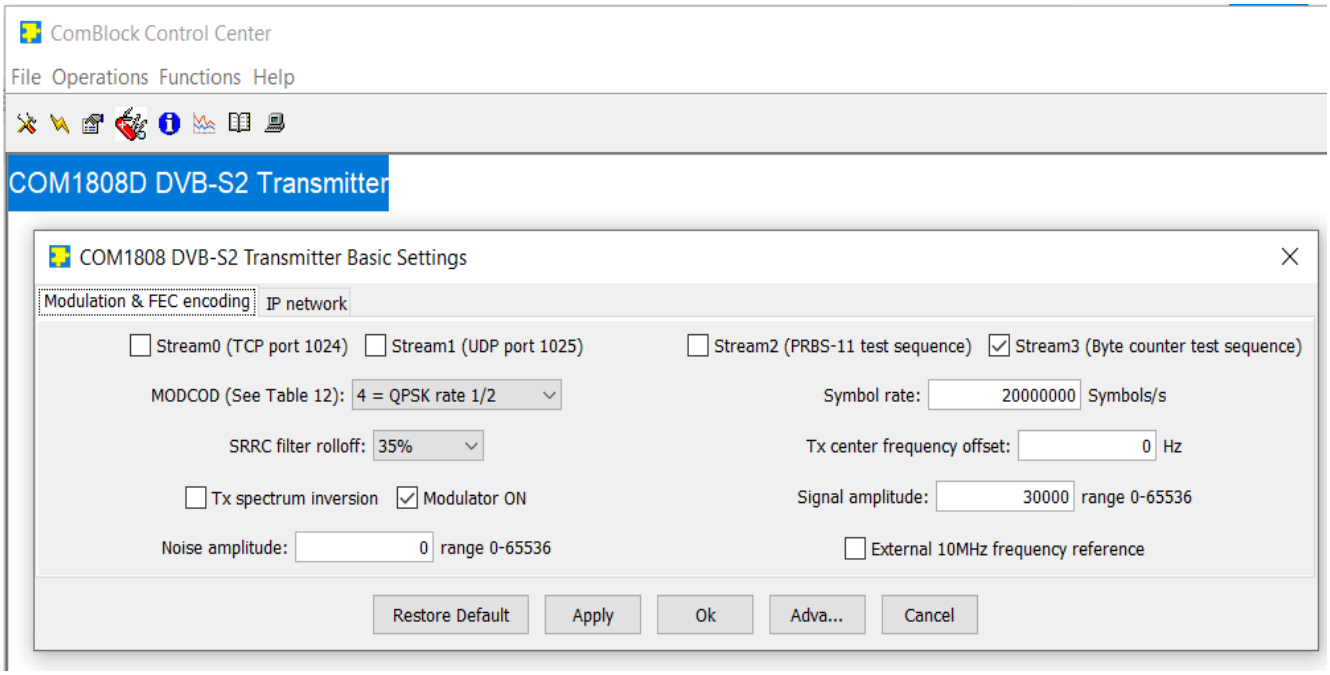
- USB, TCP-IP/LAN

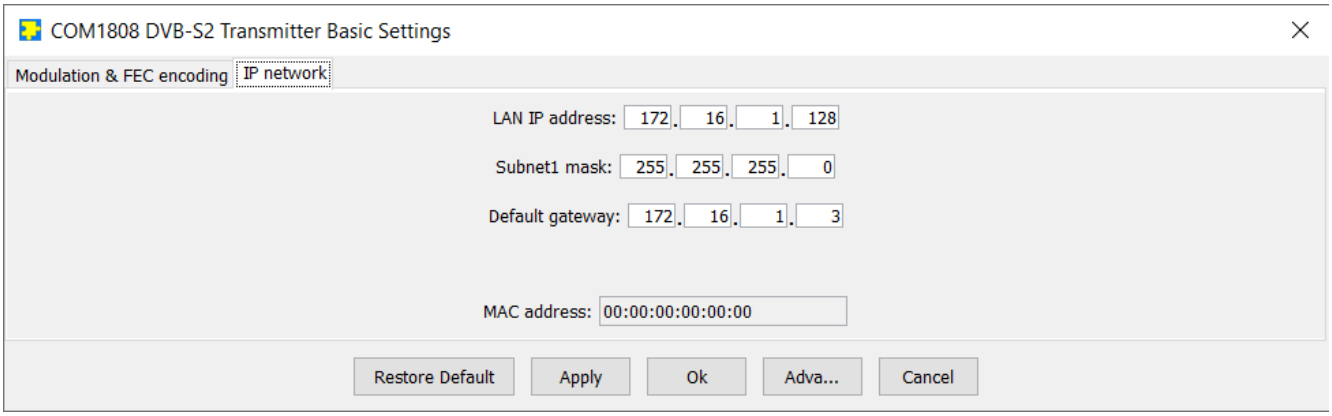
or connections via adjacent ComBlocks

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1808 is to use the **ComBlock Control Center** software (downloadable from https://comblock.com/download.html). In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1808 module to be configured, next click the *Settings* button to display the *Settings* window shown below.





Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Several key parameters are computed on the basis of the receive sampling clock f_{clk_rx} and transmit sampling clock f_{clk_tx} or the 125 MHz internal processing clock f_{clk_p}.

General	
Parameters	**Configuration**
Internal/External frequency reference	0 = internal TCXO as frequency reference. 1 = external. Use the 10 MHz clock externally supplied through the J7 SMA connector as frequency reference. REG0(7)

Modulator	
Parameters	**Configuration**
Input Stream enable	0 to disable, 1 to enable **Stream0**: TCP server port 1024 **Stream1**: UDP server port 1025 **Stream2**: PRBS 11 test sequence **Stream3**: Byte counter test sequence REG0(3:0)
Transmit sampling clock frequency f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock. Expressed as as f_{clk_tx} = 160 MHz * M / (D * O)) where D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 1.0. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 1.0. Fixed point format 7.3 Note: the graphical use interface computes the best values for M, D and O. **Baseline: 160 Msamples/s.** REG1(6:0) = D REG2 = M(7:0) REG3(1:0) = M(9:8) REG4 = O(7:0) REG5(2:0) = O(10:8)
Symbol rate f_{symbol_rate}	The modulator symbol rate is expressed as $f_{symbol\ rate\ tx} * 2^{32} / f_{clk\_dac}$ Because DDR is not supported at the DAC interface, the maximum symbol rate is f_{clk_dac} /2 [i.e. 0x80000000] REG24 (LSB) – REG27 (MSB)
Modulation type	Modulation type 0 = unmodulated 1 = DVBS2 QPSK [1] section 5.4.1 2 = DVBS2 8-PSK [1] section 5.4.2 3 = DVBS2 16-APSK [1] section 5.4.3 4 = DVBS2 32-APSK [1] section 5.4.4 REG6(4:0)
Root raised cosine filter rolloff factor	RRC filter rolloff 0 = 35%, 1 = 25%, 2 = 20% REG7(2:0)
Spectrum inversion	Invert Q bit 0 = off 1 = on REG7(6)
Turn output on/off	Controls the external RF modulator through the TX_ENB pin. The TX_ENB control signal to the RF modulator will also be turned off when there is no input data to transmit. 0 = off 1 = on REG7(7)
Digital Signal gain	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Please check for saturation (see test points) when changing either the symbol rate or the signal gain. REG10 (LSB) – REG11 (MSB)
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation (see test points) when changing this parameter. REG12 (LSB) – REG13 (MSB)
Output center frequency (f_c)	The modulated signal center frequency can be shifted in frequency

	32-bit signed integer (2's complement representation) expressed as $\mathbf{f_c} * 2^{32} / \mathbf{f_{clk\_dac}}$ REG14 (LSB) – REG17 (MSB)

External transmitter gain control	When using an external transceiver such as the COM-350x family, the transmitter gain can be controlled through the TX_GAIN_CNTRL1 analog output signal. Range 0 – 3.3V. REG22: LSB, REG23(3:0): Msb

Stream 0 attributes	
Type	Transport Stream Input or Generic Stream Input (packetized or continuous) 11 = transport stream, 188B frame 00 = generic stream, packetized, user-defined fixed length 01 = generic bit stream REG8(1:0)
User Packet Length (UPL)	User Packet Length in bits, in the range 0 to 65 535 -- fixed 188 Bytes for transport stream, up to 65535 bits for generic stream -- If UPL is greater than 65535 bits, use generic bit stream. -- For packetized stream, UPL includes the sync byte Ignored when generic continuous stream. REG20 (MSB) - REG19(LSB)
Null packet detection	Null Packet Deletion Generally enabled for transport stream and/or ACM REG8(2)
Input synchronization	Input Stream SYnchronization Indicator: If ISSYI = 1 = active, the ISSY field is inserted after each User Packet REG8(3)
BB frame length	0 DVB-S2 normal frame nldpc=64800 1 DVB-S2 and DVB-S2X short frame nldpc=16200 2 DVB-S2X medium frame nldpc=32400 REG9(1:0)

Other transport streams have fixed configurations.

Error correction	
LDPC encoding rate	Coding rate (LDPC code identifier) can change dynamically (in the case of VCM/ACM) will be enacted at the next assembled BBFRAME 0: rate 1/4 or 1/5 [normal,short,medium frames] 1: rate 1/3 [normal,short,medium frames] 2: rate 2/5 [normal,short frames] 3: rate 1/2 [normal,short frames] 4: rate 3/5 [normal,short frames] 5: rate 2/3 [normal,short frames] 6: rate 3/4 [normal,short frames] 7: rate 4/5 [normal,short frames] 8: rate 5/6 [normal,short frames] 9: rate 8/9 [normal,short frames] 10: rate 9/10 [normal frames] REG18(4:0)

Network Interface	
Parameters	**Configuration**
LAN MAC address LSB	REG236. To ensure uniqueness of MAC address. The MAC address most significant bytes are tied to the FPGA DNA ID. However, since Xilinx cannot guarantee the DNA ID uniqueness, this register can be set at the time of manufacturing to ensure uniqueness. This byte is not overwritten when importing configuration data.
Static IP address	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 REG47 (MSB) - REG50 (LSB)
Subnet mask	Typically 0x FF FF FF 00 REG51 (MSB) – REG54(LSB)
Gateway IP address	REG55 (MSB) – REG58(LSB)

(Re-)Writing to the last control register REG58 is recommended after a configuration change to enact the change.

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-9 Properly operating hardware will result in the following sequence being displayed: 01 F1 1D xx 1F 93 10 00 22 1F.
LAN PHY ID	0x22 SREG8
Tx: Modulator saturation	Saturation in the output signal path. 0 when no saturation. bit 0: saturation at root raised cosine FIR filter bit 1: saturation at first HBF, x2 interpolation filter bit 2: saturation at second HBF, x2 interpolation filter bit 3: saturation at frequency translation bit 4: saturation when adding AWGN These flags are reset upon reading this status register. SREG10(4:0)
Tx: Measured modulated signal power	SREG11(LSB) – SREG13(MSB)
Tx: Measured AWGN power	Approximation: noise power is uniform over a range of +/- 2*symbol rate SREG14(LSB) – SREG16(MSB)
GbE MAC address	Unique 48-bit hardware address (802.3). In the form SREG17:SREG18:SREG19: ….:SREG22
Ethernet MAC bad CRC counter	SREG23 (LSB) – SREG24(MSB)
TCP server connection status	TCP server port 1024 connection status for stream0 1 = connected 0 = no connection SREG(25)(0)
UDP received frame counter	Number of UDP frames received at port 1025 for stream1 SREG26 (LSB) – SREG27(MSB)

Multi-byte status variables are latched upon (re-)reading SREG7.

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. Click on the button to start, then select the signal traces and trigger are defined as follows:

Trace 1 signals	Format	Nominal sampling rate	Buffer length (samples)
1: modulated signal to DAC, I-channel	8-bit signed	DAC clock f_{clk_dac}	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: modulated signal to DAC, Q-channel	8-bit signed	DAC clock f_{clk_dac}	512

Signals sampling rates can be changed under software control by adjusting the decimation factor

In particular, selecting the f_{clk_adc} demod clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

Digital Test Points

Test Point	Definition
J4/A11	CLK_Txg (DAC clock)
J4/A12	CLK_P processing clock
J4/A13	160 MHz intermediate clock frequency

Options

Several interface types are supported through multiple firmware options. All firmware versions are on the supplied CD-ROM and can also be downloaded from
http://www.comblock.com/download.html

Changing the firmware option requires loading the firmware once using the ComBlock control center, then switching between the stored firmware versions The selected firmware option is automatically reloaded at power up or upon software command within 18 seconds

Option	Definition
-C	J8 right connector: 2*16-bit output samples, 2*12-bit input samples. This interface is compatible with the COM-3504 dual Analog<->Digital Conversions. Maximum 160 MSamples/s. J4 left connector: synchronous serial modem input and output bit streams.
-D	J8 Right connector : 2*16-bit LVDS output samples. This interface is compatible with the COM-4009 broadband RF modulator. J4 left connector: 2*12-bit input, COM-30XX compatible receiver

Operation

Transmitter Inputs

The transmitter supports up to four concurrent streams. Each input stream can be individually enabled/disabled.

Stream0:TCP data stream received over Gigabit Ethernet (10/100/1000 Mbps). The buit-in TCP server opens a socket on port 1024 and awaits a connection request from a remote TCP client. The TCP protocol ensures a proper flow control, without any underflow or overflow, as long as the TCP client sends data as fast as allowed by the TCP connection.

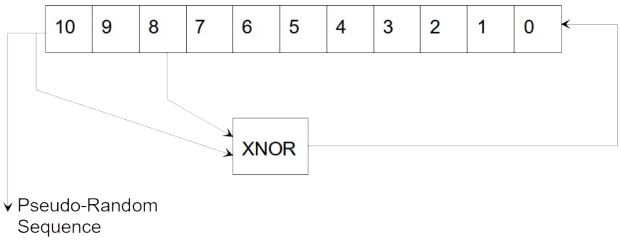
Stream1: transport stream received over GbE as 188-Byte UDP frames received at port 1025. The sender is responsible controlling the throughput (and not overflowing the tx input buffer).

Stream2: PRBS-11 pseudo-random test sequence. Useful to measure Bit Error Rate at the receiving end.

Stream3: Byte counter.

Pseudo-Random Bit Stream (Test Pattern)

A periodic pseudo-random sequence can be used as stream2. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:



The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100 1100111000 0000010011 1111010001 1110110100 1101001100 0011000001

Variable Coding & Modulation (VCM)

Streams are configured individually in terms of type, User Packet Length (UPL), null packet deletion, Input Stream SYnchronizer (ISSY), frame length, coding, modulation and pilot insertion.

Stream0: configuration is user defined in the GUI or through control registers.

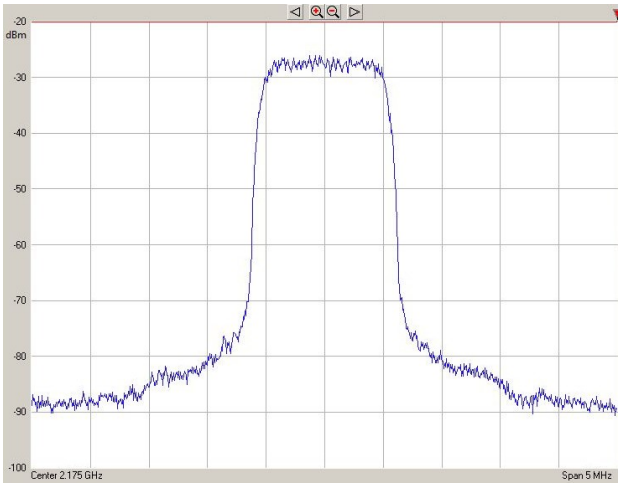
Stream1: fixed configuration:
transport stream, 188B frame, input stream synchronization, null packet detection, short frame n_{ldpc}=16200. Fixed MODCOD 4 (rate ½ coding, QPSK)

Stream2: fixed configuration:
generic bit stream, not packetized, no input stream synchronization, no null packet detection, short

frame n_{ldpc}=16200. Fixed MODCOD 12 (rate 3/5 coding, 8-PSK)

Stream3: fixed configuration:
transport stream, 188B frame, input stream synchronization, null packet detection, short frame n_{ldpc}=16200. Fixed MODCOD 18 (rate 2/3 coding, 16-APSK)

Output Spectrum

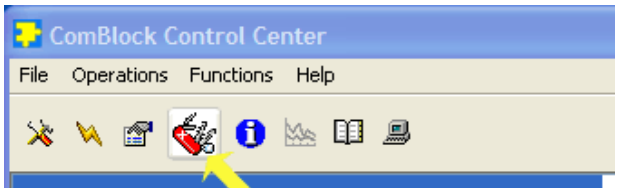


QPSK output spectrum 1MSymbols/s
(output of COM-4009 RF modulator, 2.175GHz)

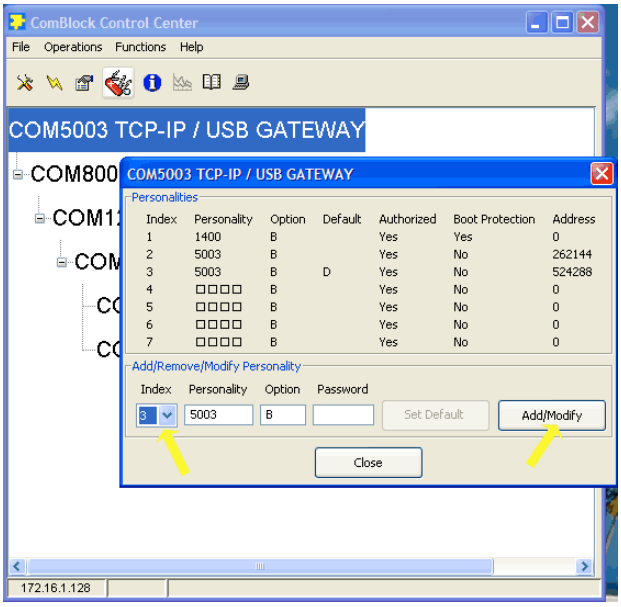
Load Software Updates

From time to time, ComBlock software updates are released.

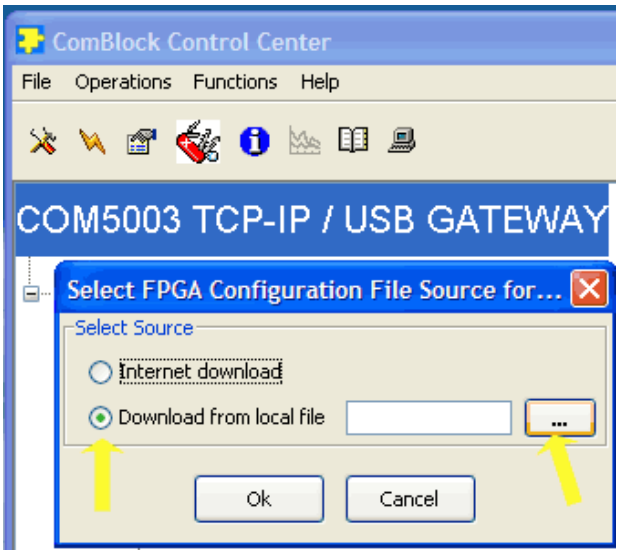
To manually update the software, highlight the ComBlock and click on the Swiss army knife button.



The receiver can store multiple personalities. The list of personalities stored within the ComBlock Flash memory will be shown upon clicking on the Swiss army knife button.



The default personality loaded at power up or after a reboot is identified by a ‘D’ in the Default column. Any unprotected personality can be updated while the Default personality is running. Select the personality index and click on the “Add/Modify” button.



The software configuration files are named with the .bit extension. The bit file can be downloaded via the Internet, from the ComBlock CD or any other local file.

The option and revision for the software currently running within the FPGA are listed at the bottom of the advanced settings window.

Recovery

This module is protected against corruption by an invalid FPGA configuration file (during firmware upgrade for example) or an invalid user configuration. To recover from such occurrence, connect a jumper in J3 and during power-up. This prevents the FPGA configuration and restore USB communication [LAN communication is restored only if the IP address is known/defined for the personality index selected as default]. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

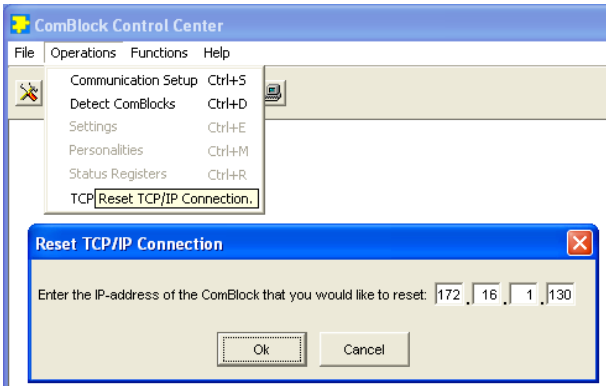
UDP Reset

Port 1029 is open as a UDP receive-only port. This port serves a single purpose: being able to reset the modem (and therefore the TCP-IP connection) gracefully. This feature is intended to remedy a common practical problem: it is a common occurrence for one side of a TCP-IP connection to end abnormally without the other side knowing that the connection is broken (for example when a client 'crashes'). In this case, new connections cannot be established without first closing the previous ones.

The problem is particularly acute when the COM-1808 is at a remote location.

The command "@001RST<CR><LF>" sent as a UDP packet to this port will reset all TCP-IP connections within the COM-1808.

TCP-IP connections can also be cleared remotely from the ComBlock Control Center as illustrated below:

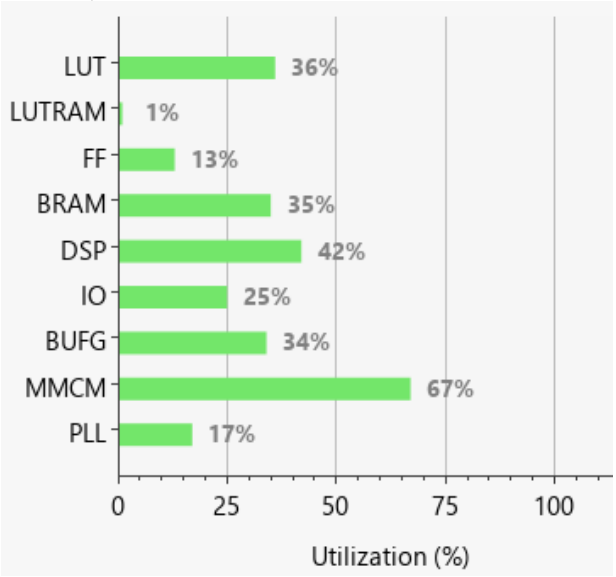


Troubleshooting Checklist

1. The module is performs self-checks at power up. Click on  to display the status registers. Properly operating hardware will result in the following sequence being displayed: SREG0-SREG8 = 01 F1 1D xx 1F 93 10 00 22.
2. Check status register SREG4 bits 0 – 5: if not 111111, the power supply voltage may be outside the nominal range of 4.9 to 5.5V.
3. Demodulator can't achieve lock even at high signal-to-noise ratios:
   - Make sure the modulator baseband I/Q signals do not saturate, as such saturation would strongly distort the modulation phase information.

VHDL code

The FPGA code is written in VHDL. It does not use any IP core or third-party software.
It occupies the following FPGA resources (when including modulator, demodulator, turbo code, AWGN):



Resource	Utilization	Available	Utilization...
LUT	22880	63400	36.09
LUTRAM	72	19000	0.38
FF	16061	126800	12.67
BRAM	47.50	135	35.19
DSP	100	240	41.67
IO	72	285	25.26
BUFG	11	32	34.38
MMCM	4	6	66.67
PLL	1	6	16.67

Operating input voltage range

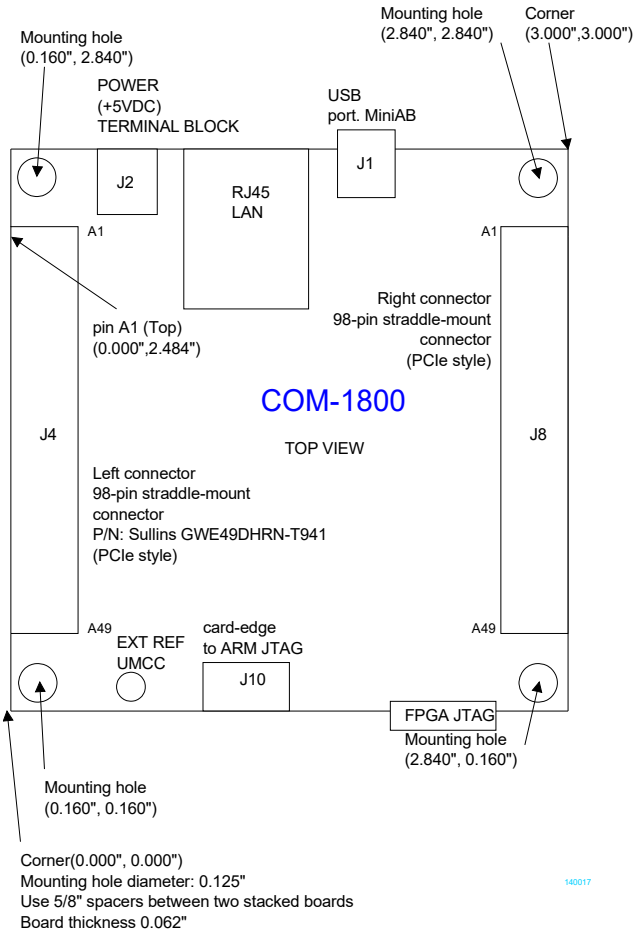
Supply voltage	+4.5V min, +12V max 650mA typ.

Absolute Maximum Ratings

Supply voltage	-0.5V min, +20V max
98-pin connector inputs	-0.5V min, +3.6V max

Important:
The I/O signals connected directly to the FPGA are NOT 5V tolerant!

Mechanical Interface



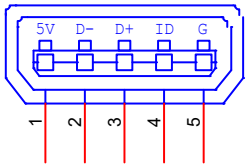
Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1800schematics.pdf

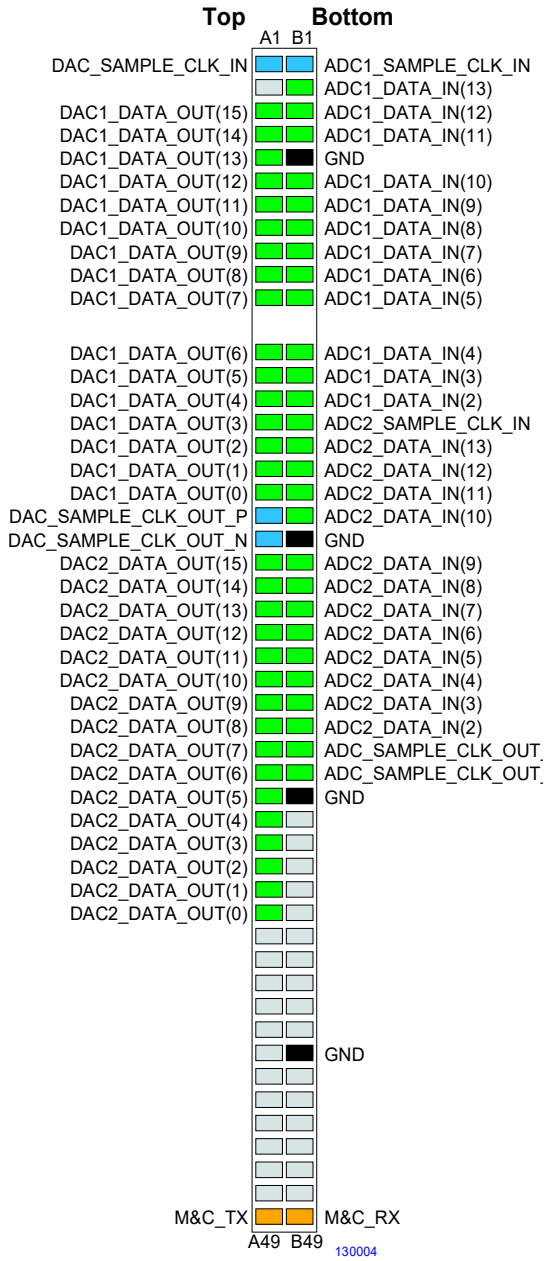
Pinout

USB

The USB port is equipped with mini type AB connectors. (G = GND). The COM-1808 acts as a USB device.

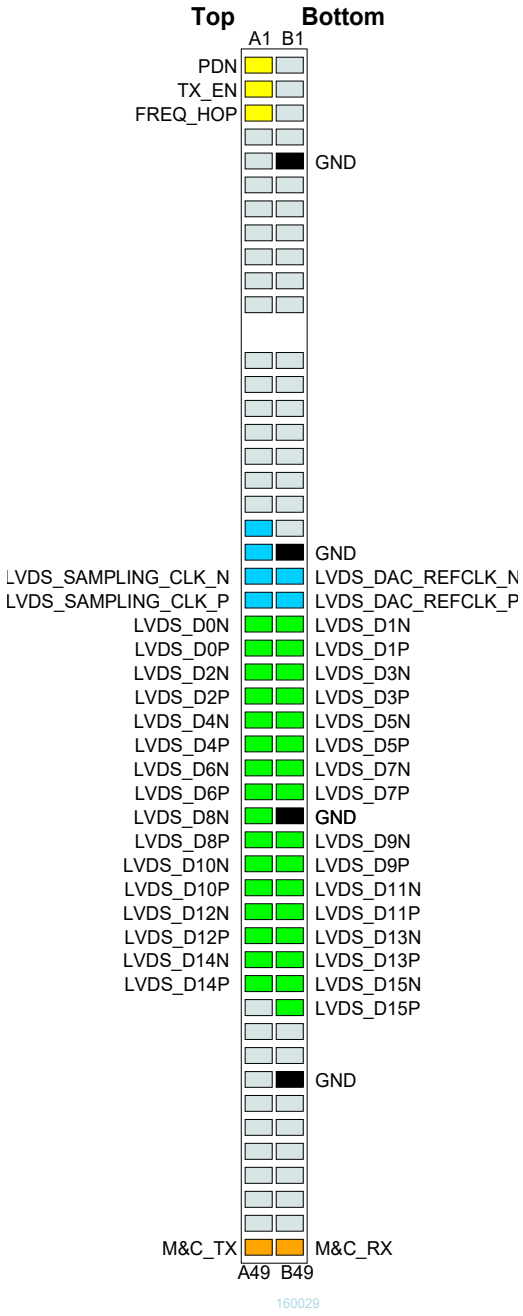


Right Connector J8



2*16-bit output samples, 2*12-bit input samples. This interface is compatible with the COM-3504 dual Analog<->Digital Conversions.
(-C firmware option)

Right Connector J8



This interface is compatible with the COM-4009 RF modulator (**-D** firmware option)

I/O Compatibility List

(not an exhaustive list)

Right connector (J9)
COM-3504 Dual Analog <-> Digital Conversions 2*16-bit 250 MSamples/s
COM-4009 400 MHz – 4.4 GHz Broadband RF modulator

Configuration Management

This specification is to be used in conjunction with VHDL software revision 1 and ComBlock control center revision 4.03b and above.

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1808 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com1808.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

Reference documents

[1] DVB-S2 specifications, ETSI EN 302 307-1 V1.4.1 (2014-11)

[2] DVB-S2 Extensions (DVB-S2X) specifications ETSI EN 302 307-2 V1.1.1 (2015-02)

Acronyms

Acronym	Definition
ACM	Adaptive Coding and Modulation
AWGN	Additive White Gaussian Noise
CCM	Constant Coding and Modulation
CTS	Clear-To-Send flow control flag
DDR	Dual Data Rate
DVB	Digital Video Broadcasting
FPGA	Field Programmable Gate Array
GS	Generic Stream
GbE	Gigabit Ethernet
ISSY	Input Stream SYnchronizer
LSb	Least Significant bit in a word
MSb	Most Significant bit in a word
RF	Radio Frequency
SRRC	Square Root Raised Cosine (filter)
TS	Transport Stream
tx	Transmit
UPL	User Packet Length
VCM	Variable Coding and Modulation

ComBlock Ordering Information

COM-1808_TX DVB-S2 digital transmitter

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