COM-1800 FPGA (XC7A100T) + ARM + DDR3 SODIMM socket + GbE DEVELOPMENT PLATFORM

Key Features

- State-of-the-art digital signal processing platform comprising
  - Large 7-series Xilinx FPGA (XC7A100T-1) FPGA for massive parallel computing
  - ARM 32-bit co-processor @100MHz (LPC1768) for complementary sequential computing[1]
  - 204-pin SODIMM socket for an optional (1 through 8 GB typ.) DDR3 memory module. 20+ Gbps effective throughput.
  - 1Gbit NAND for non-volatile storage of numerous FPGA configurations and user data.
  - Gigabit Ethernet RJ-45 tied to FPGA for maximum throughput.
  - Auxiliary DAC: 12-bit precision, 1 MSamples/s for gain control
- Comprehensive environment through plug-in modules
  - HDMI input/output and additional gigabit Ethernet transceiver (COM-5102)
  - 4 SATA disks interfaces (COM-5103)
  - High-speed analog/digital converters (COM-3504, COM-2802)
  - RF receivers (COM-30xx)
- Hi-stability frequency reference: internal VC-TCXO or external frequency reference via UMCC [2]connector.
- The COM-1800 is compatible with a comprehensive development environment of free industry-standard tools:
  - Xilinx Vivado for development from VHDL or Verilog source code to FPGA binary [from Xilinx]
  - Eclipse IDE + GNU ARM tool chain from C/C++ source code to ARM binary [from yagarto.de]
  - ComBlock flashloader to program the FPGA and ARM binaries into the board non-volatile flash memory over USB. [included]
- ComScope –enabled: key internal signals can be captured in real-time and displayed on host computer.

DDR3 SODIMM socket is underneath.

[1] Use of the ARM processor is at the user's discretion. The ARM processor is pre-programmed with all basic functions.

[2] Ultra Miniature Coaxial Connector.

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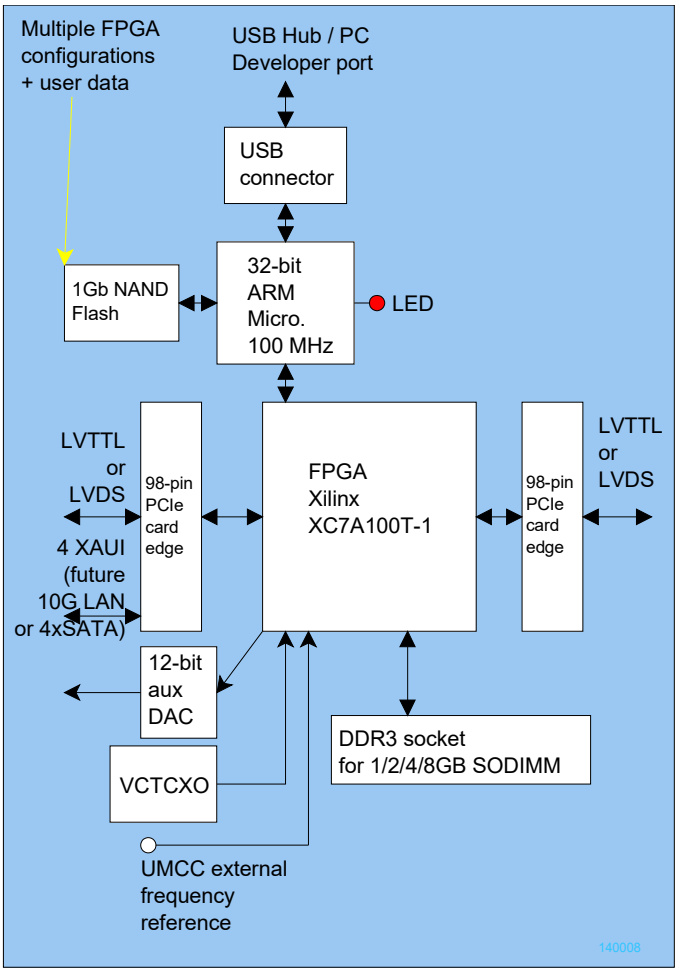
 Issued 4/11/2021

For the latest data sheet, please refer to the **ComBlock** web site: ComBlock.com/com1800.html.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to ComBlock.com/product_list.htm.



Com-1800 Hardware Block Diagram

Operating input voltage range

Supply voltage	+4.5V min, +12V max

Absolute Maximum Ratings

Supply voltage	-0.5V min, +20V max
98-pin connector inputs	-0.5V min, +3.6V max

Important:
The I/O signals connected directly to the FPGA are NOT 5V tolerant!

Operations

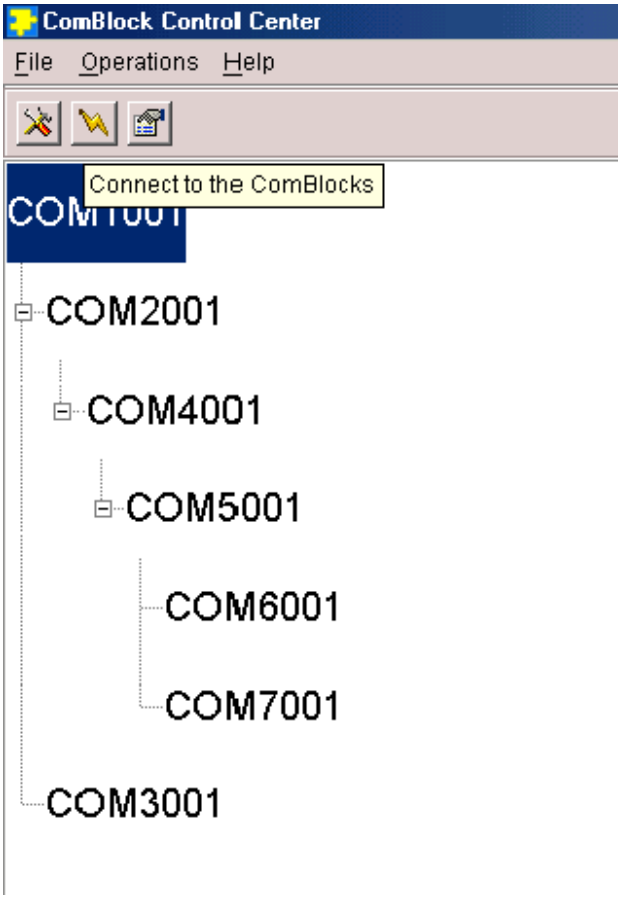
Graphical User Interface

A user-friendly graphical user interface (hereafter named ComBlock Control Center) is supplied with the COM-1800. The ComBlock Control Center runs on a host computer with Windows operating system. It allows the user to communicate with the COM-1800 over LAN, USB 2.0 or any adjacent module.

The primary use of the ComBlock Control Center is to:

(a) download new FPGA firmware (into non-volatile Flash memory)
(b) set control registers
(c) monitor status registers
(d) capture and display internal signals (ComScope)

When activated, the ComBlock Control Center enumerates the ComBlock modules within the assembly. The modules are identified by their name in a tree-like structure. Each module can be configured and monitored remotely.



The ComBlock Control Center software is provided with all ComBlock modules. The user's manual can be found at ComBlock.com/download/ccchelp.pdf.

Flash Memory

The FPGA configuration can be stored in non-volatile (Flash) memory. The ComBlock Control Center includes the utility to (re)write the FPGA .bit file into the flash memory over the selected communication link.

Communication links: the COM-1800, when used as a stand-alone module, communicates with the ComBlock Control Center over USB or LAN. When part of a larger ComBlock assembly, the COM-1800 can communicate over any other communication link supported by the assembly.

The FPGA is automatically configured after power-up or reset with one of the configuration files stored in Flash memory, as long as the J3 jumper is not present. A configuration file size for the XC7A100T is 3,825,788 bytes. Configuration time is typically 18 sec.

Remove any jumper on J3 to allow automatic FPGA configuration at power up.

FPGA JTAG

The FPGA can also be configured and monitored through the J6 6-pin JTAG interface. A jumper must be placed over J3 to select this method of external JTAG configuration.

This method requires a special programming cable (such as the Xilinx platform cable USB II DLC-10). Please note that the NAND flash cannot be programmed through the JTAG pod, only through the ComBlock control center utility.

Hardware self-check

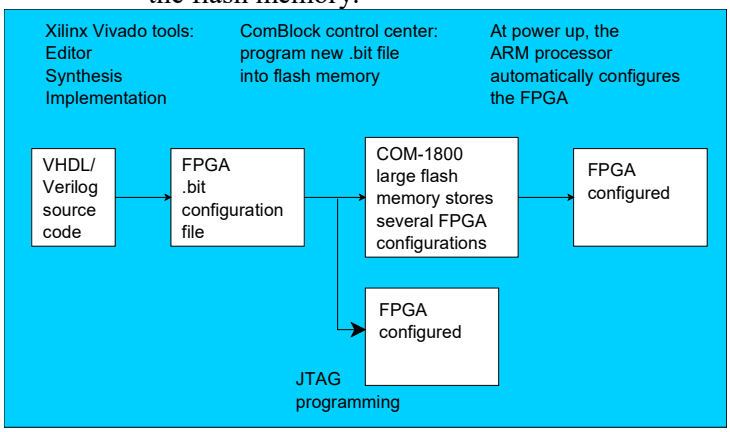
At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-8. Click on the S*tatus* button to read these status registers.

Properly operating hardware will result in the following sequence being displayed:
SREG0-SREG9 = 01 F1 1D xx 1F 93 10 xx 22 03

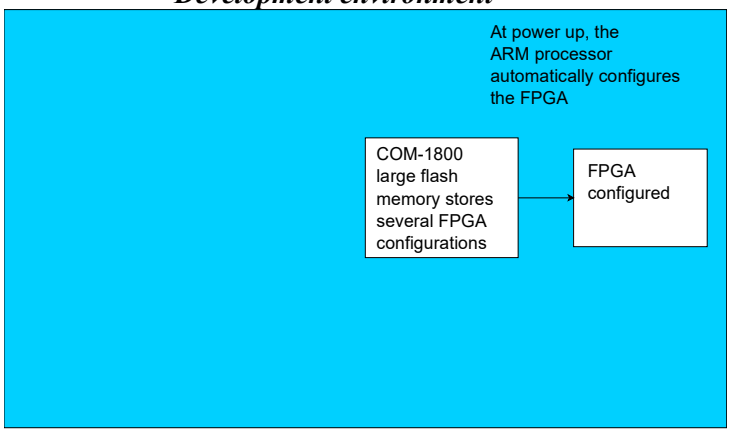
FPGA Development Steps

Developing a custom FPGA-based application requires the following key steps:

1) The user writes VHDL or Verilog source code.
2) The Xilinx tool (Xilinx Vivado design suite) performs synthesis, place and route. The output is a binary .bit FPGA configuration file.
3) The .bit file can be loaded directly into the FPGA from Vivado through a JTAG pod.
4) Alternatively, the ComBlock Control Center programs the .bit file into the board non-volatile (flash) memory.
5) At power-up, the ARM processor configures the FPGA using the designated .bit configuration file stored on the flash memory.



Development environment



Run-time environment

VHDL code template

A VHDL template project is available from the ComBlock CD or on-line at www.comblock.com/download.html#COM1800template

The template project includes:

- the VHDL source code (.vhd)
- the constraint file (.ucf) listing all pin assignments
- The Xilinx Vivado project with the synthesis and implementation settings
- The resulting .bit file is ready to be loaded into flash memory

The sample code describes how the application interfaces with the ComBlock Control Center graphical user interface through control and monitoring registers. Monitoring and control messages and syntax are described in ComBlock.com/download/m&c_reference.pdf.

It also describes how to capture key internal signals in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center.

The ComScope user manual is available at ComBlock.com/download/Comscope.pdf.

Accidental FPGA file corruption

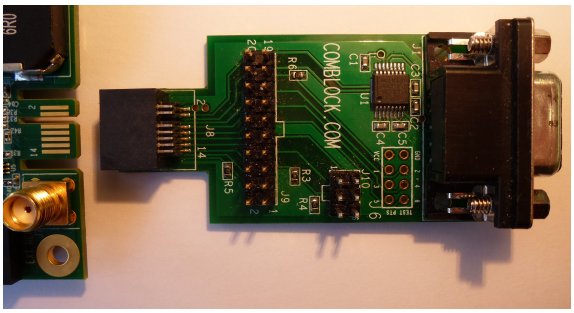
The COM-1800 is protected against corruption by an invalid FPGA configuration file. To recover from such occurrence, place a jumper on J3 then power-up the COM-1800. Remove the jumper after the red LED turns off. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center and a USB link.

ARM Programming

Writing code for the ARM co-processor is *optional*. The ARM processor is factory programmed with the full set of functions described in this document. In many application cases, the processor could be left as is.

However, since the ARM processor resources are significantly underutilized after the initial configuration, it is made available for developers to implement additional digital signal processing algorithms or customize the power profile.

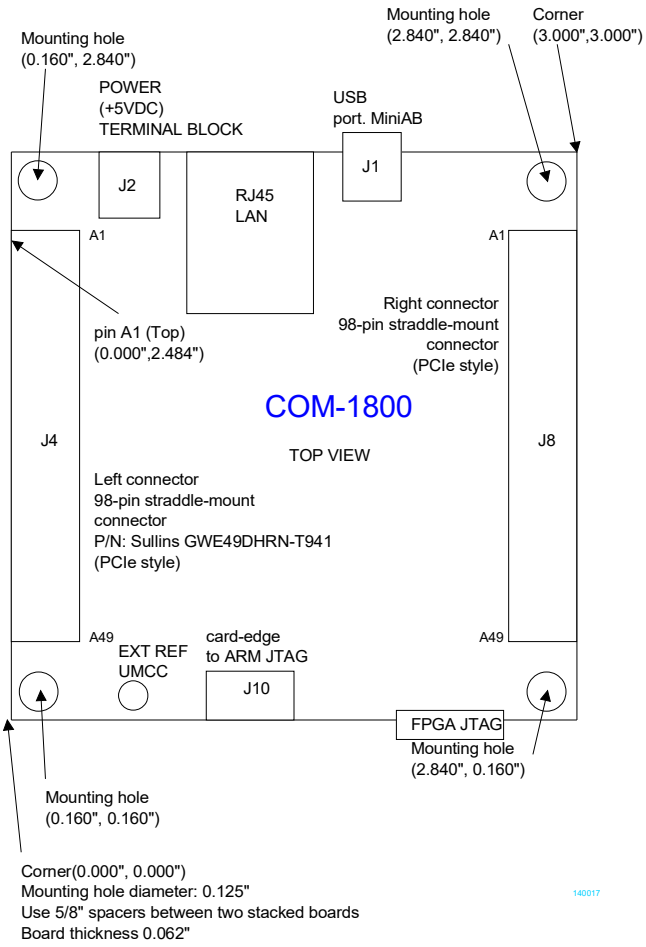
The ARM microcontroller can be programmed through an external adapter (not included) to keep the board size small. The adapter (model Y03007R4) includes a standard 20-pin ARM JTAG connector and a RS-232 DB9 connector. The latter, when used in conjunction with the flashmagictool.com tool, is a fast and reliable way to program the ARM controller flash memory with a new executable file.



Optional adapter for programming the flash-based microprocessor via serial link to a PC, or through a 20-pin ARM JTAG pod.

The ARM microcontroller source code is available for download from www.comblock.com/download.html#Latest_ARM_firmware

Mechanical Interface



Schematic

The board schematic is available on-line at
ComBlock.com/download/com_1800schematics.pdf

Clocks

Four distinct clocks are available to the FPGA:

- A 19.2 MHz voltage and temperature-controlled crystal oscillator provides the board most stable frequency reference. The VCTCXO oscillator 2.5ppm stability over -30/+75C temperature can be further reduced by calibration using the R59 trimmer.
- A 100 MHz MEMS oscillator provides a clean frequency reference intended for use with the DDR3 controller.
- A 156.25 MHz MEMS oscillator provides a clean low-jitter LVDS frequency reference intended for use with the high-speed XAUI interface on FPGA bank 216.
- A higher stability frequency reference can also be supplied externally through the J6 (UMCC) coaxial connector.

I/O Standards

The digital signals on the 98-pin connectors J4 and J8 are LVTTL (0 – 3.3V) signals by default. FPGA banks 34 and 35 could be reconfigured for 2.5V Vcco IOs by swapping a surface-mount diode and 0Ω resistor. See schematics for details. High-speed LVDS differential IOs require a 2.5V Vcco.

Digital to Analog Converter (DAC)

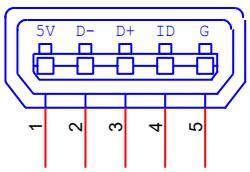
A 12-bit DAC/Analog output is built-in for gain control. The DAC operates under the direct control of the FPGA The DAC output is connected to pin "B13" of the J4 connector. The DAC can be disabled in software to a high impedance state or physically disabled by removing the 0Ω R73 resistor.

The DAC can typically operate at a 0.5V/µsec slew rate. The output voltage range is from 0 to 3.3 V. The driver provided in the code template allows for approximate refresh rate of up to 1.765 MHz (slew rate limited.)

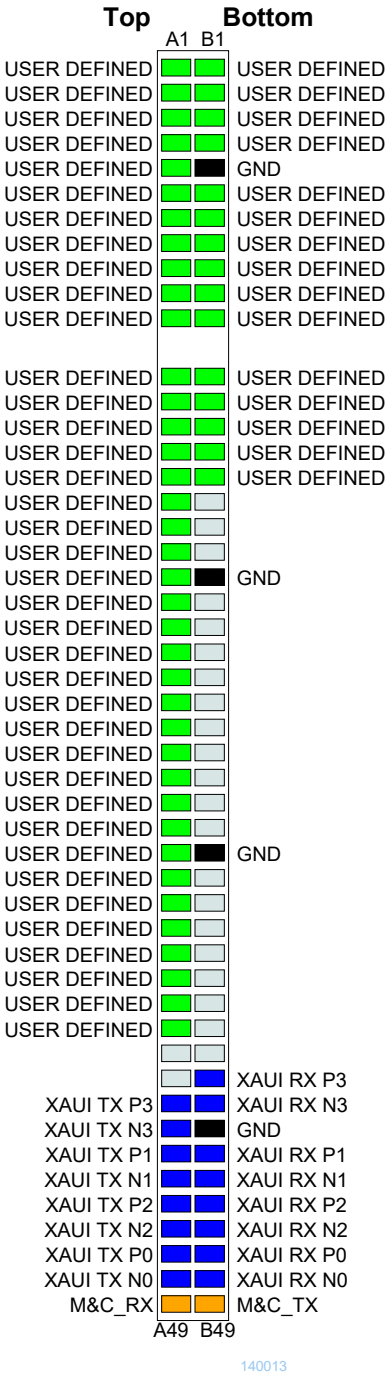
Pinout

USB

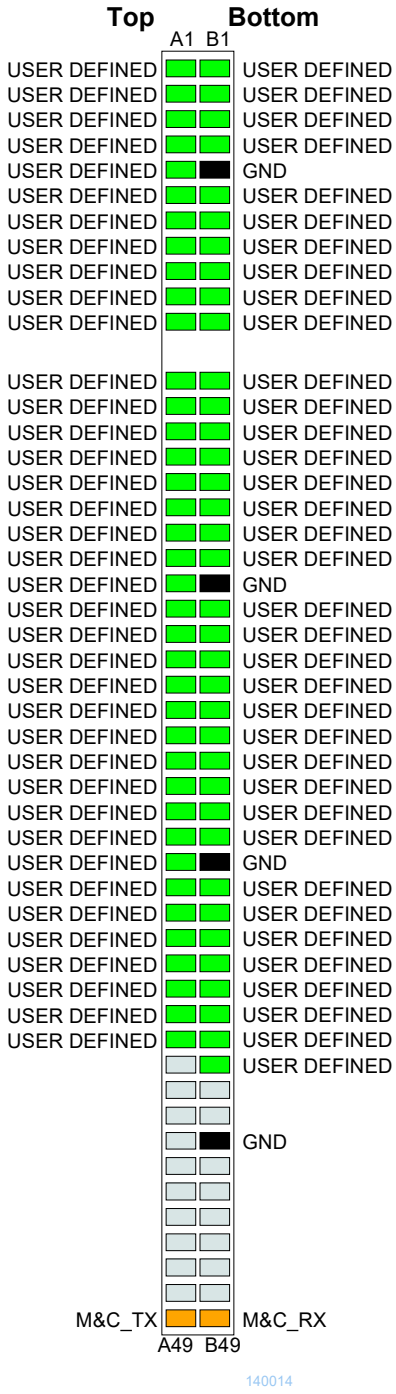
The USB port is equipped with mini type AB connectors. (G = GND). The COM-1800 acts as a USB device.



Left Connector J4



Right Connector J8



98-pin to 40-pin adapters to interface with other Comblocks are supplied free of charge. Please let us know about your interface requirements at the time of order.

Compatibility List

(Not an exhaustive list)

Compatible modules
COM-30xx RF/IF/Baseband receivers for frequencies ranging from 0 to 3 GHz.
COM-3504 Dual Analog <-> Digital Conversions
COM-5102 Gigabit Ethernet + HDMI interface
COM-5103 4 SATA interface
Software
COM-5401SOFT Tri-mode 10/100/1000 Mbps Ethernet MAC, VHDL source code

ComBlock Ordering Information

COM-1800 FPGA (Xilinx Artix-7 XC7A100T) + ARM + DDR3 SODIMM socket + GbE development platform

Optional accessory: **Y03007R4** JTAG/Serial adapter for optional ARM micro programming

ECCN: EAR99

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