COM-1519SOFT
DIRECT-SEQUENCE SPREAD-SPECTRUM MODULATOR 60 Mchip/s
VHDL SOURCE CODE OVERVIEW

Overview

The COM-1519SOFT is a digital direct-sequence spread-spectrum modulator written in VHDL, including modulation, multiple baseband interfaces, DAC drivers, and ancillary test features. It is designed to be embodied within a single low-cost FPGA such as the Xilinx Spartan-6 LX45.

The entire **VHDL source code** is provided.

Key features and performance:

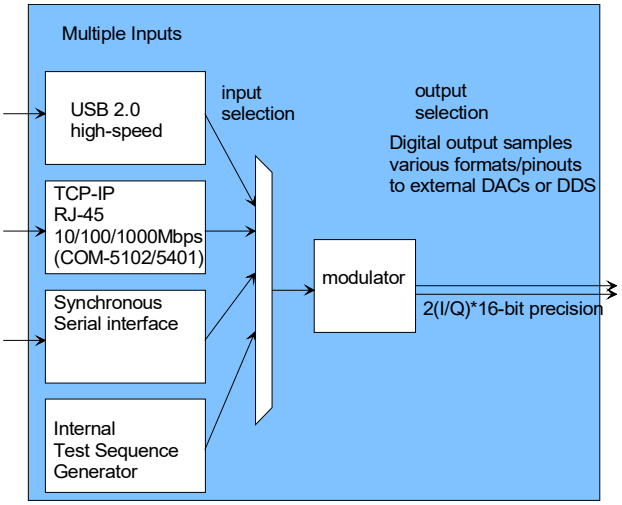
- Direct-Sequence Spread-Spectrum (DSSS) modulation
- Continuous mode operation (i.e. Burst mode is not supported)
- Maximum chip rate of 60 Mchips/s in a Xilinx Spartan-6 FPGA
- Baseband interfaces:
  - Synchronous serial interface with Plesiosynchronous buffer or
  - TCP-IP interface
  - USB 2.0 interface
- Ancillary components are also included for test signal generation and channel impairements (additive white Gaussian noise, Doppler)
- Drivers for three types of high-speed digital-to-analog converters.

Target Hardware

The code is written in generic VHDL so that it can be ported to a variety of FPGAs. The code is developed and tested on a Xilinx Spartan-6 FPGA.

It can be easily ported to any Xilinx Virtex-5, Virtex-6, Spartan-6 FPGAs and other FPGAs.

Overall Block Diagrams



Modulator connectivity

Monitoring and Control

Dynamic control and monitoring is implemented using 8-bit control registers (REG) and status registers (SREG). The top-level is written assuming that the FPGA is a peripheral on an 8-bit address/data bus controlled by an external microcontroller. The small monitoring and control section can be easily modified for other architectures.

Synthesis-time configuration parameters

The user can select the baseband interface and the DAC interface prior to synthesis by changing the **OPTION** constant at the top level.

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OPTION	DAC Type	Input
A	2*10-bit unsigned clock to DAC	USB or LAN (TCP-IP)
B	2*14-bit signed muxed, clock from DAC/DDS	USB or LAN (TCP-IP)
C	2*16-bit signed reclocked with separate fixed frequency high-speed clock	USB or LAN (TCP-IP)
D	2*10-bit unsigned clock to DAC	USB or 1-bit synchronous serial
E	2*14-bit signed muxed, clock from DAC/DDS	USB or 1-bit synchronous serial

Run-time configuration parameters

The user can set and modify the following controls at run-time through control registers, as listed below:

Parameters	Configuration
Processing clock f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock 20-bit unsigned integer expressed as $f_{clk\_tx} * 2^{20} / 300MHz$. 120 MHz maximum. 20 MHz recommended minimum REG0 = bits 7-0 (LSB) REG1 = bits 15 – 8 (MSB) REG2(3:0) = bits 19 – 16 (MSB)
Internal/External frequency reference	0 = internal. Use the internal 60 MHz clock (from the USB PHY) as frequency reference. 1 = external. Use the 10 MHz clock externally supplied through the J7 SMA connector as frequency reference. REG2(7)
Chip rate $f_{chip\ rate\ tx}$	The modulator chip rate is in the form $f_{chip\ rate\ tx} = f_{clk\_tx} / 2^n$ where n ranges from 1 (2 samples per chip) to 15 (chip rate = f_{clk_tx} / 32768). n is defined in REG3(3:0)
Code period	In chips. Valid range 3 – 65535 Can be less than the natural length of the selected code. In which case, the code is truncated. REG4: LSB REG5: MSB
Code selection	1 = Gold code (G1/G2 software selection) 2 = Maximal length sequence (G1 software selection) 3 = Barker code (lengths 11 or 13 only) 4 = GPS C/A code REG6(3:0)
Gold sequence / Maximal Length Sequence generator polynomial G1	24-bit. Describes the taps in the linear feedback shift register 1: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period $2^n - 1$. Example: $G1 = 1 + x + x^4 + x^5 + x^6$ is represented as 0x000039 This field is used only if Gold code or Maximal length sequences are selected. REG7 = LSB REG8 REG9 = MSB
Gold code generator polynomial G2	24-bit. Describes the taps in the linear feedback shift register 2: Same format as G1 above. This field is used only if Gold codes are selected. REG10 = LSB REG11 REG12 = MSB
GPS satellite ID	GPS signals from different satellites are designated by a PRN signal number in the range 1 – 37. This field is used only if GPS C/A codes are selected. REG10(5:0)

LSB = Least Significant Byte
MSB = Most Significant Byte

Symbol rate f_{symbol_rate}	The symbol rate can be set independently of the spreading code period. In this case, set REG13-16 such that $f_{symbol\_rate} * 2^{32} / f_{clk\_tx}$ REG13 = LSB REG14 REG15 REG16 = MSB Alternatively, symbols can be aligned with the spreading code period. In this case, REG16(7) as '1'. REG13-15 are ignored.
Digital Signal gain	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend checking for saturation at the D/A converter when changing either the symbol rate or the signal gain. (see status registers SREG8) REG17 = LSB REG18 = MSB
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation at the D/A converter when changing this parameter. REG19 = LSB REG20 = MSB
Modulation type	Modulation type before applying the direct-sequence spreading. Note: the modulation symbol transitions are not necessarily aligned with the chip transitions. 0 = BPSK 1 = QPSK REG21(5:0)
Spectrum inversion	Invert Q bit. (Inverts the modulated spectrum only, not the subsequent frequency translation) 0 = off 1 = on REG21(6)
Ouput spectrum shaping filter enabled	Enables/Disables raised cosine square root output spectrum shaping filter. 0 = enabled 1 = bypassed REG21(7)

Input selection / format, test modes	Select the origin of the modulator input data stream. 1 = from left J6 connector (Many comblocks), 1-bit serial 2 = high-speed USB, 8-bit parallel 3 = LAN/TCP-IP, port 1024 (through Ethernet adapter), 8-bit parallel 4 = test sequence: internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream). 5 = test sequence: unmodulated carrier. This helps checking the follow-on RF modulator. 8-bit parallel input bytes are transmitted MSb first. Test sequences override external input bit stream. REG22(2:0)
Spreading	Enable/Disable spectrum spreading. 0 = disabled 1 = enabled REG22(3)
Reserved	REG22(7) must be 0
Output Center frequency (f_{c_tx})	Fine tuning of center frequency. Typically 0 Hz. 32-bit signed integer (2's complement representation) expressed as $f_{c\_tx} * 2^{32} / f_{clk\_tx}$ For a clean output waveform, we recommend keeping the maximum frequency (center frequency + ½ symbol rate) below 1/10th of the processing clock f_{clk_tx}. Note: as the AWGN noise samples are not frequency translated, noise tests should only be performed while the center frequency translation is smaller than the modulation bandwidth. REG23: LSB REG24 REG25 REG26: MSB

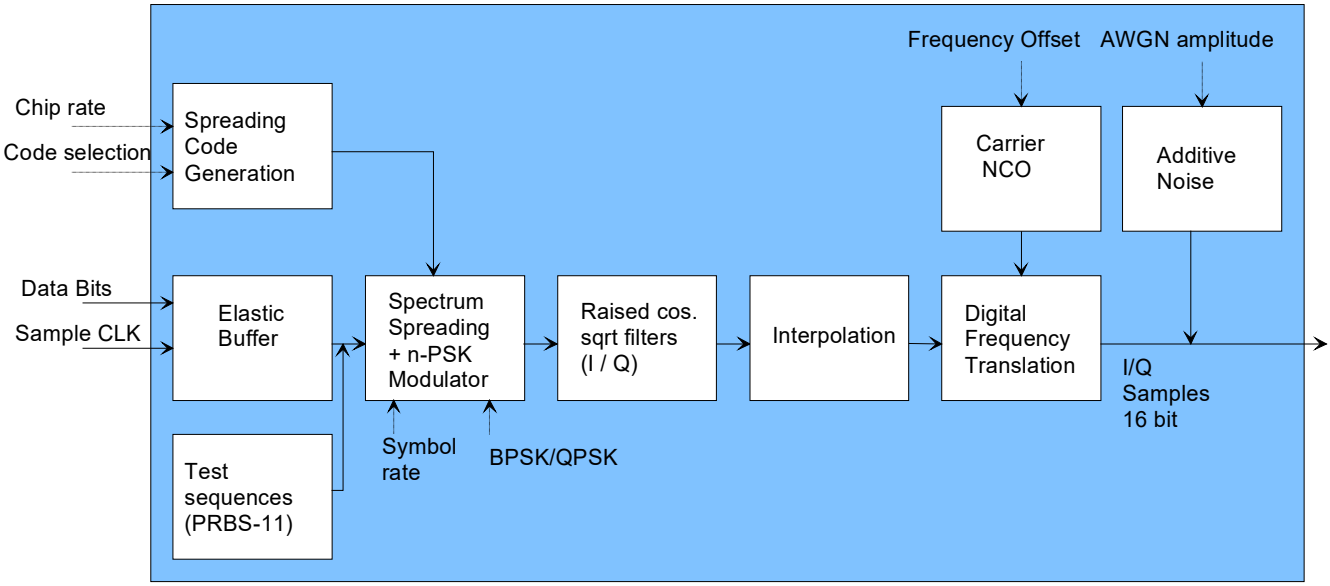
Network Interface	
Parameters	**Configuration**
Reserved	REG35 through 40 are reserved for the LAN MAC address. These registers are set at the time of manufacturing.
IP address (when connected to Gbit Ethernet PHY like **COM-5102, COM-5104**)	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG41: MSB REG42 REG43 REG44: LSB

Monitoring

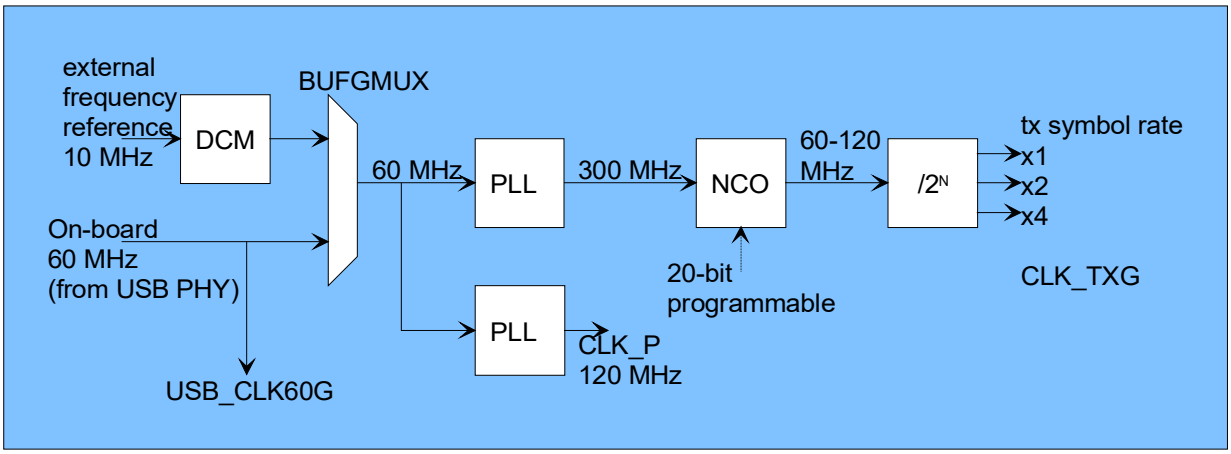
Status Registers

Parameters	**Monitoring**
USB PHY ID	Expect 0x24 when the USB PHY IC is SMSC USB3300 SREG7
Saturation	Denotes saturation in the transmit path. SREG8(0)
TCP-IP Connection Monitoring	
Parameters	**Monitoring**
TCP-IP connection on port 1024 (data stream)	Bit 0 = port 1028 (M&C) connected Bit 1 = port 1024 (data) connected 1 for connected, 0 otherwise SREG9(1:0)
LAN PHY ID	Expect 0x22 when the PHY IC is Micrel KSZ9021. SREG10(LSB)
SNR calibration	
Parameters	**Monitoring**
Measured modulated signal power	SREG11(LSB) SREG12 SREG13(MSB)
Measured AWGN power (Noise bandwidth is twice the modulated spread-spectrum signal bandwidth)	SREG14(LSB) SREG15 SREG16(MSB)

Block Diagram



Clocks generation



The code is written to accept a 10 MHz or a 60 MHz clock as frequency reference. On the target hardware, the 60 MHz clock originates from a USB PHY.

The code includes four clock domains:

1) 120 MHz general-purpose processing clock CLK_P
2) Modulator clock CLK_TXG related to the selected chip rate.
3) 60 MHz clock dedicated to the USB PHY
4) 2.5/25/125 MHz clock dedicated to the Ethernet LAN

A 20-bit NCO running at 300 MHz generates a modulator clock in the range 60 to 120 MHz. The modulator clock frequency is related to the chip rate: $f_{chip\ rate\ tx} = f_{clk\_tx} / 2^n$

Limitation and trade-off: Due to the lack of flexible programmable PLL in the Xilinx Spartan-6 family, we use a sub-optimal high-speed NCO which is afflicted by 3.3ns peak-peak jitter. This does not matter at low chip rates

when 3.3ns << chip period, but it creates some aliasing at high chip rates. A low-pass filter is used to clean the output spectrum.

Alternative: substituting the HIGH_SPEED_NCO component with a PLL eliminates the aliasing impairements but limits the symbol rate programmability to steps of 2. The substitute is also called high_speed_nco and is interface compatible.

Reference documents

[1] Specifications:
comblock.com/download/com1519.pdf

[2] Target platform schematics:
comblock.com/download/com_1500schematics.pdf

Configuration Management

The current software revision is 1.

[a] VHDL source code in directory:
com-1519\src\

[b] Xilinx ISE project file:
com-1519\com1519.xise

[c] .ucf constraint file example when used on the COM-1500 FPGA development platform:
com-1519\src\com1519?.ucf, where ? can be A through E depending on the firmware **OPTION**.

[d] test benches in directory:
com-1519\sim\

VHDL development environment

The VHDL software was developed using the following development environment:

(a) Xilinx ISE 13.4 with XST as VHDL synthesis tool
(b) Xilinx ISE Isim as VHDL simulation tool

Ready-to-use Hardware

The FPGA configurations (.mcs) are available in folder com-1519/bin for immediate use on the following Comblock hardware module:

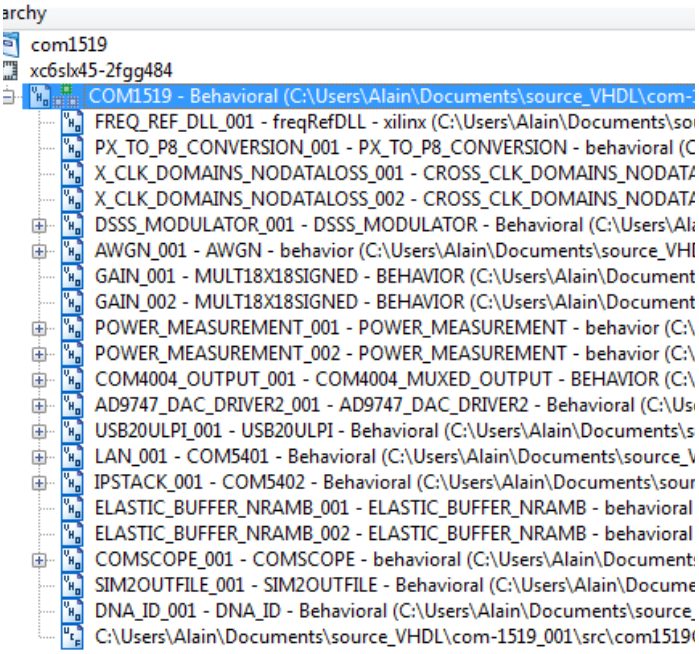
- COM-1500 FPGA + ARM + DDR2 SODIMM+ NAND + USB2 development platform

Xilinx-specific code

The VHDL source code was written in generic VHDL with few low-level Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- IBUFG
- BUFG
- BUFGMUX
- DCM_CLKGEN
- DCM_SP
- RAMB16_Sx_Sx
- ODDR2
- IDDR2
- IODELAY2

VHDL software hierarchy



The code is stored with one, and only one, entity per file as shown above.

The root program (highlighted) is *COM1519.vhd*.

The hierarchical nature of the VHDL code reflects the block diagram above:

- *COM1519* is the root program which includes the modulator *DSSS_MODULATOR.vhd*, the baseband interfaces (USB, TCP-IP, synchronous serial), several D/A converters interfaces, additive white Gaussian noise (*AWGN.vhd*) and ancillary monitoring and control functions (interface with microprocessor).
- The main Direct-Sequence Spread-Spectrum functions are encapsulated within *DSSS_MODULATOR.vhd*.
- Entity *CODEGEN.vhd* encapsulates all spreading codes.
- The frequency translation is implemented within *DIGITAL_DC2.vhd*. The frequency translation is realized in the form of a complex vector rotation, using sine/cosine lookup tables (*SIGNED_SIN_COS_TBL2.vhd*) and multipliers.
- Spectrum shaping is made by means of two root raised cosine filters *FIRRCOS20.vhd*, one for each complex axis. The filter is designed for two samples per symbol.
- The subsequent interpolation is implemented by concatenating half-band FIR filters *FIRHALFBAND3.vhd* and CIC interpolation filters *CIC_INTERP4.vhd*.
- The PRBS-11 pseudo-random test pattern is generated within the *LFSR11p.vhd* entity.
- A precise additive white gaussian noise is implemented using the Box-Muller algorithm within the *AWGN.vhd* entity.
- The *CROSS_CLK_DOMAINS_NODATALOSS.vhd* component is used to guarantee signal integrity (no glitches) when a signal crosses a clock domain.
- *POWER_MEASUREMENT.vhd* components measure the modulated signal power and the AWGN power for calibrating the SNR.

Device Utilization Summary

Device: Xilinx Spartan-6

OPTION –A (largest)		% (XC6SLX45)
Flip Flops	11887	21%
LUTs	12430	25%
RAMB16BWERs	36	31%
DSP48A1s	11	18%
GCLKs	8	50%
DCMs	3	37%
PLLs	1	25%

OPTION –D (smallest)		% (XC6SLX45)
Flip Flops	8995	16%
LUTs	8492	31%
RAMB16BWERs	21	18%
DSP48A1s	11	18%
GCLKs	8	50%
DCMs	3	37%
PLLs	1	25%

ComBlock Ordering Information

COM-1519SOFT DSSS MODULATOR

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