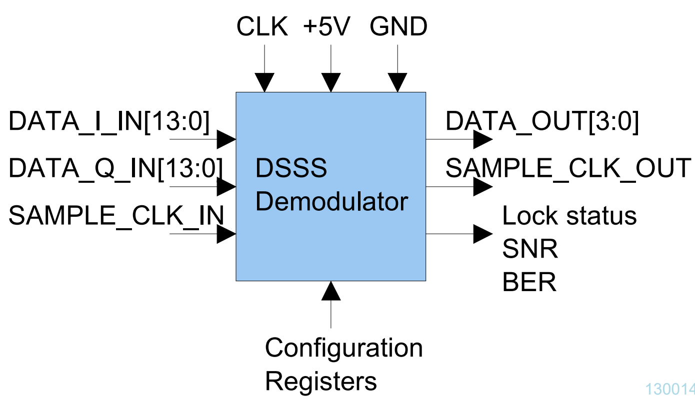
COM-1518 DIRECT SEQUENCE SPREAD-SPECTRUM DEMODULATOR 60 Mchip/s

Key Features

- Direct-Sequence Spread-Spectrum (DSSS) demodulation
- Variable chip rate up to 60 Mchips/s.
- Spreading codes: Gold, Maximal length, Barker, GPS C/A.
- BPSK, QPSK selectable.
- Continuous mode operation (i.e. Burst mode is not supported)
- Maximum processing gain: 33 dB
  Spreading factor: 3 to 2047
- Code period can be (significantly) longer than symbol period:
  Maximal code period: 65535
- 30-bin parallel code search for fast code acquisition.
- False code lock prevention.
- Accurate time of arrival pulse generated once per code period (can be used for round-trip delay measurement for example).
- Built-in Bit Error Rate measurement.
- Demodulation performances: within 1.5 dB from theory at threshold Eb/No of 2 dB.
- 4-bit soft-quantized demodulated bits to USB, LAN[1] or synchronous output.
- Monitoring:
  - Receiver lock
  - Carrier frequency error
  - SNR
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3"x 3" module for ease of prototyping. Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

Electrical Interface



[1] When used in conjunction with COM-5102

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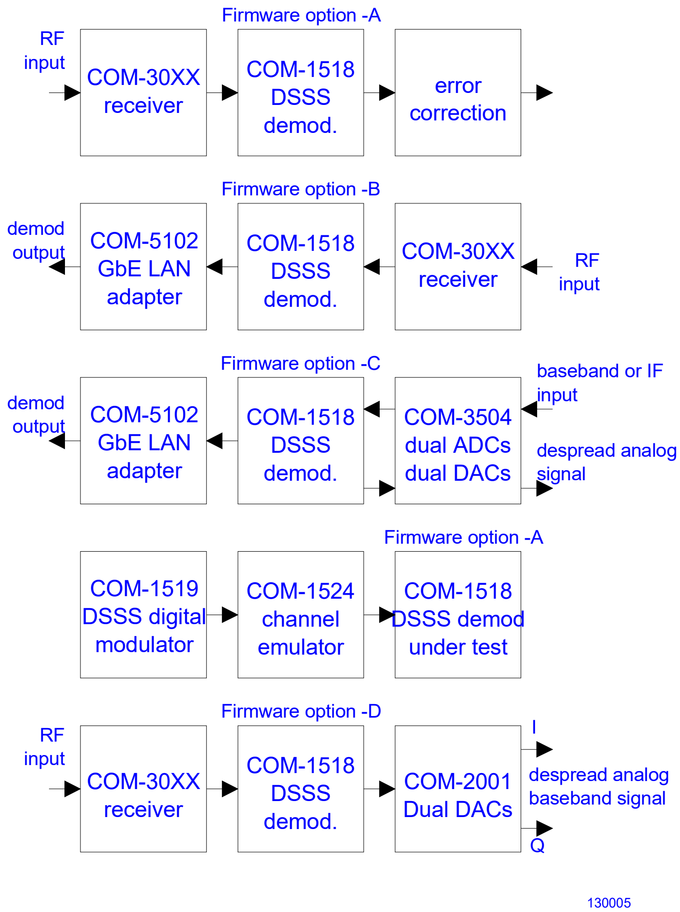
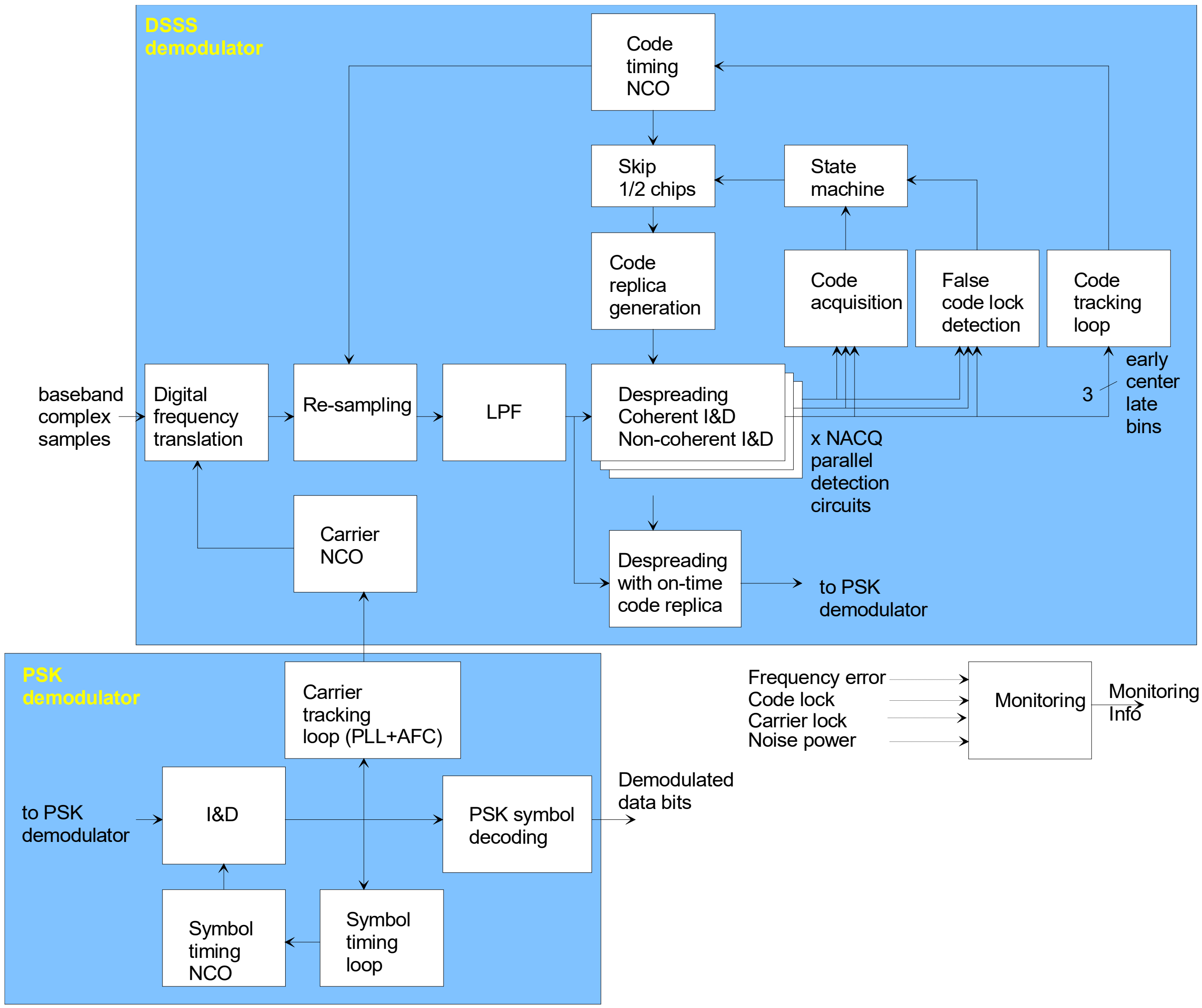
For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com1518.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

Typical Configurations



Block Diagram



Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB

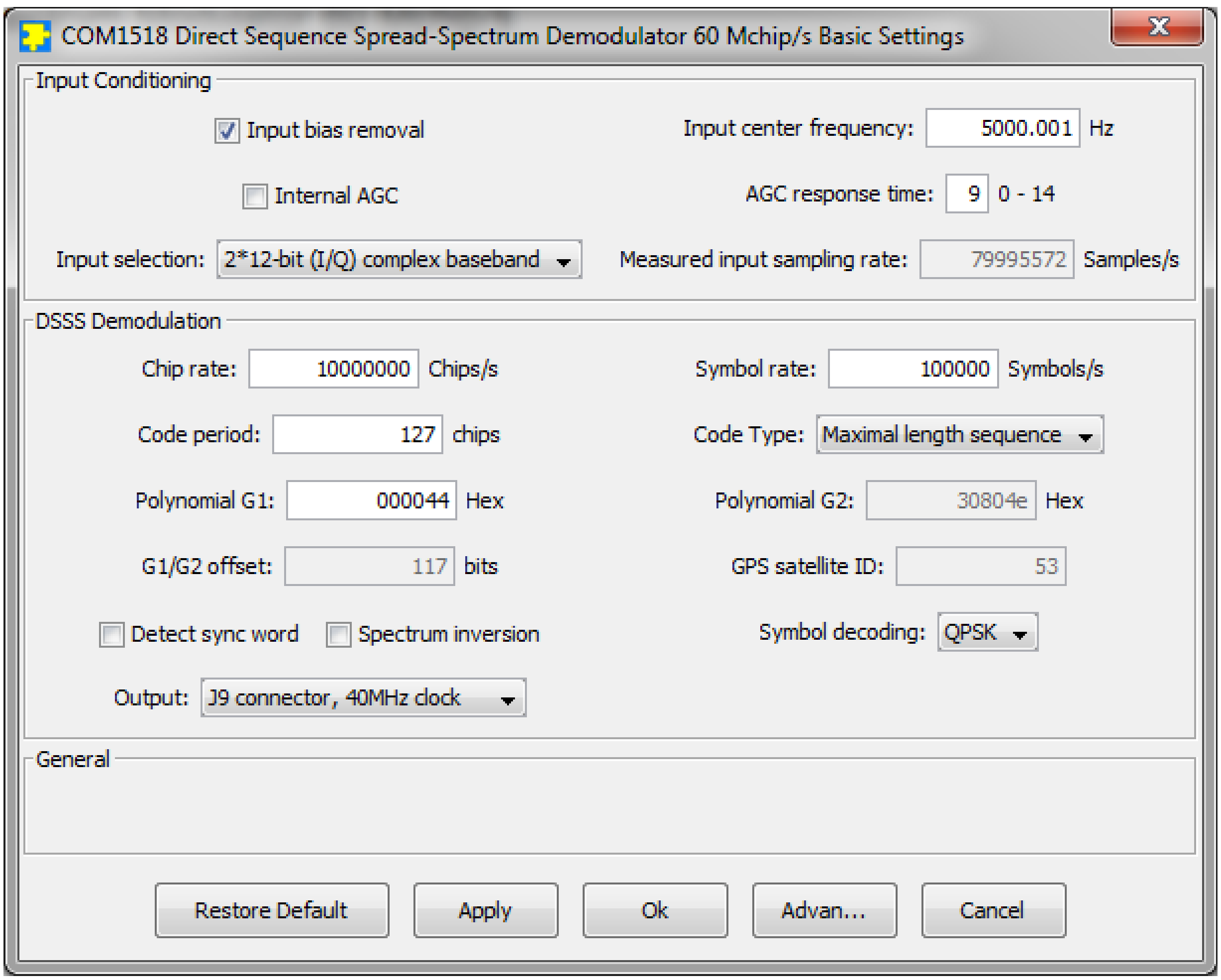
or connections via adjacent ComBlocks:

- USB, TCP-IP/LAN, Asynchronous serial (DB9), PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1518 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1518 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Several key parameters are computed on the basis of the 120 MHz internal processing clock f_{clk_p}: frequency translation, chip rate, etc.

Parameters	Configuration
Nominal input center frequency (f_c)	The nominal center frequency can be null (in the case of a baseband input signal) or non-zero in the case of an IF input signal. If the IF center frequency is sufficiently greater than the modulation bandwidth (chip rate), the Q input can be ignored and forced to zero, thus saving an ADC. This field can also be used for fine frequency corrections, for example to correct clock drifts. 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk\_p}$ REG1 = bits 7 – 0 (LSB[2]) REG2 = bits 15 – 8 REG3 = bits 23 – 16 REG4 = bits 31 – 24 (MSB)
Chip rate (fchip rate)	32-bit integer expressed as fchip rate $* 2^{32} / f_{clk\_p}$. The maximum practical chip rate is f_{clk_p} /2. Example 40 Mchips/s: 0x55555555 The maximum allowed error between transmitted and received chip rate is +/- 100ppm. REG5 = bits 7-0 (LSB) REG6 = bits 15 – 8 REG7 = bits 23 – 16 REG8 = bits 31 – 24 (MSB)
Code period	In chips. Valid range 3 – 65535 Can be less than the natural length of the selected code. In which case, the code is truncated.
	REG9 LSB REG10 MSB
Code selection	1 = Gold code 2 = Maximal length sequence 3 = Barker code (lengths 11 or 13 only) 4 = GPS C/A codes (use G2 as GPS PRN number) REG11(2:0)
Gold sequence / Maximal Length Sequence generator polynomial G1	24-bit. Describes the taps in the linear feedback shift register 1: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period $2^n - 1$. Example: $G1 = 1 + x + x^4 + x^5 + x^6$ is represented as 0x000039 This field is used only if Gold code or Maximal length sequences are selected. REG12 = bits 7 – 0 (LSB) REG13 = bits 15 – 8 REG14 = bits 23 – 16 (MSB)
Gold code generator polynomial G2	24-bit. Describes the taps in the linear feedback shift register 2: Same format as G1 above. This field is used only if Gold codes are selected. REG15 = bits 7 – 0 (LSB) REG16 = bits 15 – 8 REG17 = bits 23 – 16 (MSB)
Gold code G1/G2 phase offset	A Gold code is generated by adding two maximal length sequences (as defined by their generator polynomials G1 and G2). A set of orthogonal Gold codes can be created by changing the phase offset between the two maximal length sequences. REG18 = bits 7 – 0 (LSB) REG19 = bits 15 – 8 REG20 = bits 23 – 16 (MSB)
GPS satellite ID	GPS signals from different satellites are designated by a PRN signal number in the range 1 – 37. This field is used only if GPS C/A codes are selected. REG18(5:0)
Symbol rate f_{symbol_rate}	The symbol rate can be set independently of the spreading code period as $f_{symbol\_rate} * 2^{32} / f_{clk\_p}$ Limitation: the symbol rate must be higher than chip rate / 2047. REG21 = bits 7 – 0 (LSB) REG22 = bits 15 – 8 REG23 = bits 23 – 16 REG24 = bits 31 – 24 (MSB)

[2] LSB = Least Significant Byte
MSB = Most Significant Byte

Spreading factor (Processing gain)	Approximate (i.e truncated) ratio of chip rate / symbol rate Range: 3 – 2047 Note: to effectively achieve this processing gain, the code period must be longer than one symbol duration. REG25 = bits 7 – 0 (LSB) REG26(2:0) = bits 8 - 10
Spectrum inversion	Invert Q bit. (Inverts the modulated spectrum only, not the subsequent frequency translation) 0 = off 1 = on REG27(0)
BPSK / QPSK decoding	Note: the modulation symbol transitions are not necessarily aligned with the chip transitions. 0 = BPSK 1 = QPSK REG27(1)
Sync word detection	0 = disabled 1 = enabled Enable when the modulator sends a periodic synchronization sequence. The demodulator inherent phase ambiguity can only be removed if this feature is enabled at both modulator and demodulator. REG27(5)
Internal AGC	The code always acts as a level sensor for an external gain control actuator (for example RF or IF receiver gain control) to prevent saturation at the external A/D converter. When no such external gain control exists, a substitute internal gain control should be enabled here. Do not enable the internal AGC in the case of IF undersampling as it may cause instabilities. 0 = internal AGC enabled 1 = internal AGC bypassed REG27(6)
Baseband or IF input	0 = baseband input (I/Q complex samples) 1 = IF input (I as real input, Q is ignored) REG27(7)
Bias removal enable	The bias removal circuit removes any spurious DC bias that may be introduced by an external A/D convert. Disable this function if the input signal includes a legitimate DC offset. 0 = disable 1 = enable REG28(0)
AGC response time	Users can to optimize AGC response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and chip rate). The AGC_DAC gain control signal is updated as follows 0 = every chip, 1 = every 2 input chips, 2 = every 4 input chips, 3 = every 8 input chips, etc…. 10 = every 1000 input chips. Valid range 0 to 14. REG29(4:0)
Demodulated output selection	1 = J9 connector , 40 MHz clock. I/Q serialized when QPSK. 2 = USB, 1-bit hard quantized, packed into 8-bit bytes, MSb first. 3 = USB, 4-bit soft-quantized, packed into 8-bit bytes. 4 = LAN/TCP(port 1028), 1-bit hard quantized, packed into 8-bit bytes, MSb first. 5 = LAN/TCP(port 1028), 4-bit soft-quantized, packed into 8-bit bytes. 6 = despread I/Q samples, 120 MS/s REG32(2:0)
Enable test points	Enable (1)/Disable (0) test points on J6 connector REG32(7)

Network Interface	
Parameters	**Configuration**
Reserved	REG35 through 40 are reserved for the LAN MAC address. These registers are set at the time of manufacturing.
IP address (when connected to Gbit Ethernet PHY like **COM-5102, COM-5104**)	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG41: MSB REG42 REG43 REG44: LSB

(Re-)Writing to the last control register REG44 is recommended after a configuration change to enact the change.

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-7 Properly operating hardware will result in the following sequence being displayed: SREG0/1/2/3/4/5/6 = 2C F1 95 xx 0F 01 24. SREG7 is 22 when LAN adapter is plugged in.
Input sampling rate	The input sampling rate is measured and displayed here. The frequency measurement accuracy is a function of the internal clock stability. The measurement is expressed in Hz. SREG8 = bit 7-0 (LSB) SREG9 = bit 15 – 8 SREG10 = bit 23 – 16 SREG11(2:0) = bit 26 – 24 (MSB)
AGC	Front-end AGC gain settings. 12-bit unsigned. Inverted (0 for maximum gain) SREG12 (LSB) SREG13(3:0) (MSB)
Decimation factor R	Internal decimation ratio based on the input sampling rate and the specified chip rate. SREG14 (LSB) SREG15 (MSB)
Carrier frequency offset	Residual frequency offset with respect to the nominal carrier frequency. 24-bit signed integer expressed as fcdelta * * 2^{24} / f_{clk_p} SREG16 = bits 7 – 0 (LSB) SREG17 = bits 15 – 8 SREG18 = bits 23 – 16 (MSB)
Carrier lock status	SREG20(0) 0 = unlocked 1 = locked
Code lock status	SREG20(1) 0 = unlocked 1 = locked
Signal presence (from FFT)	SREG20(2) 0 = not present 1 = present
SOF lock status	Detect presence of periodic sync word when enabled. SREG20(3) 0 = unlocked 1 = locked
Despread signal power S	Average signal power after despreading. Compute the signal to noise ratio after despreading as S/N. The absolute value is meaningless because of multiple agcs.

	SREG21 = bits 7 – 0, LSB SREG22 = bits 15 – 8, MSB
Noise power N	Average noise power. Used to compute the SNR after despreading. The absolute value is meaningless because of multiple agcs. SREG23 = bits 7 – 0, LSB SREG24 = bits 15 – 8, MSB
SNR	2*(S+N)/N ratio, valid only during code lock. Linear (not in dBs). Fixed point 14.2 SREG25 (LSB) SREG26 (MSB)
Bit error rate	Monitors the BER (number of bit errors over 1,000,000 received bits) when the modulator is sending a PRBS-11 test sequence. SREG27: LSB SREG28: SREG29: SREG30: MSB
BER tester synchronized	SREG31(0): 1 when the BERT is synchronized with the received PRBS-11 test sequence.
TCP-IP Connection Monitoring	
Parameters	**Monitoring**
LAN PHY ID	Expect 0x22 when LAN adapter is plugged in. SREG7
MAC address	Unique 48-bit hardware address (802.3). In the form SREG32:SREG33:SREG34:…:SREG37
TCP-IP connections	Bit 0 = port 1028 (M&C) connected Bit 1 = port 1024 (data) connected 1 for connected, 0 otherwise SREG38(1:0)

Multi-byte status variables are latched upon (re-)reading SREG7.

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. Click on the button to start, then select the signal traces and trigger are defined as follows:

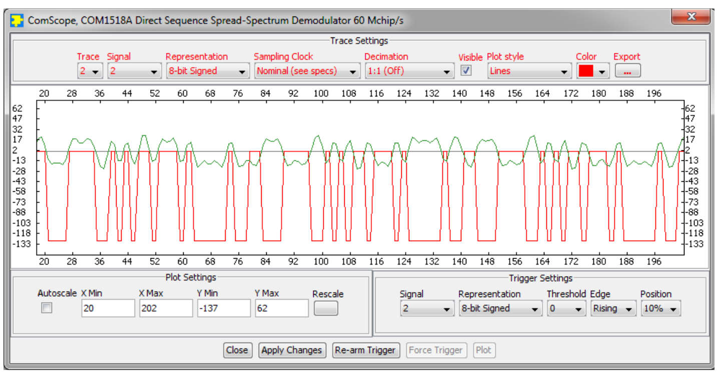
Trace 1 signals	Format	Nominal sampling rate	Buffer length (samples)
1: Input signal I-channel	8-bit signed	Input sampling rate	512
2: Input signal (I-channel) after AGC, frequency translation, decimation	8-bit signed	Input sampling rate/R	512
3: Despread I-channel, center, after I&D	8-bit signed	2 samples / symbol	512
4: front-end AGC	8-bit unsigned	1 sample / symbol	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input signal Q-channel	8-bit signed	Input sampling rate	512
2: Code replica. Compare with spread input signals	8-bit signed	2 samples/chip	512
3: Demodulated I-channel	8-bit signed	1 sample / symbol	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: spread I-channel after carrier tracking and channel LPF	8-bit signed	2 samples/chip	512
2: Code tracking phase correction (accumulated)	8-bit signed	2 samples / symbol	512
3: Carrier tracking phase	8-bit signed	Input sampling rate/R	512
4: Symbol tracking phase (accumulated)	8-bit signed	1 sample / symbol	512
Trace 4 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: 2(S+N)/N after despreading. Valid only if code is locked. Linear (i.e. not in	8-bit unsigned	f_{clk}	512

dBs)			
2: Averaged signal power (valid only during code tracking)	8-bit signed	f_{clk}	512
3: Averaged noise power (valid only during code tracking)	8-bit signed	f_{clk}	512
Trigger Signal	**Format**		
1: Start of code replica	Binary		
2. Code Lock	Binary		

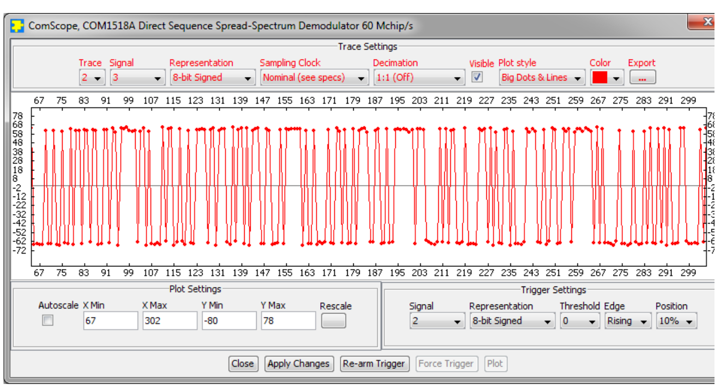
Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk} processing clock as real-time sampling clock.

In particular, selecting the f_{clk} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope example, showing code lock with aligned: received spread signal after RRC filter (green) vs code replica (red)



ComScope example: showing demodulated I-channel

Digital Test Points

Enabled if REG32(7) = '1', high-impedance otherwise.

Test Point	Definition
J6/A29	Recovered carrier/center frequency (coarse)
J6/A30	Carrier lock
J6/A31	Code lock
J6/A32	Recovered carrier/center frequency (fine)
J6/A33	Recovered symbol clock
J6/A34	Start of spreading code replica (compare with start of spreading code at the modulator)
J6/A35	Spreading code replica
J6/A36	Spread I signal (MSB) (compare with spreading code replica above)
J6/A37	BER tester synchronized
J6/A38	Byte error detected by BER tester

Operation

Spreading codes

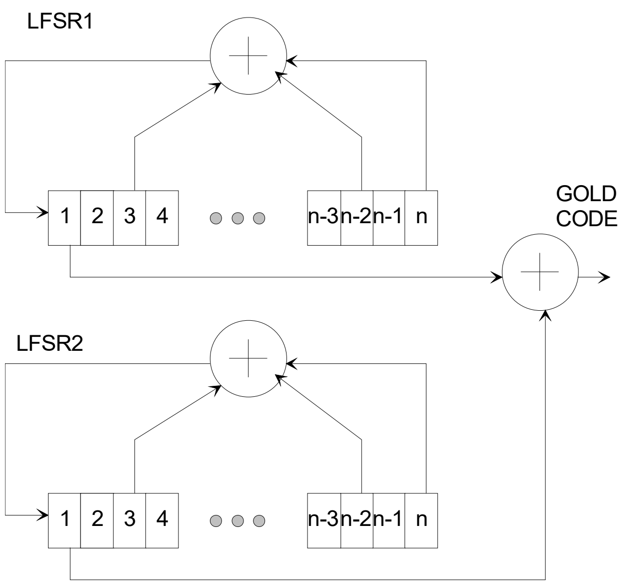
Spreading codes are pseudo random sequences which falls within the following categories:

- Gold sequences, for best autocorrelation properties
- Maximal length sequences
- Barker codes (length 11, 13)
- GPS C/A codes.

The same spreading code is used on both the in-phase (I) and quadrature (Q) channels.

Gold sequences

Gold sequences are generated using two linear feedback shift registers LFSR1 and LFSR2 as illustrated below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its two generator polynominals. The highest order is n. The generator polynominals are user programmable.

A few commonly used Gold sequences are listed below:

n = 5 (length 31):
G1 = $1 + x^2 + x^5$ (0x000012)
G2 = $1 + x + x^2 + x^4 + x^5$ (0x00001B)

n = 6 (length 63):
G1 = $1 + x^5 + x^6$ (0x000030)
G2 = $1 + x + x^4 + x^5 + x^6$ (0x000039)

n = 7 (length 127):
G1 = $1 + x^3 + x^7$ (0x000044)
G2 = $1 + x + x^2 + x^3 + x^4 + x^5 + x^7$ (0x00005F)

n = 9 (length 511):
G1 = $1 + x^5 + x^9$ (0x000110)
G2 = $1 + x^3 + x^5 + x^6 + x^9$ (0x000134)

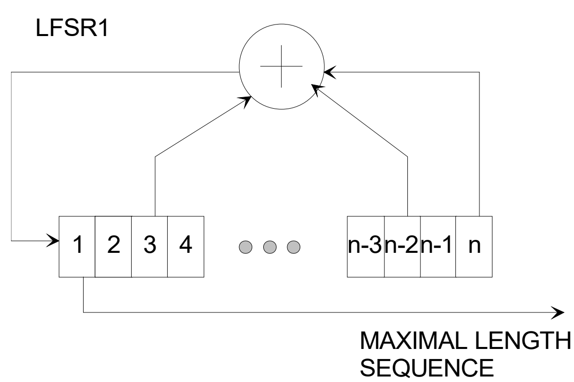
n = 10 (length 1023):
G1 = $1 + x^7 + x^{10}$ (0x000240)
G2 = $1 + x^2 + x^7 + x^8 + x^{10}$ (0x0002C2)

n = 11 (length 2047):
G1 = $1 + x^9 + x^{11}$ (0x000500)
G2 = $1 + x^3 + x^6 + x^9 + x^{11}$ (0x000524)

n = 17 (length 131071):
G1 = $1 + x^3 + x^6 + x^7 + x^9 + x^{10} + x^{14} + x^{16} + x^{17}$ (0x01A364)
G2 = $1 + x^9 + x^{13} + x^{14} + x^{17}$ (0x013100)

Maximal length sequences

Maximal length sequences are generated using one linear feedback shift register LFSR1 as shown below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its generator polynominal. The highest order is n. The generator polynominal is user programmable.

A few commonly used maximal length sequences are listed below:

n = 4 (length 15):
$G1 = 1 + x + x^4$ (0x000009)
n = 5 (length 31):
$G1 = 1 + x^2 + x^5$ (0x000012)
n = 6 (length 63):
$G1 = 1 + x + x^6$ (0x000021)
n = 7 (length 127):
$G1 = 1 + x + x^7$ (0x000041)
n = 8 (length 255):
$G1 = 1 + x^2 + x^3 + x^4 + x^8$ (0x00008E)
n = 9 (length 511):
$G1 = 1 + x^4 + x^9$ (0x000108)
n = 10 (length 1023):
$G1 = 1 + x^3 + x^{10}$ (0x000204)

Barker Codes

11 bit Barker code: 101 1011 1000, or 0x5B8
13 bit Barker code: 1 1111 0011 0101, or 0x1F35

The length (11 or 13) must be entered as spreading factor in REG4/5.

GPS C/A Codes

GPS C/A codes are modified Gold codes of length 1023 with generator polynomials:
$G1 = 1 + x^3 + x^{10}$
$G2 = 1 + x^2 + x^3 + x^6 + x^8 + x^9 + x^{10}$

The G2 generator output is slightly modified so as to create a distinct code for each satellite. The G2 output is generated by summing two specific taps of the shift register. In the case of Satellite ID 1 for example, taps 2 and 6 are summed.

The G2 output taps are listed below:

Satellite ID / GPS PRN Signal Number	G2 output taps selection	Satellite ID / GPS PRN Signal Number	G2 output taps selection
1	2 xor 6	21	5 xor 8
2	3 xor 7	22	6 xor 9
3	4 xor 8	23	1 xor 3
4	5 xor 9	24	4 xor 6
5	1 xor 9	25	5 xor 7
6	2 xor 10	26	6 xor 8
7	1 xor 8	27	7 xor 9
8	2 xor 9	28	8 xor 10
9	3 xor 10	29	1 xor 6
10	2 xor 3	30	2 xor 7
11	3 xor 4	31	3 xor 8
12	5 xor 6	32	4 xor 9
13	6 xor 7	33	5 xor 10
14	7 xor 8	34	4 xor 10
15	8 xor 9	35	1 xor 7
16	9 xor 10	36	2 xor 8
17	1 xor 4	37	4 xor 10
18	2 xor 5		
19	3 xor 6		
20	4 xor 7		

Compliant with “Navstar GPS Space Segment / Navigation User Interfaces” specifications, ICD-GPS-200, Revision C. IRN-200C-004, 12 April 2000.

Symbol Rate

The demodulation symbol rate is independent of the chip rate and code period. The demodulator includes an autonomous symbol tracking loop, separate from the code tracking loop.
However, the full spread-spectrum processing gain can only be achieved if the code period is greater than the symbol period.

Frequency Tracking

The demodulator comprises a phase locked loop (PLL) and FFT-based frequency acquisition circuit. Once the code is locked, the frequency acquisition circuit detects and corrects a maximum initial frequency error of +/- chip_rate / 256.

Once locked, the carrier tracking loops tracks the carrier phase over a very wide frequency range.

Note: the minimum practical symbol rate is such that (symbol_rate/200) > (chip_rate/(256*2048)). Reason: the Costas carrier tracking loop must be able to acquire any frequency error remaining after the initial frequency acquisition.

Code Tracking Loop

The code tracking loop is a coherent delay lock loop (DLL) of the 1^{st} order.

Code Acquisition

30 parallel detectors search for code aligment during the code acquisition phase. During the subsequent code tracking phase, 3 detectors track the early/center/late code while the other 27 detectors scan for false lock. The detectors are staggered ½ chip apart.

Detection is performed in two steps: first a coherent detector averages the despread signal over ½ a symbol period. The result is squared and further averaged over 25 symbols.

Variable decimation

This module is designed to work over a wide range of chip rates. It includes a variable decimation filter at the input to prevent aliasing when resampling at low chip rates. The optimum decimation ratio is set automatically.

Front-End AGC

The purpose of this AGC is to prevent saturation at the input signal A/D converters while making full use of the A/D converters dynamic range. Therefore, AGC reacts to the composite input signal which may comprise not only the useful signal but also adjacent channel interferers and noise. The principle of operations is outlined below:

(a) The peak magnitude of the complex input samples in any symbol period is computed and continuously averaged. The length of averaging depends on the AGC response parameter set by the user.

(b) The average magnitude is compared with a target magnitude threshold and the AGC gain is adjusted accordingly.

(c) An analog gain control signal AGC_OUT is generated either by a 12-bit DAC or a 10-bit PWM, depending on the connectivity and firmware option.

(d) If the external receiver has its own local AGC or does not feature a gain control input, then the COM-1518 AGC loop should be set as 'internal'.

Options

Several interface types are supported through multiple firmware options. All firmware versions can be downloaded from

http://www.comblock.com/download.html

Changing the firmware option requires loading the firmware once using the ComBlock control center, then switching between the stored firmware versions The selected firmware option is automatically reloaded at power up or upon software command within 1.2 seconds

Option	Definition
-A	Left (J6) connector: complex or real baseband input sampled signal. 2*12-bit clock synchronous (compatible with COM-30xx receivers) Right (J9) connector: 4-bit soft-quantized demodulated output, synchronous serial
-B	Left (J6) connector: GbE LAN adapter interface (compatible with COM-5102 adapters) Right (J9) connector: complex or real baseband input sampled signal. 2*12-bit clock synchronous (compatible with COM-30xx receivers)
-C	Left (J6) connector: GbE LAN adapter interface (compatible with COM-5102 adapters) Right (J9) connector: analog baseband I/O. (compatible with COM-3504 dual Analog<->Digital conversion)
-D	Left (J6) connector: complex or real baseband input sampled signal. 2*12-bit clock synchronous (compatible with COM-30xx receivers) Right (J9) connector: despread output to an external dual DAC, 2*10-bit clock synchronous. (compatible with COM-2001 dual DAC)

Recovery

This module is protected against corruption by an invalid FPGA configuration file (during firmware upgrade for example) or an invalid user configuration. To recover from such occurrence, connect a jumper in JP1 position 2-3 prior and during power-up. This prevents the FPGA configuration and restore communication. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

Troubleshooting Checklist

Demodulator can't achieve lock even at high signal-to-noise ratios:

- Make sure the modulator baseband I/Q signals do not saturate, as such saturation would strongly distort the modulation phase information. (this is a phase demodulator!)

Demodulator can demodulate BPSK but not QPSK:

- A spectrum inversion may have occurred in the RF transmission chain. If so, invert the spectrum inversion flag at the demodulator.

Interfaces

Input Interface	Definition
DATA_I_IN[11:0]	Modulated input signal, real axis. 12-bit precision unsigned. Unused LSBs are pulled low. LVTTL 0 – 3.3V
DATA_Q_IN[11:0]	Modulated input signal, imaginary axis. Same format as DATA_I_IN.
SAMPLE_CLK_IN	Input signal sampling clock. One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = '1'. Samples can be consecutive. Signal is pulled-up. LVTTL 0 – 3.3V
AGC1_OUT	Output. When this demodulator is connected directly to an analog receiver, it generates an analog or PWM signal to control the gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain.
CLK_IN	Input reference clock for synchronous I/O. DATA_x_IN and SAMPLE_CLK_IN are read at the rising edge of CLK_IN. Maximum 120 MHz.

Demodulated Output	Definition
DATA_I_OUT[3:0]	4-bit soft-quantized demodulated bits, real axis. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'. When the serial output mode is selected, I and Q samples are transmitted one after another on this interface. I is transmitted before Q.
DATA_Q_OUT[3:0]	4-bit soft-quantized demodulated bits, imaginary axis. Same format as DATA_I_OUT. When the serial output mode is selected, this interface is unused.
SAMPLE_CLK_OUT	Demodulated bit clock. One CLK-wide pulse. Read the output signal at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.
RX_LOCK	'1' when the demodulator is locked, '0' otherwise. The lock status is based on the code lock.
CLK_OUT	40 MHz output reference clock.

Monitoring Output	Definition
DESPREAD_I[9:0]	Output I-channel signal after channel filtering, despreading, integrate and dump. 10-bit precision unsigned. Can drive a COM-2001 dual D/A converter. LVTTL 0 – 3.3V
DESPREAD_Q[9:0]	Q-channel. Same format as DESPREAD_I
DESPREAD_CLK	Output signal sampling clock. One CLK-wide pulse once per symbol. Read the output signal at the rising edge of CLK when DESPREAD_CLK = '1'.
CLK_P	90 MHz output clock (internal processing clock).

Power Interface	4.75 – 5.25VDC. Terminal block. 250 mA typ.

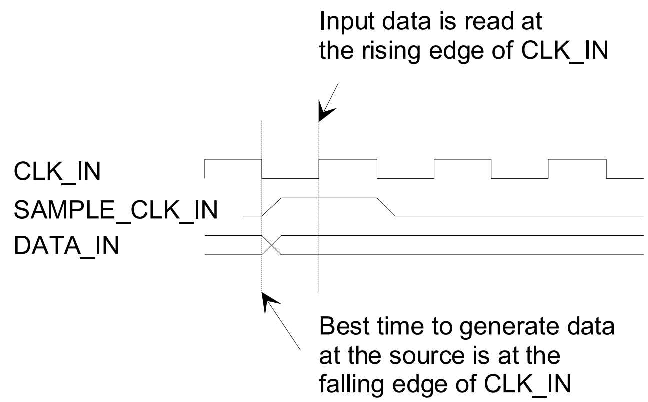
Absolute Maximum Ratings

Supply voltage	-0.5V min, +6V max
40-pin connector inputs (when configured as LVTTL)	-0.5V min, +3.6V max

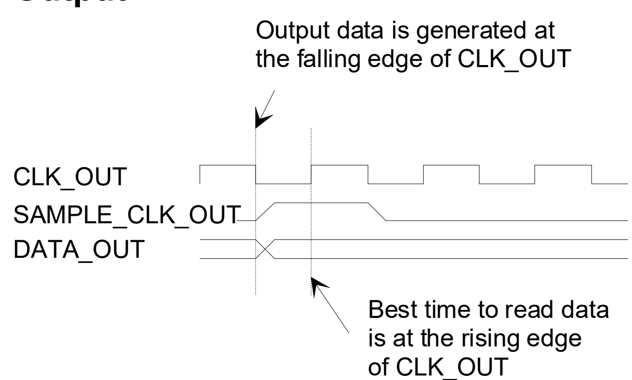
Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Timing

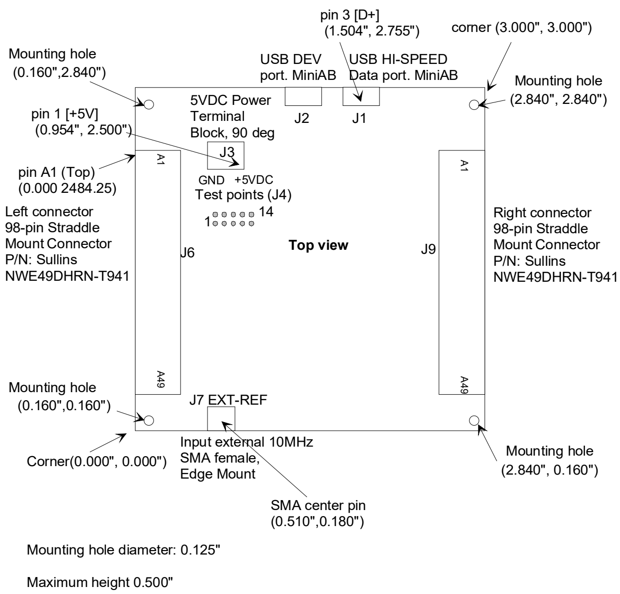
Input



Output



Mechanical Interface



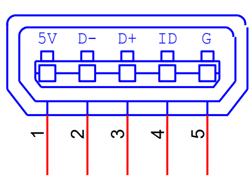
Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1500schematics.pdf

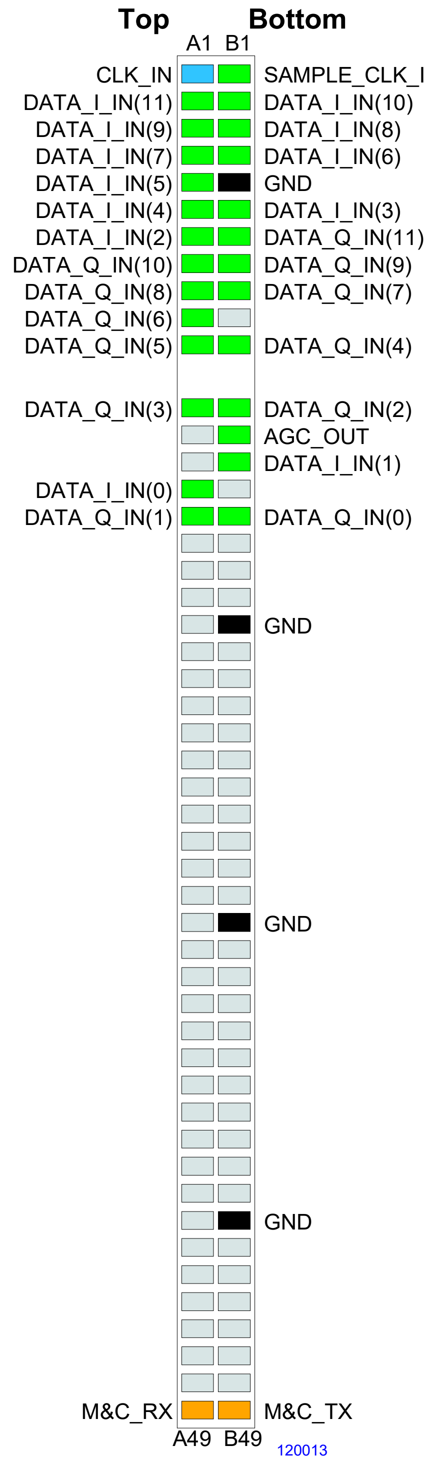
Pinout

USB

Both USB ports are equipped with mini type AB connectors. (G = GND). In both cases, the COM-1524 acts as a USB device.

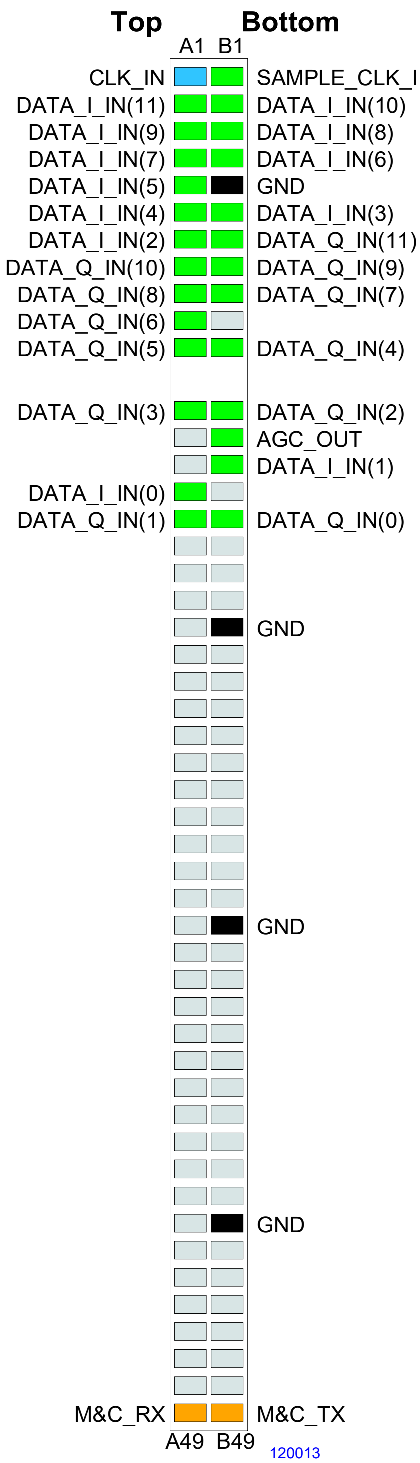


Left Connector J6

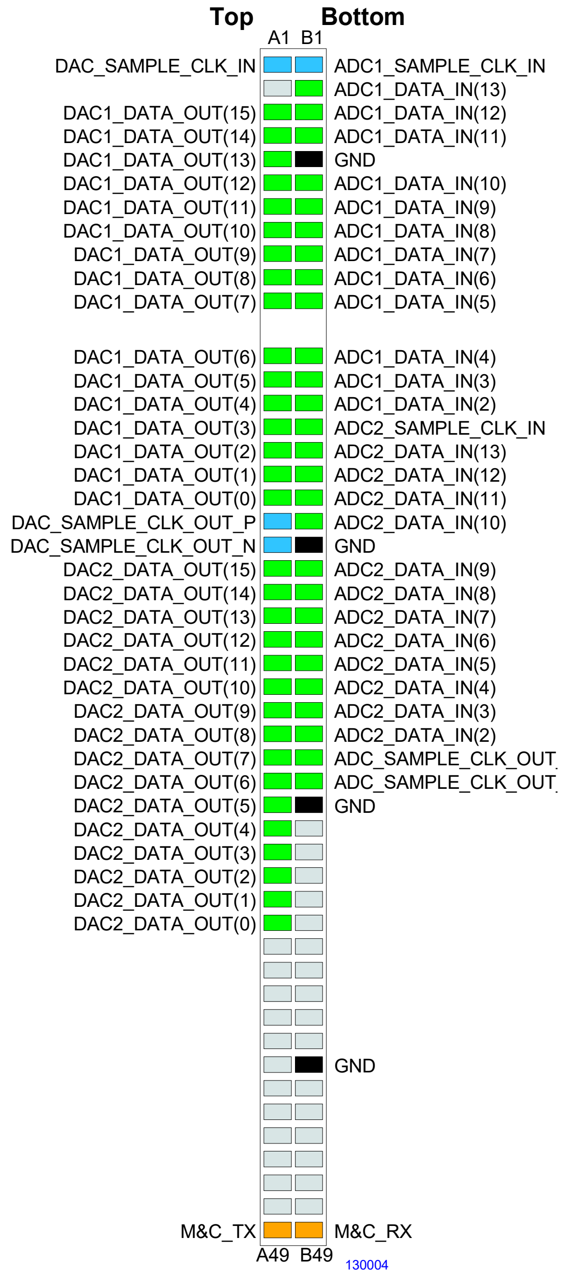


Firmware Option **-A**. Input compatible with COM-30xx receivers.

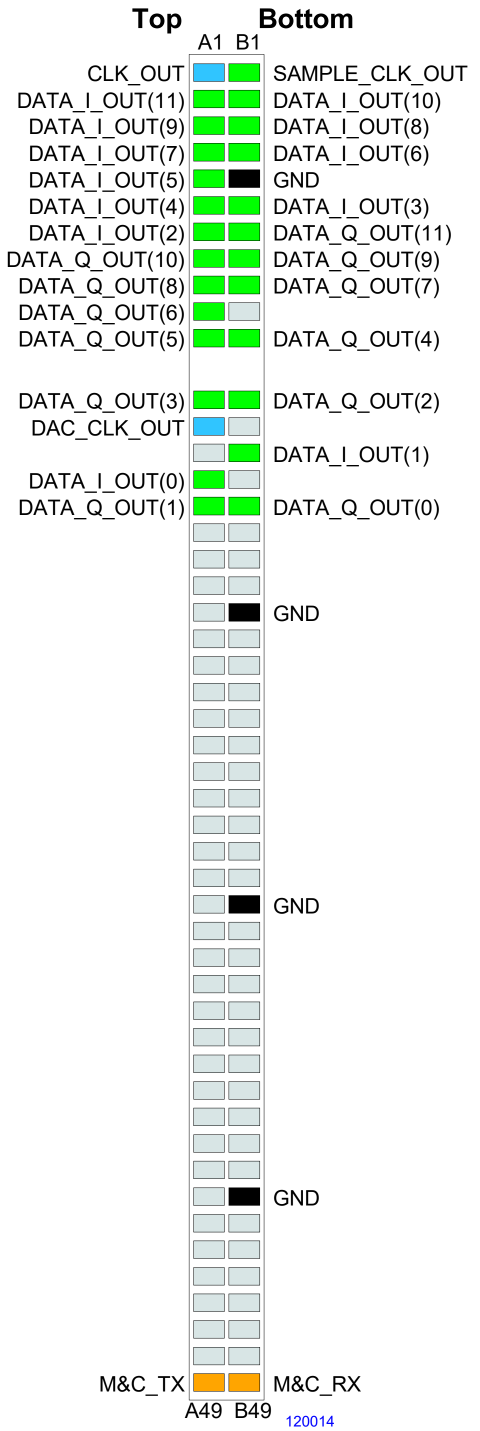
Right Connector J9



Firmware Option **-B**. 2*12-bit input samples.
Input compatible with COM-30xx receivers.



Firmware Option **-C**. 2*16-bit output samples, 2*12-bit input samples. This interface is compatible with the COM-3504 dual Analog<->Digital Conversions.



Firmware Options **–D**. 2*12-bit output samples. This interface is compatible with the COM-2001 dual 10-bit DACs.

I/O Compatibility List

(not an exhaustive list)

Left connector (J6)
COM-5102 Gigabit Ethernet + HDMI interface
COM-5401 4-port 10/100/1000 Mbps Ethernet Transceivers (limited to one port)
COM-30xx RF/IF/Baseband receivers for frequencies ranging from 0 to 3 GHz.
COM-1524 channel emulator
COM-1519 DSSS modulator (back to back)
COM-1800/1500 FPGA + ARM development platforms
Right connector (J9)
COM-3504 Dual Analog <-> Digital Conversions 2*16-bit 250 MSamples/s
COM-30xx RF/IF/Baseband receivers for frequencies ranging from 0 to 3 GHz.
COM-2001 Digital-to-Analog Conversion, Baseband 2*10-bit 125 MSamples/s
COM-1524 channel emulator
COM-1509 Error correction codec 120Mbits/s
COM-7002 Turbo code decoder
COM-1519 DSSS modulator (back to back)
COM-1600/1500 FPGA + ARM development platforms

Configuration Management

This specification is to be used in conjunction with VHDL software revision 5 and ComBlock control center revision 3.09d and above.

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1518 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

Comparison with Previous ComBlocks

Key Improvements with respect to COM-1418 Direct-Sequence Spead-Spectrum Demodulator
- Support for IF undersampling (real) input - 2x faster: maximum chip rate is fclk/2 - Independent chip rate and symbol rate: symbol duration and alignment are independent of the spreading code period (2 independent tracking loops for code and symbol timing) - Higher symbol rate (60 Mchips/s) - Variable decimation and anti-aliasing filtering - Faster code acquisition through parallel code acquisition (30 parallel cells) instead of sequential search. - Faster center frequency acquisition through FFT. - Better performance through reduced dependencies between loops: code acquisition is less dependent on center frequency error. - Independent AGCs before and after despreading. - Phase ambiguity resolution under control of external FEC decoder.

ComBlock Ordering Information

COM-1518 Direct sequence spread-spectrum demodulator. 60 Mchip/s.

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