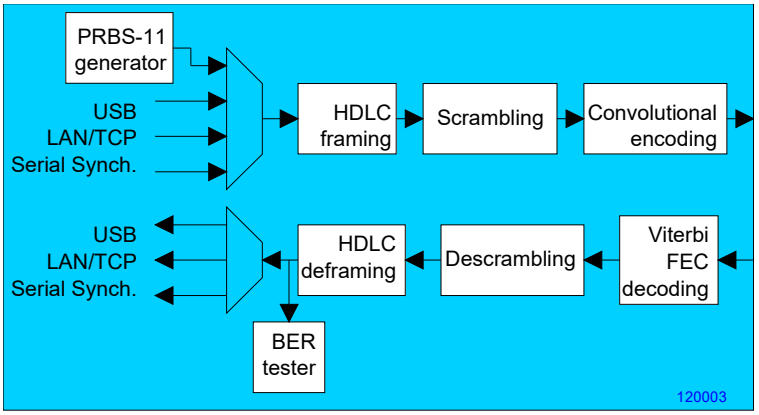
COM-1509 ERROR CORRECTION CODEC

Key Features

- Bi-directional error correction encoder/decoder, including
  - Convolutional encoding/Viterbi decoding
  - V.35 scrambling/descrambling
  - Serial HDLC framing/deframing
- Convolutional codec with selectable rate and constraint lengths:
  K = 5, rate 1/7
  K = 7, rates 1/2, 2/3, 3/4, 5/6, 7/8
  K = 9, rates 1/3, 1/2, 2/3
- Differential decoder to resolve bit stream inversion.
- Maximum encoded output and coded input rates: 120 Mbps (for K=5, 7), 90 Mbps (K=9).
- 4-bit soft-quantized or 1-bit hard decision coded input.
- Built-in test tools:
  - PRBS-11 test sequence generation
  - BER measurement (coded, decoded)
- Single 5V supply with overvoltage, reverse voltage and surge protection. Connectorized 3"x 3" module for ease of prototyping. Standard 98 pin PCIe high-speed connectors (left, right). Interfaces with 3.3V LVTTL logic.

Block Diagram



For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1509.pdf.

These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

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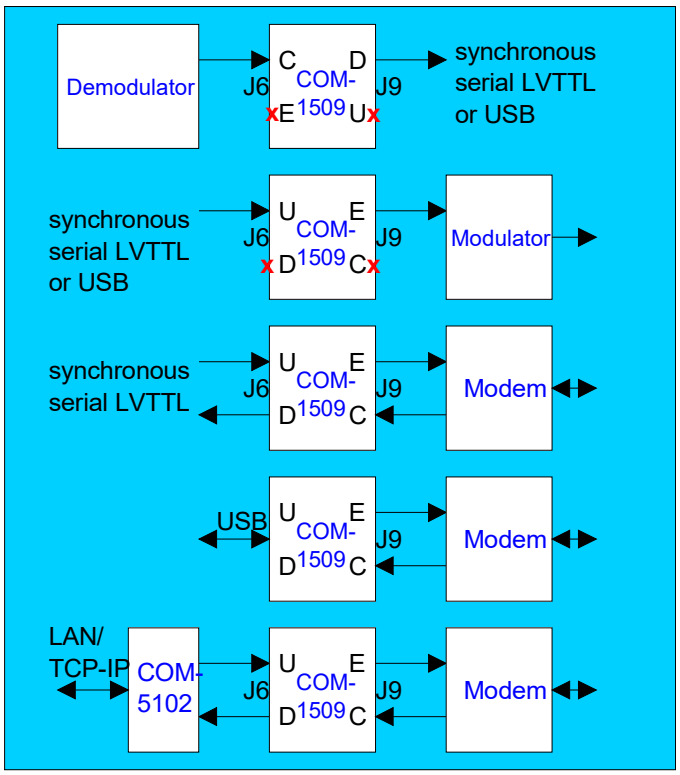
Inputs/Outputs



U = uncoded input
E = encoded output
C = coded input
D = decoded output

120004

Throughout this document, (**U**) refers to the Uncoded encoder input, (**E**) refers to the Encoded encoder output, (**C**) refers to the Coded decoder input and (**D**) to the Decoded decoder output.

Electrical Interface

Synchronous serial interface. Decoder input	**Definition**
DATA_C_IN[3:0]	4-bit soft-quantized demodulated bits. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'. Can also be configured for 1-bit hard-quantized input, in which case only bit 3 is used. Read at the rising edge of CLK_C_IN
SAMPLE_C_CLK_IN	Enable signal.
	Read at the rising edge of CLK_C_IN
SOF_C_IN	Optional start of frame reset input. Used only in block mode. Ignored in continuous mode. 1 CLK-wide pulse. Aligned with SAMPLE_C_CLK_IN.
CLK_C_IN	Synchronous clock for coded input. Maximum speed is 120 MHz.
Output Module Interface	**Definition**
DATA_OUT	Output data stream. 1-bit serial
SAMPLE_CLK_OUT	Output symbol clock. One CLK-wide pulse. Read the output signals at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.
Other Digital Modem Interfaces	**Definition**
USB 2.0	Mini type AB connector. This interface supports two virtual channels: one for monitoring and control, the other to convey information data between the modem and a host computer.
LAN / TCP-IP	Networking requires an additional 10/100/1000 Mbps Ethernet adapter (COM-5102 or COM-5401) plugged in the left (J6) connector. The COM-1504 includes a TCP-IP server, awaiting a remote client connection at port 1024.
Power Interface	4.75 – 5.5VDC. Terminal block. Power consumption is approximately proportional to the symbol clock rate (f_{symbol_clk}). The maximum power consumption is TBDmA.

Nominal Operation

Supply voltage	+4.75 to +5.25 VDC

Absolute Maximum Ratings

Supply voltage	-16V min, +16V max
98-pin connector inputs	-0.5V min, +3.6V max

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB
- Asynchronous serial (LVTTL)

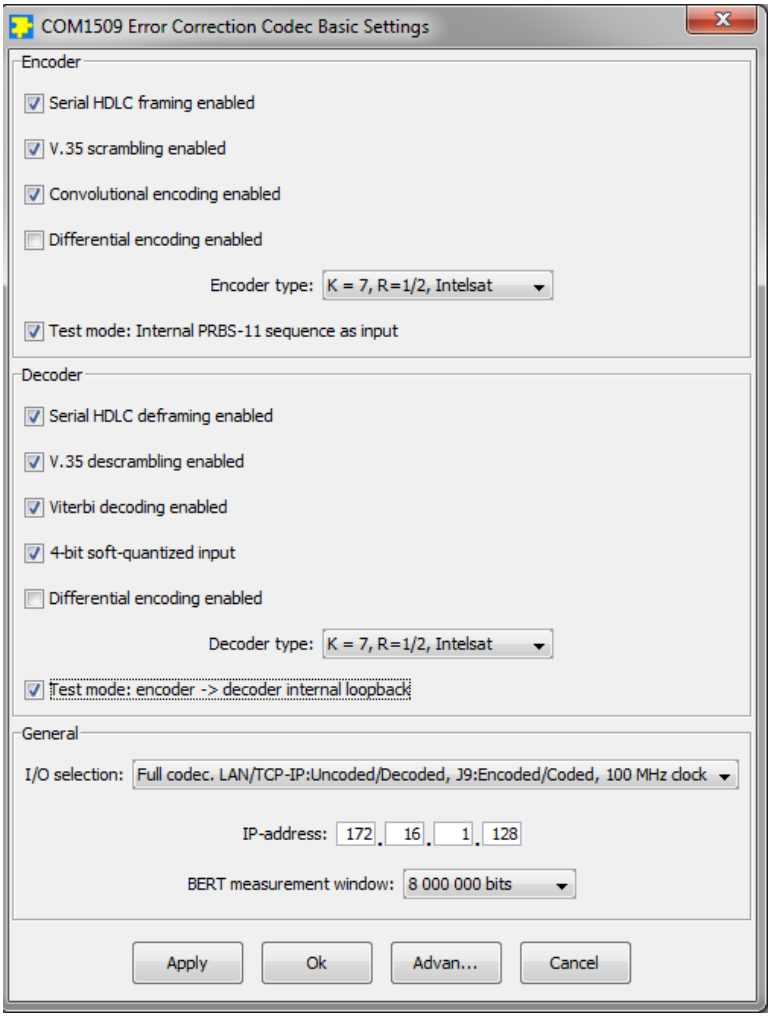
or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9/LVTTL)
- PC Card (CardBus).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1509 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1509 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

COM-1509 module I/O configuration	
Parameters	**Configuration**
I/Os	0 = decoder-only. **C**oded input samples through left J6 connector (synchronous serial). **D**ecoded output samples through right J9 connector. (synchronous serial, 40 MHz clock). COM-1009 replacement. 1 = decoder-only. **C**oded input samples through left J6 connector (synchronous serial). **D**ecoded output samples through right J9 connector. (synchronous serial, 120 MHz clock[1]). 2 = decoder-only. **C**oded input samples through left J6 connector (synchronous serial). **D**ecoded output samples through USB. 8 = encoder-only. **U**ncoded input samples through through left J6 connector (synchronous serial). **E**ncoded output samples through right J9 connector. (synchronous serial, 40 MHz clock). COM-1010 replacement. 9 = encoder-only. **U**ncoded input samples through through left J6 connector (synchronous serial). **E**ncoded output samples through right J9 connector. (synchronous serial, 120 MHz clock output[1]) 10 = encoder-only. **U**ncoded input samples through through left J6 connector (synchronous serial). Encoded output samples through USB. 16 = full codec. **U**ncoded input and **D**ecoded output through left J6 connector (synchronous serial) **E**ncoded output and **C**oded input through right J9 connector. 40 MHz clock output. 17 = full codec. **U**ncoded input and **D**ecoded output through left J6 connector (synchronous serial) **E**ncoded output and **C**oded input through right J9 connector. 120 MHz clock output[1]. 18 = full codec. Same as 16, with tx/rx pins flipped in J9 connector. 19 = full codec. Same as 17, with tx/rx pins flipped in J9 connector. 24 = full codec. **U**ncoded input and **D**ecoded output through USB **E**ncoded output and **C**oded input through right J9 connector (synchronous serial, 120 MHz clock[1] output). 25 = full codec. **U**ncoded input and **D**ecoded output through USB **E**ncoded output and **C**oded input through right J9 connector (synchronous serial, 40 MHz clock output). 26 = full codec. Same as 24, with tx/rx pins flipped in J9 connector. 27 = full codec. Same as 25, with tx/rx pins flipped in J9 connector. 32 = full codec. **U**ncoded input and **D**ecoded output through LAN/TCP-IP, port 1024.

[1] 90 MHz output clock when K=9

	Encoded output and **C**oded input through right J9 connector (synchronous serial, 120 MHz clock output[1]). Requires LAN adapter (such as COM-5102). 33 = full codec. **U**ncoded input and **D**ecoded output through LAN/TCP-IP, port 1024. **E**ncoded output and **C**oded input through right J9 connector (synchronous serial, 40 MHz clock output). Requires LAN adapter (such as COM-5102). 34 = full codec. Same as 32, with tx/rx pins flipped in J9 connector. 35 = full codec. Same as 33, with tx/rx pins flipped in J9 connector. REG0(5:0)

Encoder	
Parameters	**Configuration**
Encoder input selection	0 = external input 1 = internally generated PRBS-11 test sequence (for end-to-end bit error rate measurements) REG0(7)
Serial HDLC framing enable	0 = bypassed 1 = enabled REG1(0)
V.35/Intelsat IESS 308 scrambling enable	0 = bypassed 1 = enabled REG2(0)
FEC convolutional encoding enable	1 = encoding enabled 0 = bypass REG3(0)
Convolutional encoding constraint length K and rate R	0000 = (K=5, R=1/7) Intelsat IESS-308/309 0001 = (K = 7, R=1/2, Intelsat) 0010 = (K = 7, R=2/3, Intelsat) 0011 = (K = 7, R=3/4, Intelsat) 0100 = (K = 7, R=5/6, Intelsat) 0101 = (K = 7, R=7/8, Intelsat) 0110 = (K = 9, R=1/3) 0111 = (K = 9, R=1/2) 1000 = (K = 9, R=2/3) DVB ETS 300 421 DVB ETS 300 744 1010 = (K = 7, R=1/2, DVB) 1011 = (K = 7, R=1/2, CCSDS) 1100 = (K = 7, R=2/3, CCSDS/DVB) 1101 = (K = 7, R=3/4, CCSDS/DVB) 1110 = (K = 7, R=5/6, CCSDS/DVB) 1111 = (K = 7, R=7/8, CCSDS/DVB) REG3(4:1)
Differential Encoding	Differential encoding is useful in removing phase ambiguities at the PSK demodulator, at the expense of doubling the bit error rate. When enabled, the differential decoding must be enabled at the receiving end. There is no need to use the differential encoding to remove phase ambiguities at the PSK demodulator when the Viterbi decoder and HDLC decoder are enabled. 0 = disabled 1 = enabled REG3(5)

Decoder	
Parameters	**Configuration**
Decoder input selection	0 = external input 1 = internal loopback for test purposes REG10(0)
Soft/Hard Decision Decoding	Determines whether 4 bits (soft decision) or 1 bit (hard decision) will be used to decode the data. 0 = 4-bit soft decision 1 = 1-bit hard decision (uses input signal DATA_C_IN(3) only). REG10(7)
Viterbi decoding enabled	1 = decoding enabled 0 = bypass decoder REG11(0)
Viterbi decoding constraint length K and rate R	Firmware options **–A** and **–B** only 0000 = (K=5, R=1/7) Firmware options **–C** and **–D** only 0001 = (K = 7, R=1/2, Intelsat) 0010 = (K = 7, R=2/3, Intelsat) 0011 = (K = 7, R=3/4, Intelsat) 0100 = (K = 7, R=5/6, Intelsat) 0101 = (K = 7, R=7/8, Intelsat) 1010 = (K = 7, R=1/2, DVB) 1011 = (K = 7, R=1/2, CCSDS) 1100 = (K = 7, R=2/3, CCSDS/DVB) 1101 = (K = 7, R=3/4, CCSDS/DVB) 1110 = (K = 7, R=5/6, CCSDS/DVB) 1111 = (K = 7, R=7/8, CCSDS/DVB) Firmware options **–E** and **–F** only 0110 = (K = 9, R=1/3) 0111 = (K = 9, R=1/2) 1000 = (K = 9, R=2/3)
	REG11(4:1)
Differential Decoding	0 = disabled 1 = enabled REG11(5)
Measurement window	Number of bits in the window where raw bit errors (bit errors on the encoded bit stream) are computed: Always 1,000 bits
V.35/Intelsat IESS 308 descrambling enable	0 = bypassed 1 = enabled REG13(0)
Serial HDLC deframing enable	0 = bypassed 1 = enabled REG14(0)
BER tester measurement window	Number of bits in the window where errors are counted: 000 = 8,000 001 = 80,000 010 = 800,000 011 = 8,000,000 100 = 80,000,000 101 = 800,000,000 110 = 8,000,000,000 REG15(2:0)
Network Interface	
Parameters	**Configuration**
IP address (when connected to Gbit Ethernet PHY like **COM-5102, COM-5104**)	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG21 (MSB) – REG24 (LSB)
Reserved	REG25 through 30 are reserved for the LAN MAC address. These registers are set at the time of manufacturing. Since the MAC address is unique, it can also be used as a unique identifier in a radio network with many nodes.

Monitoring

Status Registers

Status registers are read-only. Multi-byte status words are latched in together upon reading status register SREG8.

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-7 Properly operating hardware will result in the following sequence being displayed: SREG0/1/2/3/4/5/6/7 = 2C F1 95 xx 0F 01 00 24
FEC decoder synchronized	Synchronized SREG8(0)
FEC decoder input BER	Encoded stream bit errors detected by the FEC decoder over a 1000-bit window. This method can be used at all time, irrespective of the transmitted sequence. SREG9 = bits 7 – 0 (LSB) SREG10 = bits 15 – 8 SREG11 = bits 23 – 16
BER tester synchronized	Synchronized SREG12(0)
BER	End-to-end bit error rate, including all enabled functions (FEC codec, V.35 scrambling/descrambling, HDLC framing). This method requires transmission of a PRBS-11 test sequence (as enabled through control register REG0(7)) The BER is measured over a 8Mbit window. The measurement is only valid when the BER tester is synchronized with the expected PRBS-11 test sequence. SREG13 = bits 7 – 0 (LSB) SREG14 = bits 15 – 8 SREG15 = bits 23 – 16 SREG16 = bits 31 – 24 (MSB)
Cumulative number of valid bits at HDLC output	SREG17: LSB SREG18: SREG19: SREG20: MSB
LAN TCP connection	'1' when a remote client is connected. Bit 0: client connected to port 1028 for monitoring and control Bit1: client connected to port 1024 for high-speed data transfer. SREG23(1:0)
LAN PHY ID	Read the LAN adapter Ethernet PHY ID as a hardware check. Returns 0x22 when using a COM-5102 adapter. SREG24
Ethernet MAC address	Unique 48-bit hardware address (802.3). In the form SREG25:SREG26…:SREG30

Digital Test Points

Test points are provided on the J9 right connector top side

Test Point	Definition
TP31	Solid '1' when the Viterbi decoder is synchronized. Toggling otherwise.
TP32	Detected bit error in the Coded bit stream
TP33	Re-synchronization attempt. Each time the Viterbi decoder attempts to re-synchronize, it generates this pulse.
TP34	Serial HDLC decoder out of sync (pulses)
TP35	BER tester matched filter output (detects periodic start of PRBS-11 sequence every 2047 bits)
TP36	Solid '1' when BER tester is synchronized
TP37	BER tester detected bit error
DONE	'1' indicates proper FPGA configuration.

Implementation

K = 5

The generator polynomials for K = 5 R = 1/7 is

$G_0(x) = 1 + x + x^2 + x^4$

$G_1(x) = 1 + x^2 + x^3 + x^4$

$G_2(x) = 1 + x^2 + x^4$

$G_3(x) = 1 + x^2 + x^3 + x^4$

$G_4(x) = 1 + x + x^3 + x^4$

$G_5(x) = 1 + x + x^2 + x^4$

$G_6(x) = 1 + x + x^2 + x^3 + x^4$

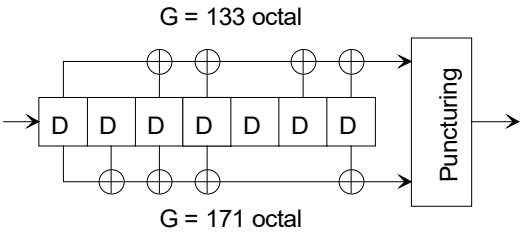
K = 7 (Intelsat)

The generator polynomials for K = 7 R = ½ are

$G_0(x) = 1 + x^2 + x^3 + x^5 + x^6$ 133(octal)

$G_1(x) = 1 + x + x^2 + x^3 + x^6$ 171(octal)

The implementation is depicted below:



Rates other than ½ are implemented by puncturing the rate ½ encoded data stream. The puncturing pattern is as follows (1 denotes transmission, 0 blocking)

Rate 2/3	G_0	11
	G_1	10
Rate 3/4	G_0	110
	G_1	101
Rate 5/6	G_0	11010
	G_1	10101
Rate 7/8	G_0	1111010
	G_1	1000101

K = 7 (DVB)

Similar to Intelsat, but G0/G1 are reversed.

$G_0(x) = 1 + x + x^2 + x^3 + x^6$ 171(octal)

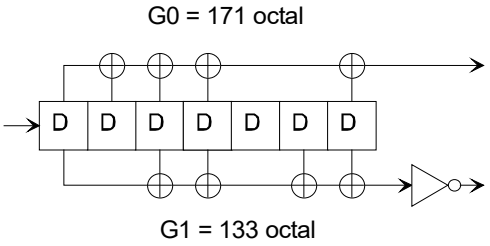
$G_1(x) = 1 + x^2 + x^3 + x^5 + x^6$ 133(octal)

Rates other than ½ are implemented by puncturing the rate ½ encoded data stream. The puncturing pattern is as follows (1 denotes transmission, 0 blocking)

Rate 2/3	G_0	10
	G_1	11
Rate 3/4	G_0	101
	G_1	110
Rate 5/6	G_0	10101
	G_1	11010
Rate 7/8	G_0	1000101
	G_1	1111010

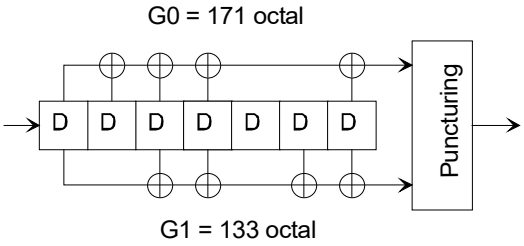
K = 7 (CCSDS)

Similar to Intelsat, but G0/G1 are reversed and the G1 output is inverted for non-punctured rate R = ½ as illustrated below:



Basic CCSDS convolutional encoder (no puncturing)

The basic encoder inverts the G_1 output. When using puncturing, this inverter is removed.



CCSDS convolutional encoder with puncturing

Rates other than ½ are implemented by puncturing the rate ½ encoded data stream. The puncturing pattern is as follows (1 denotes transmission, 0 blocking)

Rate 2/3	G_0	10
	G_1	11
Rate 3/4	G_0	101
	G_1	110
Rate 5/6	G_0	10101
	G_1	11010
Rate 7/8	G_0	1000101
	G_1	1111010

K = 9

The generator polynomials for K = 9 R = 1/3 is

$G_0(x) = 1 + x^2 + x^3 + x^5 + x^6 + x^7 + x^8$

$G_1(x) = 1 + x + x^3 + x^4 + x^7 + x^8$

$G_2(x) = 1 + x + x^2 + x^5 + x^8$

The generator polynomials for K = 9 R = 2/3 is

$G_0(x) = 1 + x + x^2 + x^3 + x^5 + x^7 + x^8$

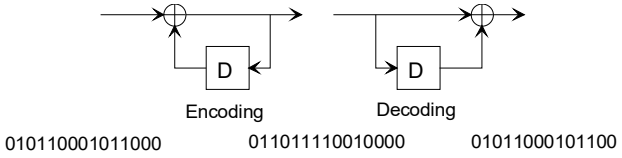
$G_1(x) = 1 + x^2 + x^3 + x^4 + x^8$

The rate 2/3 decoder is configured for a rate ½ encoded data stream with the following puncturing pattern (1 denotes transmission, 0 blocking):

Rate 2/3	G_0	11
	G_1	01

Differential Decoding

Differential decoding can be used following FEC decoding as specified in Intelsat IESS-308/309. This feature can be enabled/disabled by software.



This mode compensates for any bit inversion occurring in the transmission channel (for example at a BPSK demodulator which cannot resolve the inherent 180deg phase ambiguity).

Self Synchronization

This Viterbi decoder implementation is self-synchronizing. The synchronization algorithm is described below.

The nature of the Viterbi algorithm requires that the input data bits occur in a certain order.

Example: For every giving input bit (B_{In}) the Rate 1/3 generator polynomials will give three output bits (B_{Out0}, B_{Out1}, B_{Out2}). For the Viterbi algorithm to decode properly, the bits must be received in the order B_{Out0}, B_{Out1}, B_{Out2}.

In addition, the decoder expects to *start* decoding at a certain position. This is determined by the first input bit. In the previous example, the Viterbi expects the first input bit to be B_{Out0}, followed by B_{Out1} and B_{Out2}. Generally in block mode this is always the case.

However, due to startup conditions, this not guaranteed in continuous mode. In the case of the example, the first input bit may be B_{Out2}, followed by B_{Out0} and B_{Out1} (Note the order is still maintained). Since the Viterbi expects the first input bit to be B_{Out0}, it will decode this received input series of

B_{Out2}, B_{Out0}, B_{Out1}

As

B_{Out0}, B_{Out1}, B_{Out2}

Thus, the decoded output will be incorrect, and the decoder is considered to be unsynchronized.

When the decoder detects that the bit error is greater than a pre-determined threshold, it attempts to re-synchronize.

The lock status signal will equal ‘0’ and the decoder will shift the input bit’s position.

For example, in the received input sequence,

B_{Out2}, B_{Out0}, B_{Out1}

The decoder will bypass the first bit and start instead at:

Bypassed B_{Out0}, B_{Out1},

The decoder will continue to shift until it is synchronized.

Encoded Bit Error Rate Measurement

The decoder estimates the bit error rate on the encoded bit stream by comparing the actual received bit stream with an estimate of the transmitted bit stream. This estimate is generated by re-encoding the nearly error-free decoded bit stream.

The algorithm is based on the proposition that the decoded bit stream is nearly error-free. If the decoded bit stream were error-free, then the re-encoded bit stream would be the actual transmitted encoded bit stream before bit errors occur in the transmission channel.

The encoded bit error rate is computed over a window of 1000-encoded bits. Synchronization is declared when the BER is below the following preset thresholds:

32% for rate 1/2

16% for rate 2/3

11.5% for rate 3/4

8% for rate 5/6

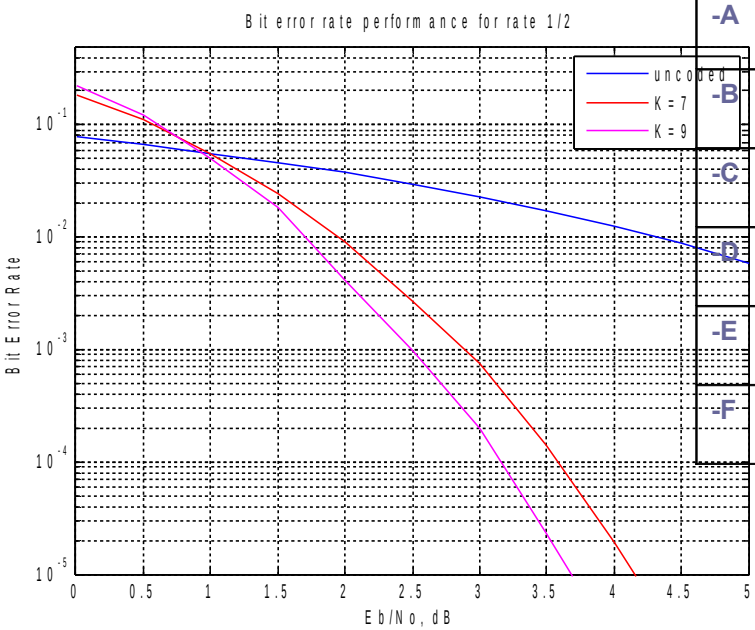
6.2%for rate 7/8

Eb/No Threshold

The Viterbi decoder is capable of operating (i.e. self-synchronizing, staying locked, no false out-of-sync condition) above the following Eb/No thresholds:

K, R	Eb/No threshold
K=7,9, R=1/2	0 dB
K=7, R=2/3	1 dB
K=7, R=3/4	1.4 dB
K=7, R=5/6	2.2 dB
K=7, R=7/8	3 dB

BER Performance



BER performance for rate 1/2

Options

Due to FPGA size limitations, the codec multiple functional modes are distributed over four different firmware options. The four firmware versions can be downloaded from www.comblock.com/download.

Changing the functionality requires loading the firmware once using the ComBlock control center, then switching between the stored firmware versions The selected firmware option is automatically reloaded at power up or upon software command within 1.2 seconds

Option	Definition
-A	K=5 FEC Synchronous serial interface or USB
-B	K=5 FEC USB or LAN/TCP-IP (with COM-5102)
-C	K=7 FEC Synchronous serial interface or USB
-D	K=7 FEC USB or LAN/TCP-IP (with COM-5102)
-E	K=9 FEC Synchronous serial interface or USB
-F	K=9 FEC USB or LAN/TCP-IP (with COM-5102)

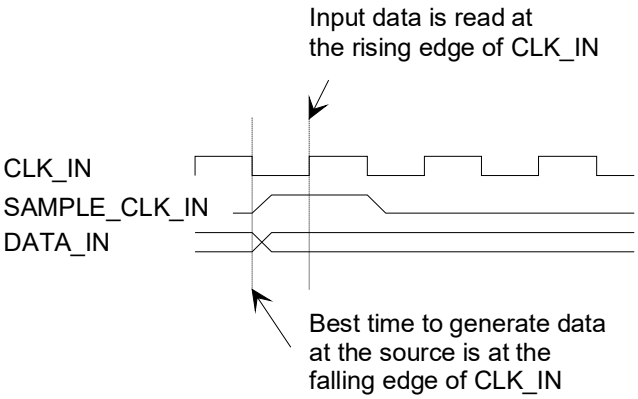
Timing

This module operates at an internal clock rate $\mathbf{f_{clk}}$ of 120 MHz[1]. Inputs use indepent clocks CLK_U_IN and CLK_C_IN at frequencies up to 120 MHz[1].

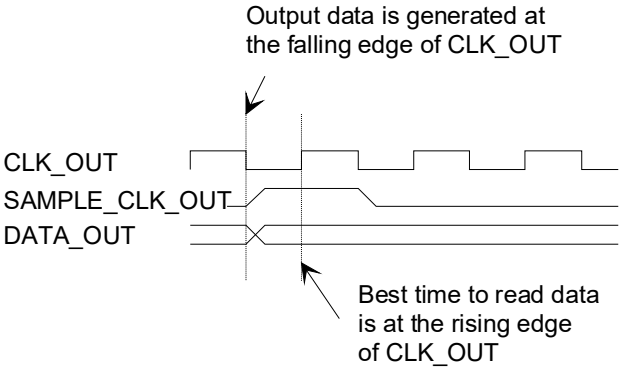
For backwards compatibility with older ComBlocks, outputs with 40 MHz IO clocks are also supported.

The I/O signals are synchronous with the rising edge of CLK_IN (i.e. all signals transitions always occur after the rising edge of the reference clock CLK_IN).

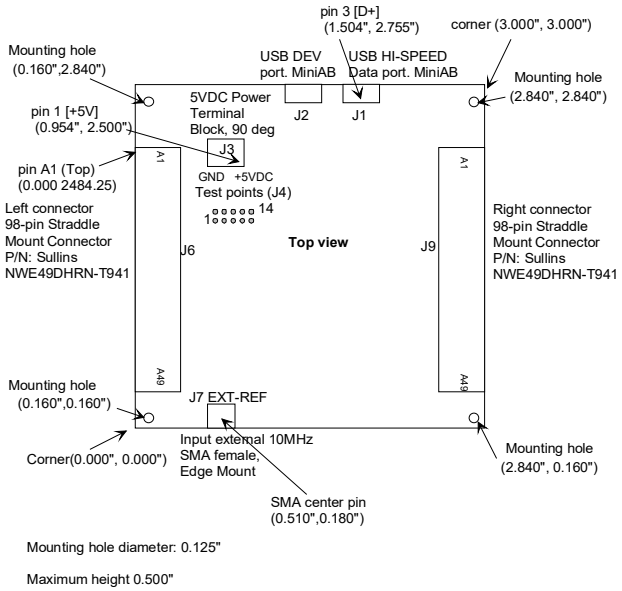
LVTTL Synchronous Serial Input



LVTTL Synchronous Serial Output



Mechanical Interface



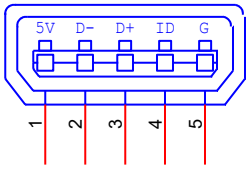
Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1500schematics.pdf

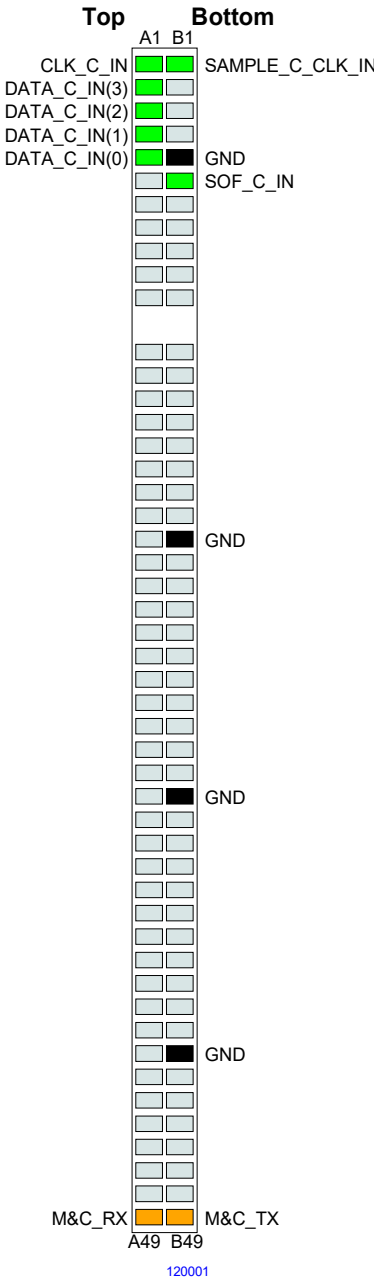
Pinout

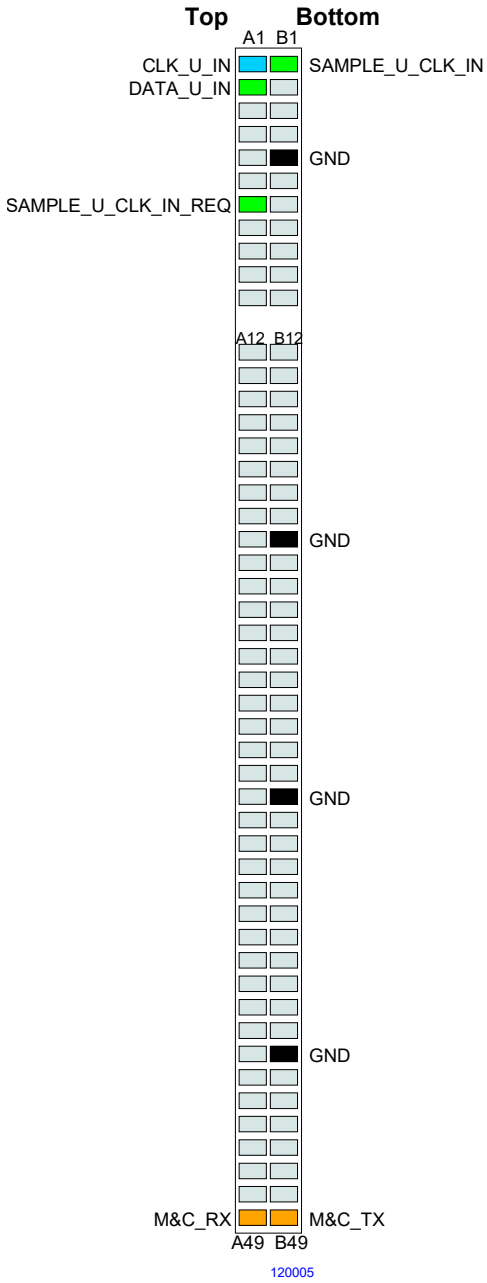
USB

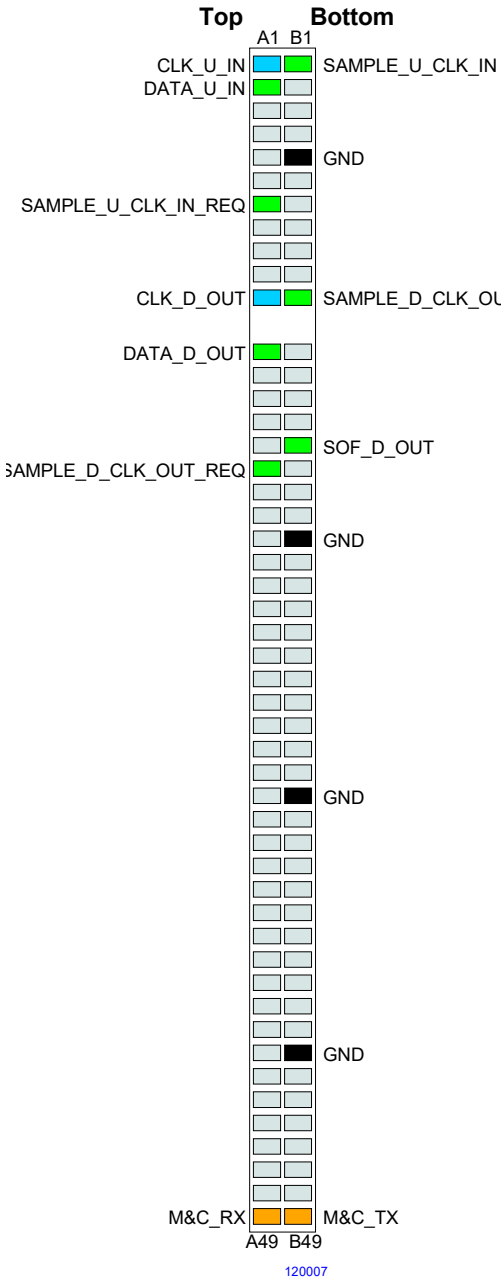
The USB port labeled HIGH-SPEED is equipped with a mini type AB connector. (G = GND). The COM-1509 acts as a USB device.



Left Connector J6







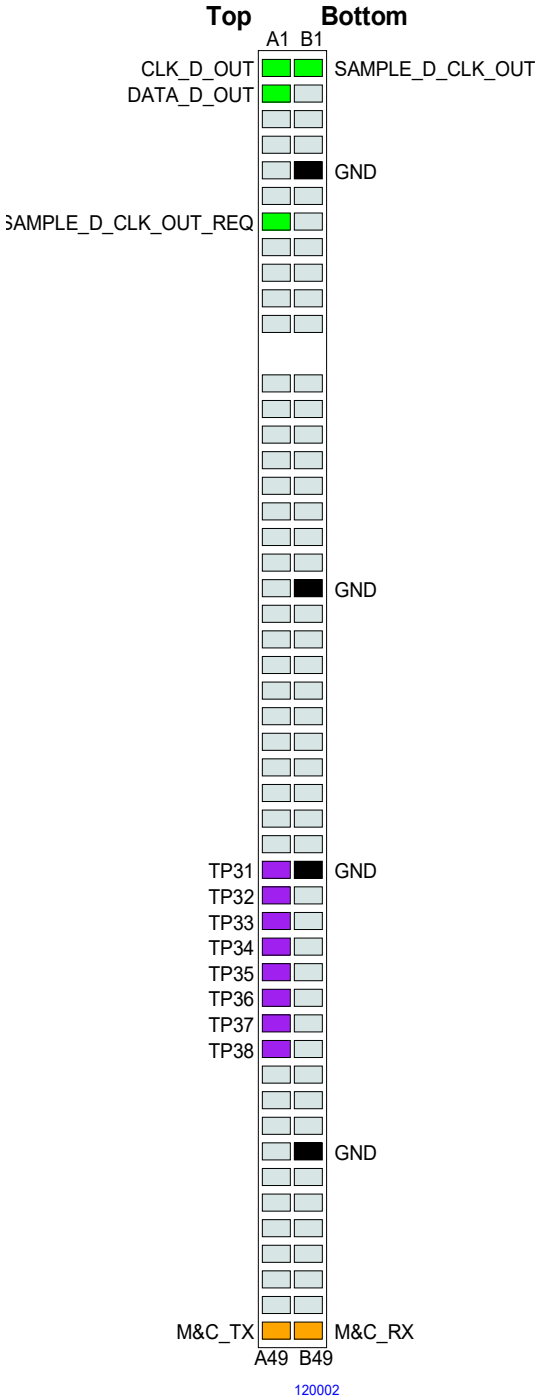
Decoder-only
REG0(5:0) = 0,1 or 2

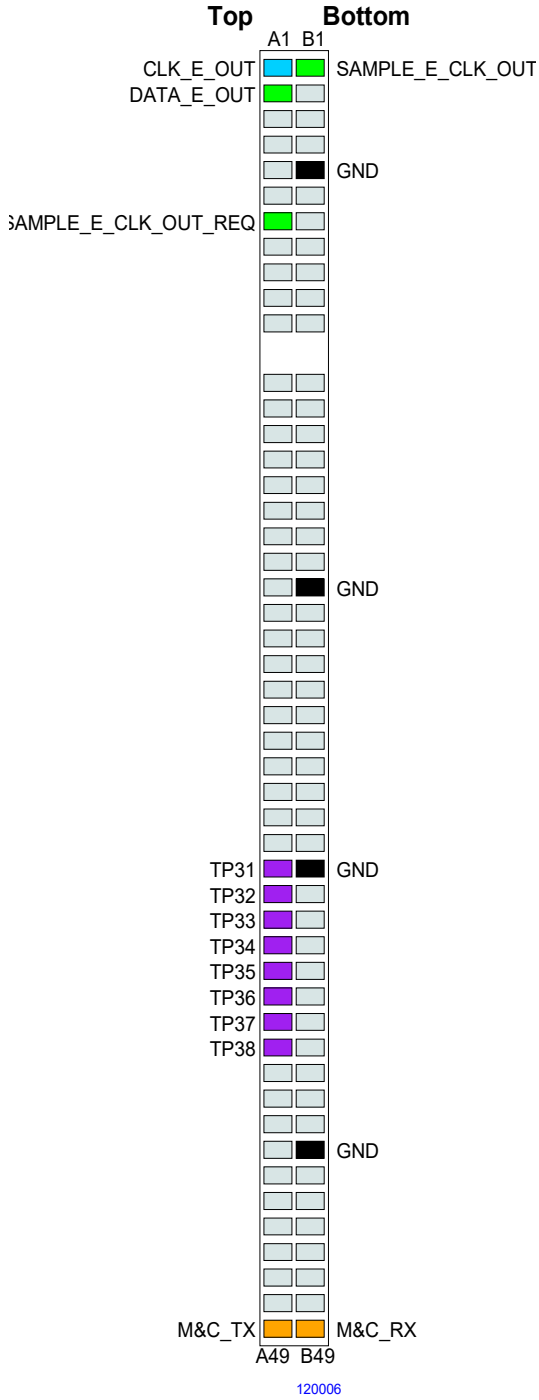
Encoder-only
REG0(5:0) = 8,9 or 10

Full codec
REG0(5:0) = 16,17,18 or 19

98-pin to 40-pin adapters to interface with other Comblocks are supplied free of charge. Please let us know about your interface requirements at the time of order.

Right Connector J9

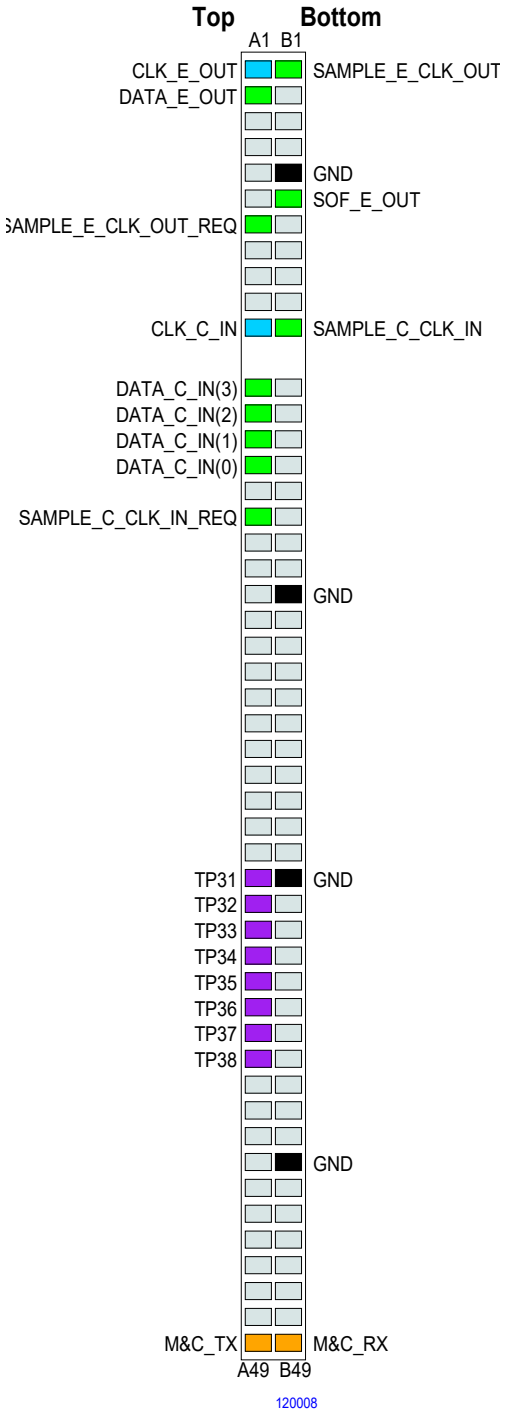




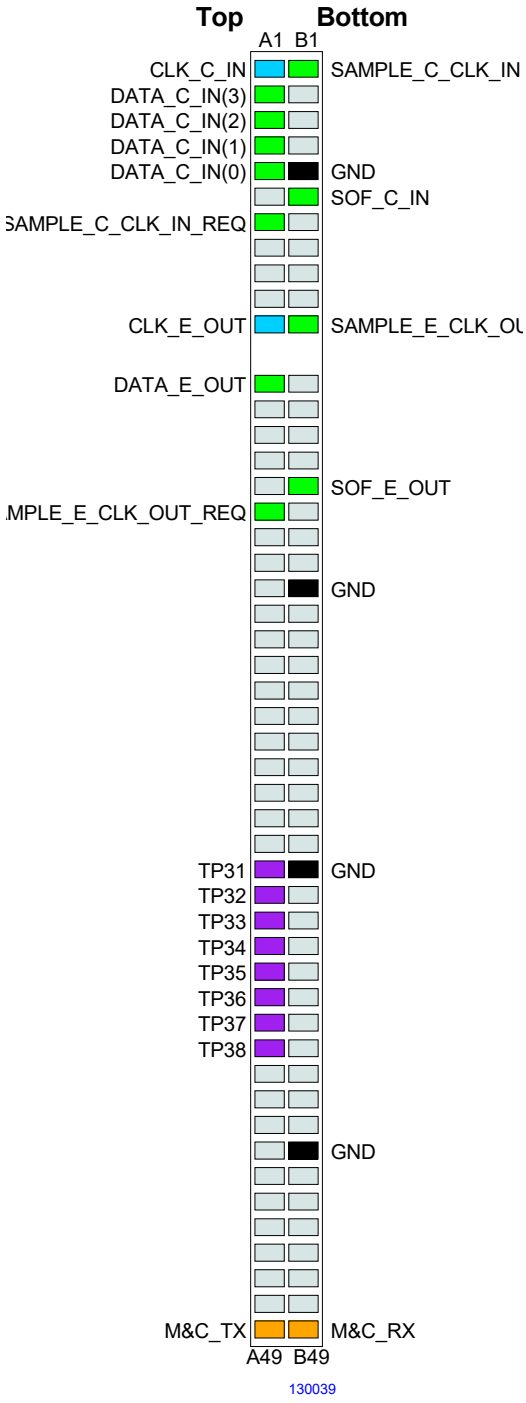
Decoder-only
REG0(5:0) = 0 or 1

Encoder-only
REG0(5:0) = 8,9 or 10

98-pin to 40-pin adapters to interface with other Comblocks are supplied free of charge. Please let us know about your interface requirements at the time of order.



Full codec
REG0(5:0) = 16,17,24,25,32 or 33



Full codec (flipped tx/rx)
REG0(5:0) = 18,19,26,27,34,35

I/O Compatibility List

(not an exhaustive list)

Encoded side
COM-1202 PSK/QAM/APSK modem
COM-1519 DSSS Modulator
COM-1028 FSK/MSK/GFSK/GMSK Modulator
Coded side
COM-1202 PSK/QAM/APSK modem
COM-1518 DSSS Demodulator
COM-1027 FSK/MSK/GFSK/GMSK demodulator
Baseband side
COM-5102 Gigabit Ethernet + HDMI interface (for Ethernet use only)
COM-1500 FPGA + ARM development platforms

Configuration Management

This specification is to be used in conjunction with VHDL software revision 3.

ComBlock Ordering Information

COM-1509 Error correction codec

ECCN 5A991

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