COM-1503 FSK/MSK/GMSK Burst Modem, 15 Msymbols/s

Key Features

- Support for FSK, MSK and GMSK modulations
  - Programmable symbol rate up to 15 Msymbols/s
  - Multi-node network configuration: one master unit, several slave units.
  - Full duplex or half-duplex
  - Configurable as continuous mode, random access burst mode, or time-division multiple access (TDMA)
  - Modulator and demodulator are independently configured.
- Low-overhead error correction: long BCH code (16008,16200,12) corrects 12 bit errors in a 16Kbit frame.
- Demodulator inputs: Digital (12-bit real or complex, up to 120Msamples/s). Sampling clock is controlled by this board.
- Modulator outputs: Digital 1-bit or 16-bit up to 240 Msamples/s
- Modem data I/Os:
  - Two synchronous serial interfaces
  - USB 2.0.
  - LAN/TCP (with optional COM-5401/COM-5102)
- Extensive test & monitoring:
  - BER measurement when transmitting PRBS-11 test sequence or frame sync.
  - PRBS-11 test sequence generator
  - Loopback mode
- Input for an external, higher-stability 10 MHz frequency reference.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.

COM-1503

For the latest data sheet, please refer to the **ComBlock** web site: comblock.com/download/com1503.html.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to comblock.com/product_list.html .

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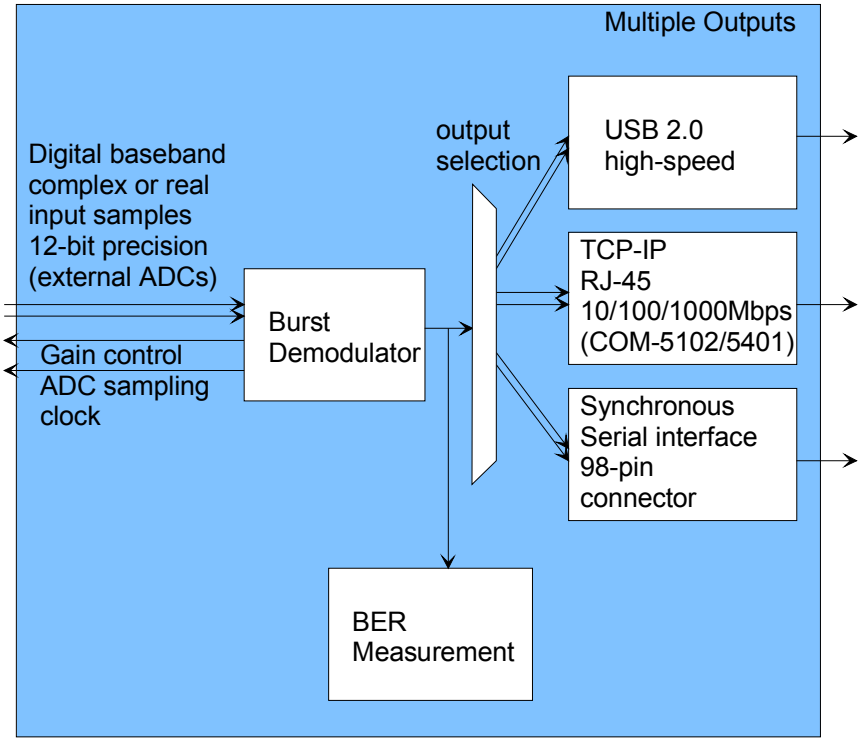
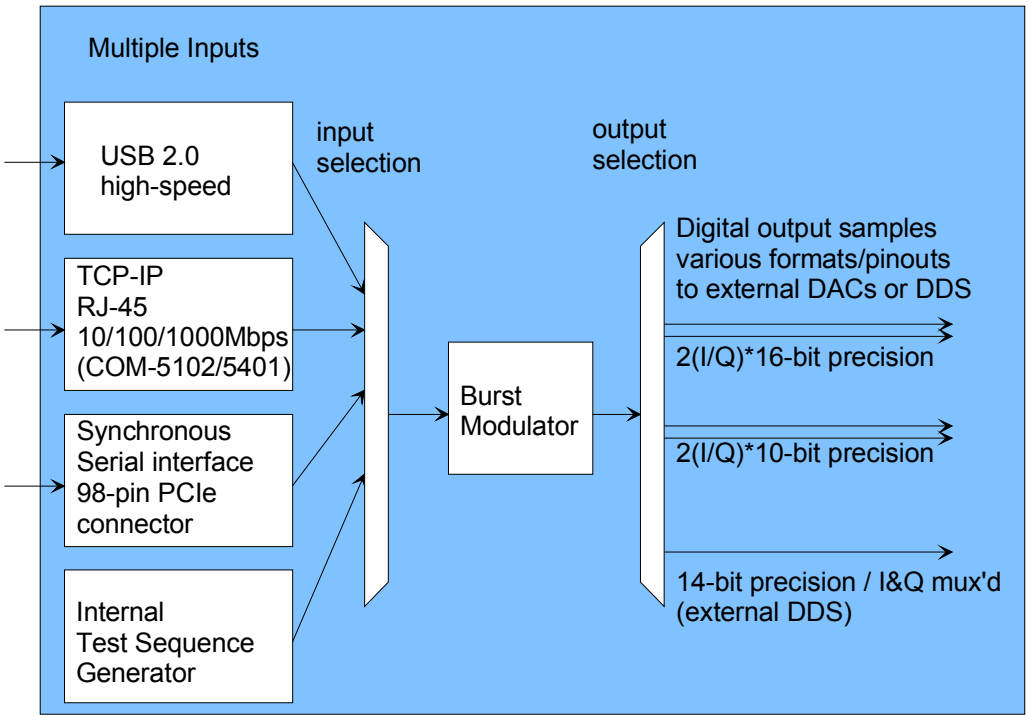
Overall Block Diagrams

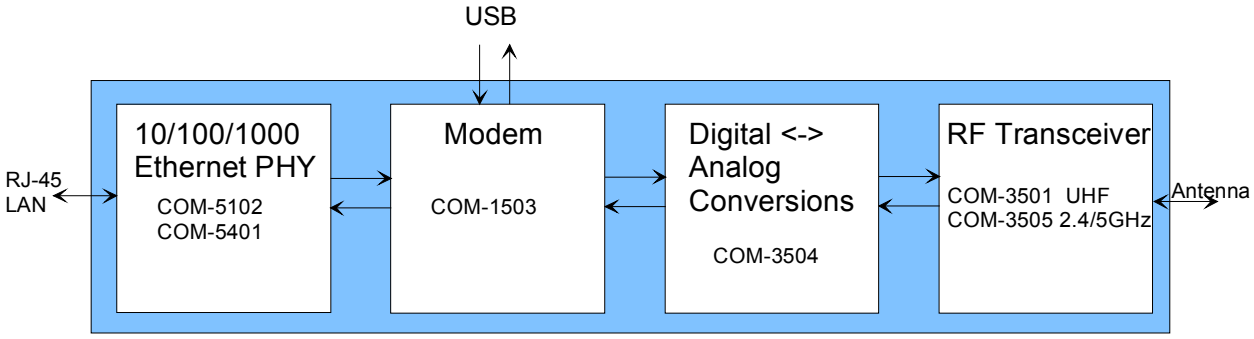


Demodulator connectivity

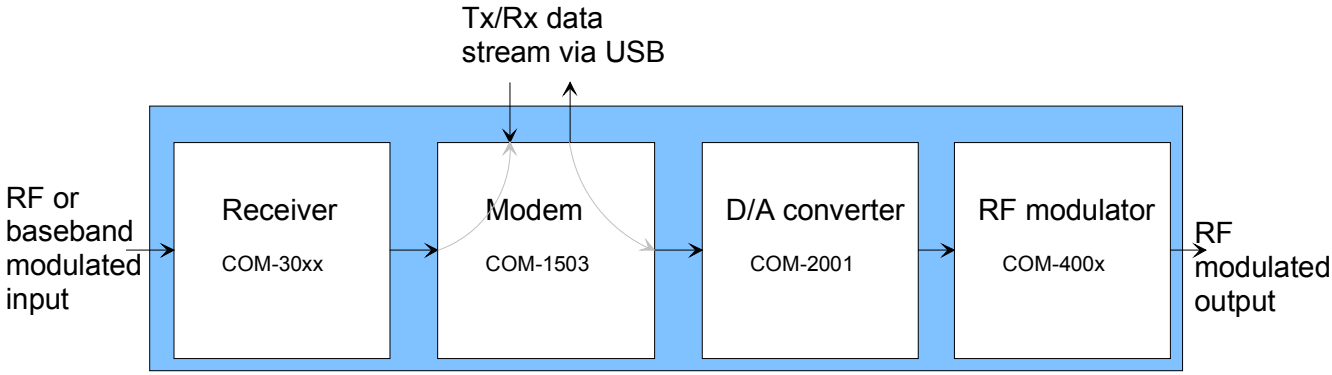


Modulator connectivity

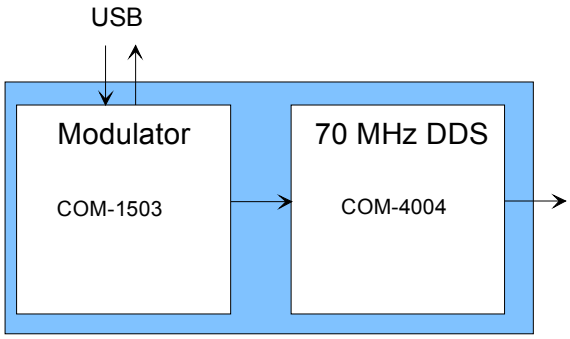
Use example #1 Half-Duplex modem



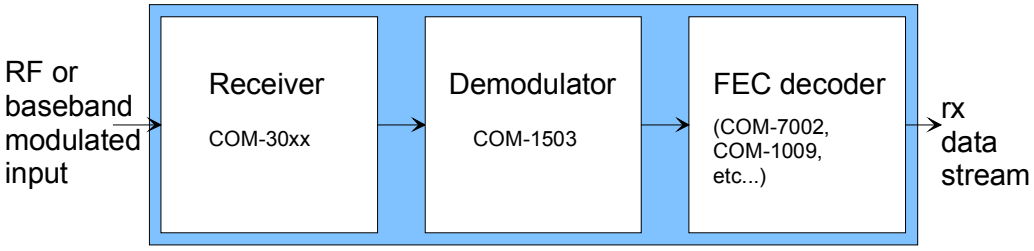
Use example #2 Full-Duplex modem



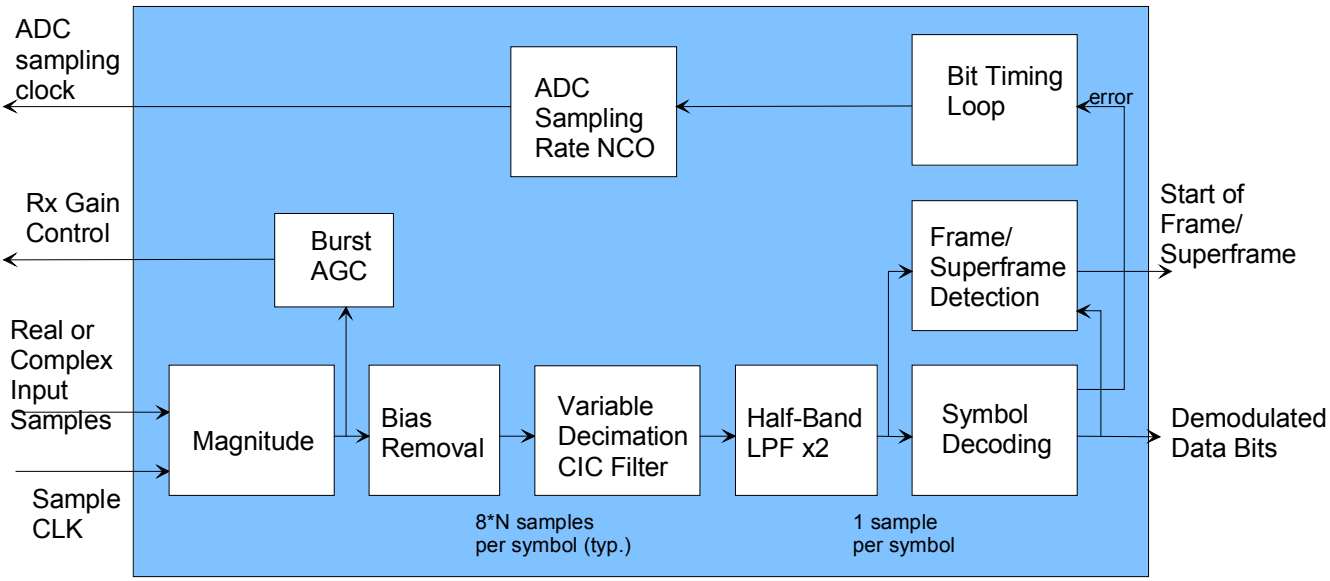
Use example #3 70 MHz IF Burst Modulator



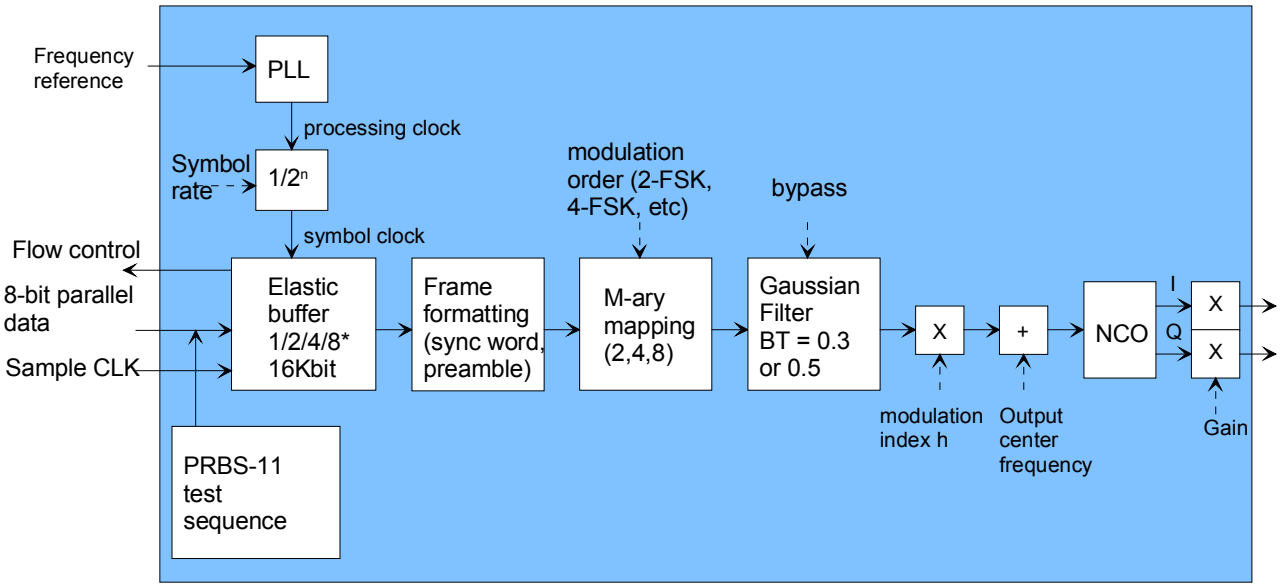
Use example #4 Demodulator-only



Block Diagram (FSK/MSK/GFSK Digital Demodulator)



Block Diagram (FSK/MSK/GFSK Digital Modulator)



Electrical Interface

Other Digital Modem Interfaces	Definition
USB 2.0	Type B receptacle. This interface supports two virtual channels: one for monitoring and control, the other to convey information data between the modem and a host computer.
LAN / TCP-IP	Networking requires an additional 10/100/1000 Mbps Ethernet adapter (COM-5102 or COM-5401) plugged in the left (J6) connector. The COM-1503 includes a TCP-IP server, awaiting a remote client connection at port 1024.

Power Interface	4.75 – 5.5VDC. Terminal block. Power consumption is approximately proportional to the symbol clock rate ($f_{symbol\ clk}$). The

	maximum power consumption is TBDmA.

Nominal Operation

Supply voltage	+4.75 to +5.25 VDC

Absolute Maximum Ratings

Supply voltage	-16V min, +16V max
98-pin connector inputs	-0.5V min, +3.6V max

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB
- Asynchronous serial (LVTTL)

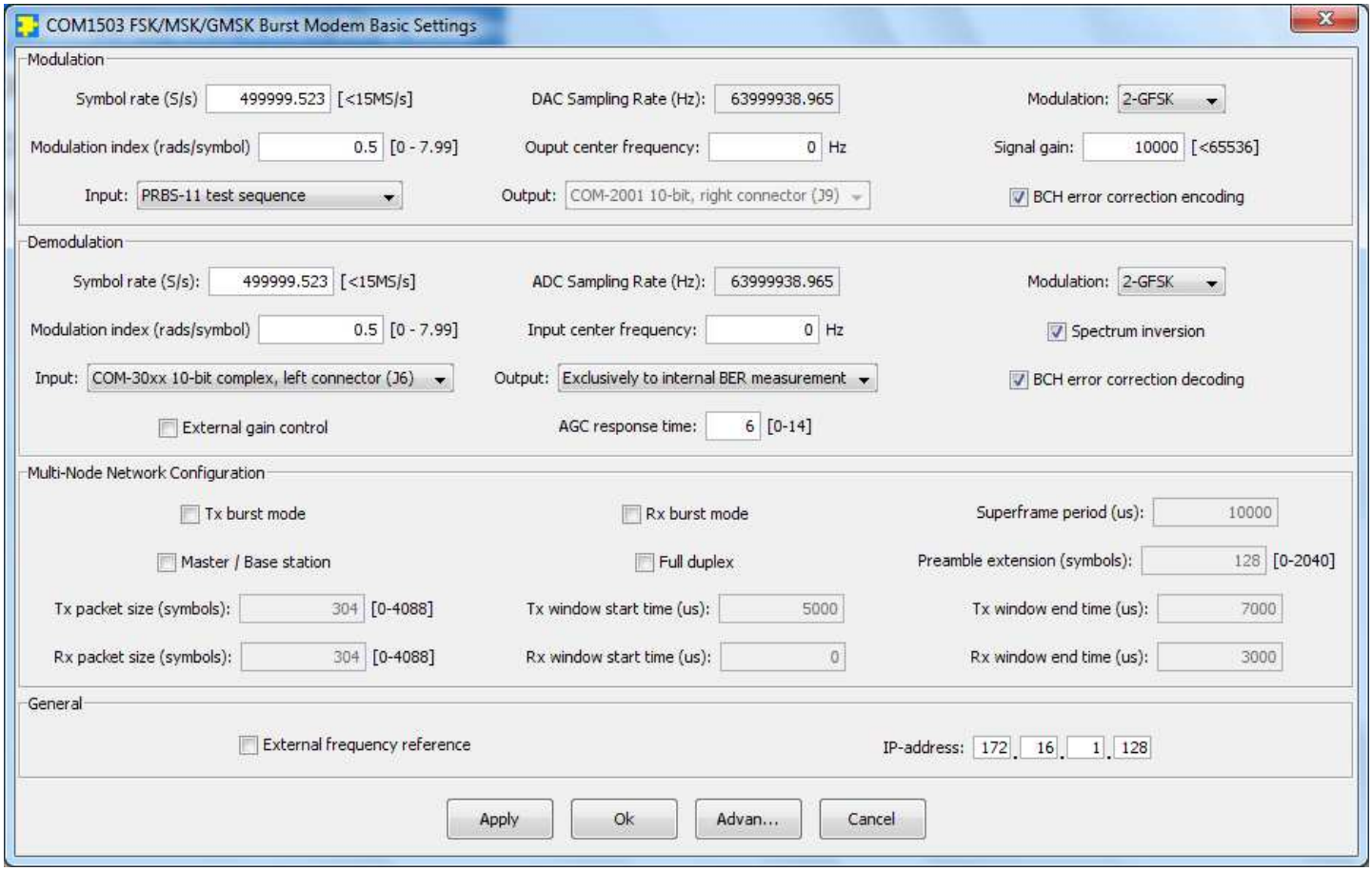
or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9/LVTTL)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1503 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1503 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Modulator	
Parameters	**Configuration**
Processing clock f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock after frequency doubling. 20-bit unsigned integer expressed as $f_{clk\_tx} * 2^{20}$ / 360MHz. 120 MHz maximum. 20 MHz recommended minimum REG0 = bits 7-0 (LSB) REG1 = bits 15 – 8 (MSB) REG2(3:0) = bits 19 – 16 (MSB)
Internal/External frequency reference	0 = internal. Use the internal 60 MHz clock (from the USB PHY) as frequency reference. 1 = external. Use the 10 MHz clock externally supplied through J7 as frequency reference. REG2(7)
Symbol rate $f_{symbol\ rate\ tx}$	The modulator symbol rate is in the form $f_{symbol\ rate\ tx} = f_{clk\_tx} / 2^n$ where n ranges from 0 (1 sample per symbol) to 15 (symbol rate = f_{clk_tx} / 32768). n is defined in REG3(3:0)
Modulation Index h	Modulation index h. Format 3.8 Thus, 0x0080 represents an index of 0.5. (MSK). Valid range: 0 – 7.996 REG4(7:0): LSB, after decimal point REG6(7:5): MSB, before decimal point
Modulation type	0 = 2-FSK 1 = 2-GFSK 2 = 4-FSK 3 = 4-GMSK 4 = 8-FSK 5 = 8-GMSK REG5(5:0)
Continuous vs burst modulation	0 = burst mode 1 = continuous mode While in continuous mode, the following configuration parameters are ignored: packet size, window start and stop times. REG5(6)
Gaussian Filter BT	0 = BT 0.3 1 = BT 0.5 REG5(7)
Output Center frequency (f_{c_tx})	Frequency translation. 32-bit signed integer (2's complement representation) expressed as $f_{c\_tx} * 2^{32} / f_{clk\_tx}$ For a clean output waveform, we recommend keeping the maximum frequency (center frequency + ½ symbol rate) below 1/10th of the processing clock f_{clk_tx}. REG57: LSB REG58 REG59 REG60: MSB
Input selection / format, test modes	Select the origin of the modulator input data stream. 0 = high-speed USB, 8-bit parallel 1 = LAN/TCP-IP, port 1024 (through Ethernet adapter), 8-bit parallel 2 = from left J6 connector (Many comblocks), 1-bit serial 3 = internal generation of 2047-bit periodic pseudo-random bit sequence (with BCH encoding when enabled) 4 = internal generation of modulo-256 counting test sequence. (with BCH encoding only)

	5 = internal generation of null test sequence. 8-bit parallel input bytes are transmitted MSb first. Test sequences override external input bit stream. REG6(3:0)
BCH encoder bypass	'0' = BCH encoder enabled '1' = BCH encoder bypassed REG6(4)
Signal gain	Signal level. 16-bit unsigned integer. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend checking for saturation at the D/A converter when changing either the symbol rate or the signal gain. REG7 = bits 7-0 (LSB) REG8= bits 15-8 (MSB)
Transmit packet size N_{pltx}	Transmit packet size expressed in number of payload symbols N_{pltx}. Must be an integer of 8. REG10: LSB REG11(3:0): MSb
Transmission window start time	Start time of the window during which the modulator is allowed to initiate a frame transmission. In µs after the start of superframe. Always zero for master unit. REG12: LSB REG13 REG14: MSB
Transmission window end time	End time of the window during which the modulator is allowed to initiate a frame transmission. A frame transmission in progress can extend beyond the end of the transmission window. In us after the start of superframe. REG15: LSB REG16 REG17: MSB
Preamble extension	Prepend a dummy preamble to the packet to give the receiver AGC time to converge before the sync field. Expressed as number of symbols/8.

	Valid range 0 – 255 (representing 0 to 2040 symbol preamble). Adjust as a function of the receiver AGC response time. REG18
Output selection	The output selection is based on the firmware option (i.e. personality) loaded in the FPGA. The modulator output can be directed to one of several possible interfaces: **(-A)** Digital 16-bit precision unsigned, right (J9) connector, compatible with COM-3504 **(-B)** Digital 10-bit precision unsigned, right (J9) connector, compatible with COM-2001 **(-C)** Digital 14-bit precision unsigned, right (J9) connector, compatible with COM-4004 A digital 1-bit precision output is always present on left connector pin B36 (valid only for OOK modulation). Click on the swiss army knife button to select the proper firmware option.
Multi-Node Network Configuration	
Mode	0 = Slave / remote unit 1 = Master / base station (one per network) REG11(7)
Half/Full Duplex	0 = Half-duplex. Tx/Rx are mutually exclusive 1 = Full duplex. Tx/Rx can occur simultaneously REG11(6)
Superframe period	Periodic superframe duration, in us. REG20: LSB REG21 REG22: MSB
Demodulator	
Parameters	**Configuration**
Processing clock f_{clk_rx}	Demodulator processing nominal frequency. The demodulator processing clock also serves as ADC sampling clock.

	The demodulator corrects the processing clock (ADC sampling clock) frequency around its nominal value so as to track small changes in the received signal symbol rate. 20-bit unsigned integer expressed as $f_{clk\_rx} * 2^{20} / 360MHz$. 120 MHz maximum. 20 MHz recommended minimum REG25 = bits 7-0 (LSB) REG26 = bits 15 – 8 (MSB) REG27(3:0) = bits 19 – 16 (MSB)
Nominal symbol rate $f_{symbol\ rate\ rx}$	The demodulator nominal symbol rate is in the form $f_{symbol\ rate\ rx} = f_{clk\_rx} / 2^n$ where n ranges from 0 (1 sample per symbol) to 15 (symbol rate = f_{clk_rx} / 32768). n is defined in REG28(3:0)
Inverse Modulation Index **1/h**	1/(Modulation index **h**). Format 8.8 Thus, 0x0200 represents the inverse of a modulation index of 0.5. (MSK or GMSK modulation imply h = 0.5). Valid range for **1/h**: 0.125 – 4 REG51: LSB REG52: MSB
Modulation type	0 = 2-FSK 1 = 2-GFSK 2 = 4-FSK 3 = 4-GMSK 4 = 8-FSK 5 = 8-GMSK REG30(5:0)
Continuous vs burst mode	0 = burst mode 1 = continuous mode While in continuous mode, the following configuration parameters are ignored: packet size, window start and stop times. REG30(6)
Spectrum inversion	Whenever the received spectrum has been inverted during the frequency up and down-conversions, this bit should be set. In particular, spectrum inversion occurs in most COM-300x receiver modules. 0 = off, 1 = on REG11(5)

Nominal Center frequency (f_{c_rx})	Expected center frequency of the received signal. 32-bit signed integer (2's complement representation) expressed as $f_{c\_rx} * 2^{32} / f_{clk\_rx}$ Maximum recommended range: ± 10 MHz. REG53: LSB, REG54, REG55, REG56: MSB
BCH decoder bypass	'0' = BCH decoder enabled '1' = BCH decoder bypassed REG32(4)
Receive packet size N_{plrx}	Receive burst size expressed in number of payload symbols N_{plrx}. Must be an integer of 8. REG31: LSB REG32(3:0): MSb
Reception window start time	Start time of the window during which the demodulator is allowed to start receiving a frame. In us after the first frame preamble in a received superframe. REG33: LSB REG34 REG35: MSB
Reception window end time	End time of the window during which the demodulator is allowed to start receiving a frame. A frame reception in progress can extend beyond the end of this window. In us after the first frame preamble in a received superframe. REG36: LSB REG37 REG38: MSB
Input selection	0 = digital real 12-bit unsigned samples, right connector, COM-3504. 1 = digital complex 2*12-bit unsigned samples, right connector, COM-3504. 2 = digital complex 2*10 or 2*12-bit unsigned samples, left connector. Compatible with most COM-30xx modules. 7 = internal loopback mode, from modulator. (not functional if the symbol rate is selected with one symbol per processing clock). REG39(2:0)

AGC1 response time	Users can to optimize AGC1 response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and symbol rate). The response time is approximately: 0 = 8 symbols, 1 = 16 symbols, 2 = 32 symbols, 3 = 64 symbols, etc…. 7 = every thousand symbols. Note: a x4 faster AGC is used during the burst preamble. Valid range 0 to 14. REG39(7:3)
Internal/external gain control	The gain actuation can be internal (0) or external (1) REG11(4)
Output selection	0 = USB 1 = TCP-IP (through COM-5102/5401 Ethernet interface) 2 = 1-bit serial raw demodulator output left (J6) connector. 3 = 1-bit serial raw demodulator output right (J9) connector. 4 = exclusively to internal BER measurement REG40(2:0)
IP address	4-byte IP address. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG41: MSB REG42 REG43 REG44: LSB
Reserved	REG45 through 50 are reserved for the LAN MAC address. These registers are set at the time of manufacturing.

(Re-)Writing to the last control register (REG60) is recommended after a configuration change to enact the change (Note: this is done automatically when using the graphical user interface).

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Status Registers

Digital status registers are read-only.

BER Measurement	
Parameters	**Monitoring**
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-7 Properly operating hardware will result in the following sequence being displayed: SREG0/1/2/3/4/5/6/7 = 2C F1 95 xx 0F 01 00 24
Dummy status	Read this dummy status register to latch in (freeze) multi-byte status words such as bit error count, etc. SREG8
Slave demodulator locked	'1' when the demodulator is configured as slave and it detects reliable periodic Start Of Superframe sync words from the remote master. SREG8(0)
Bit Errors	Bit errors can be counted when a PRBS-11 test sequence is transmitted. Number of bit errors in a 800,000 bit window. 32 bit unsigned. SREG9: error_count[7:0] SREG10: error_count[15:8] SREG11: error_count[23:16] SREG12: error_count[31:24] The bit errors counter is updated once every periodic measurement window. Reading the value will not reset the counter. One must read status register SREG8 prior to reading this bit error count.
BER Synchronization status	0 = not synchronized. 2047-bit pattern is not detected. 1 = synchronized SREG13 bit 0.
Reserved	SREG14/15/16
TCP-IP Connection Monitoring	
Parameters	**Monitoring**
TCP-IP connected	1 = connected, 0 otherwise. SREG33(0): port 1024 data stream SREG33(1): port 1028, monitoring & control
Ethernet PHY ID (LSB)	Self-check. 22 when connected to COM-5102 or COM-5402 LAN interface. SREG34
MAC address	Unique 48-bit hardware address (802.3). In the form SREG35:SREG36:SREG37:…:SREG40

ComScope Monitoring

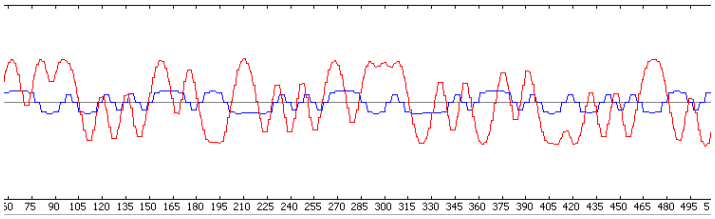
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1503 signal traces and trigger are defined as follows:

Trace 1 signals (demod)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: input signal I-channel	8-bit signed	f_{clk_rx}	512
2: phase difference between two successive symbols (center of the eye diagram)	8-bit signed	1 samples /symbol	512
3: cumulative symbol timing correction	8-bit signed	symbol rate	512
Trace 2 signals (demod)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: input signal after frequency translation to baseband and decimation	8-bit unsigned	4 samples /symbol	512
2: front-end AGC	8-bit unsigned	AGC update rate	512
3: AFC frequency correction	8-bit signed	f_{clk_rx}	512
Trace 3 signals (mod)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: modulator output (I-channel) after frequency translation	8-bit signed	f_{clk_rx}	512
Trigger Signal	**Format**		
1: demodulated start of frame = first data symbol in the data segment.	1-bit		
2: transmit burst enable	1-bit		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk_rx} processing clock as real-time sampling clock.

In particular, selecting the $\mathbf{f_{clk\_rx}}$ processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing the demodulated symbols (blue trace1/signal 2) and the received signal I-channel after frequency translation to baseband (red trace2/signal 1)

ComScope Window Sample: showing the demodulated symbols at the symbol center (blue trace1/signal 2, dots)

Operation

FSK Modulation

The FSK modulation and its derivatives (CPFSK, MSK, GMSK, GFSK) are best described by the following equations for the modulated signal s(t). The first equation describes a phase modulator, with the modulated centered around the center frequency f_c.

$$s(t) = \sqrt{\frac{2E_s}{T}}.\cos(2\pi f_c t + \theta(t) + \theta_0)$$

where

- E_s is the energy per symbol
- T is the symbol period
- f_c is the center frequency
- $\theta(t)$ is the phase modulation

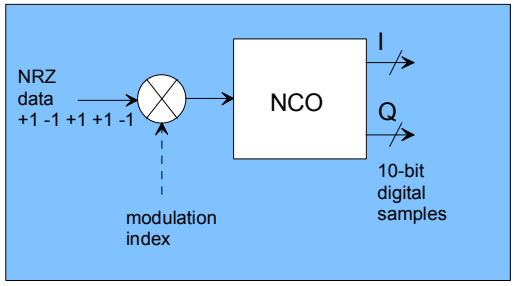
The COM-1503 implements a continuous phase FSK modulator. There are no phase discontinuities between symbols. The CPFSK phase modulation can be described as:

$$\theta(t) = \frac{\pi h}{T}\int_0^t a_i(t)dt$$

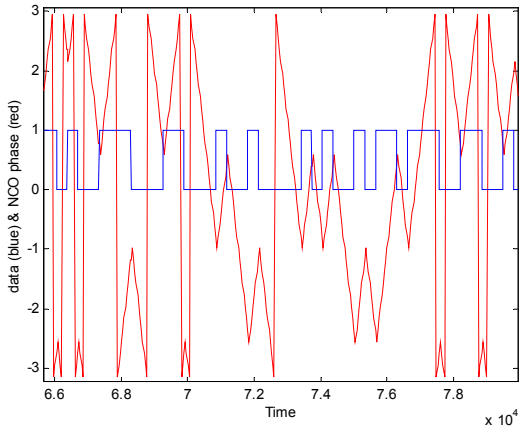
where:

- h is the modulation index. A modulation index of 0.5 yields a maximum phase change of π/2 over a symbol.
- a_i are the symbols. With 2-FSK, the binary data is represented as –1 (for '0') and +1 (for '1').

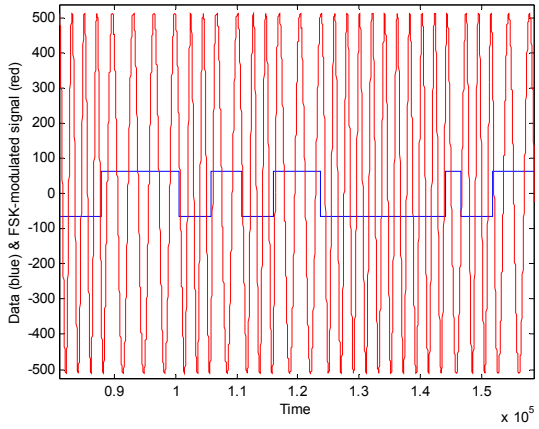
The generic implementation of a CPFSK modulator is based on the use of a numerically controlled oscillator (NCO) as shown in the block diagram below:



CPFSK modulator



NCO phase, continuous phase FSK 2-FSK, center frequency fc = 0, modulation index h = 0.5



Continuous FSK modulated signal example

FSK modulation is sometimes characterized by the frequency separation between symbols. The relationship between modulation index h and frequency separation is $f_{separation} = 0.5\ h\ f_{symbol\_clk}$

M-ary Number M

Transmitted data is grouped into symbols of size 1, 2, or 3 consecutive bits. The size of the symbol alphabet is thus M = 2, 4 or 8. The packing of serial data bits into alphabet symbols is such that the MSB is received first at the DATA_IN serial input.

The mapping between symbol alphabet and modulation symbol a_i is described in the table below:

Symbol alphabet	Modulation symbol a_i
2-FSK '0'	-1
2-FSK '1'	+1
4-FSK "00"	-3
4-FSK "01"	-1
4-FSK "10"	+1
4-FSK "11"	+3
8-FSK "000"	-7
8-FSK "001"	-5
8-FSK "010"	-3
8-FSK "011"	-1
8-FSK "100"	+1
8-FSK "101"	+3
8-FSK "110"	+5
8-FSK "111"	+7

Gaussian Filter

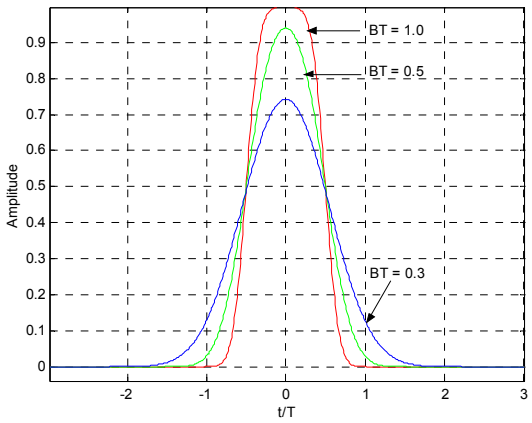
A filter with Gaussian impulse response can be used as pre-filtering of the symbols prior to the continuous phase modulation. Its purpose is to control the modulated signal bandwidth.

The Gaussian filter is characterized by its BT product (B is the –3 dB bandwidth, T is the symbol period = $1/f_{symbol\ rate}$). The lower the BT product, the narrower the modulation bandwidth and the higher the inter-symbol interference.

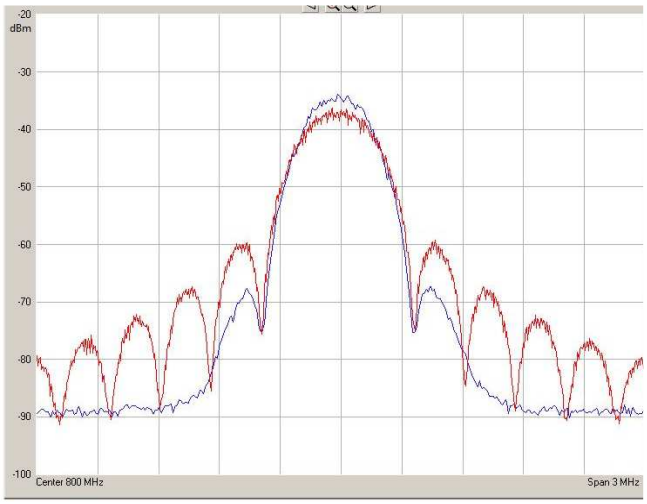
The filter impulse response is expressed analytically as: $h(t) = \frac{1}{\sqrt{2\pi}\sigma T}\exp\left(\frac{-t^2}{2\sigma^2 T^2}\right)$

where $\sigma = \frac{\sqrt{\ln(2)}}{2\pi BT}$

The impulse response h(t) is further convoluted with the rectangular waveform representing the symbol width T. The resulting impulse is illustrated below for BT = 0.3, 0.5 and 1.0.



Shaping pulses for BT = 0.3, 0.5 and 1.0 (Gaussian convoluted with rectangle window)



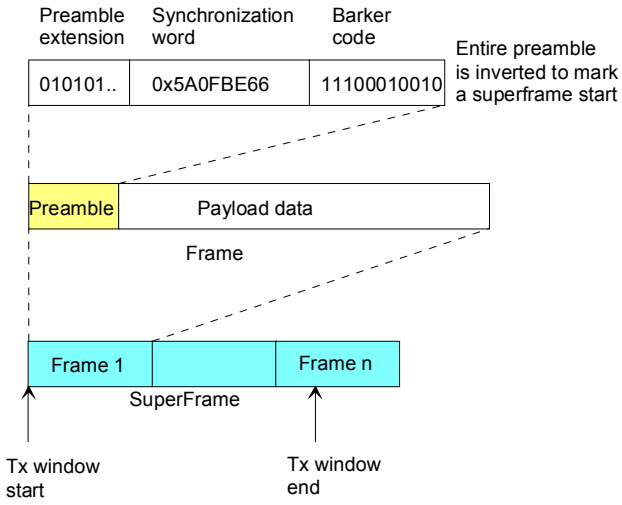
Output spectrum 500Ksymbols/s, mod index 0.5 GMSK BT=0.3 blue trace, MSK red trace

Burst Mode

Payload data is encapsulated within fixed-length frames. Each frame starts with a preamble comprising three fields:

- A variable length preamble extension consisting of alternating 0's and 1's. The purpose of this field is to give the receiver AGC enough time to converge. See the preamble extension control register REG18. This preamble extension is used only on the first frame in a superframe.
- A 32-bit synchronization field 0x5A0FBE66. In this field, the bit length is set at 1.5 times the nominal symbol length (to facilitate symbol synchronization at the receiver).
- A 11-bit Barker code 11100010010

The preamble is always 2-ary modulated. An inverted preamble marks the start of superframe.

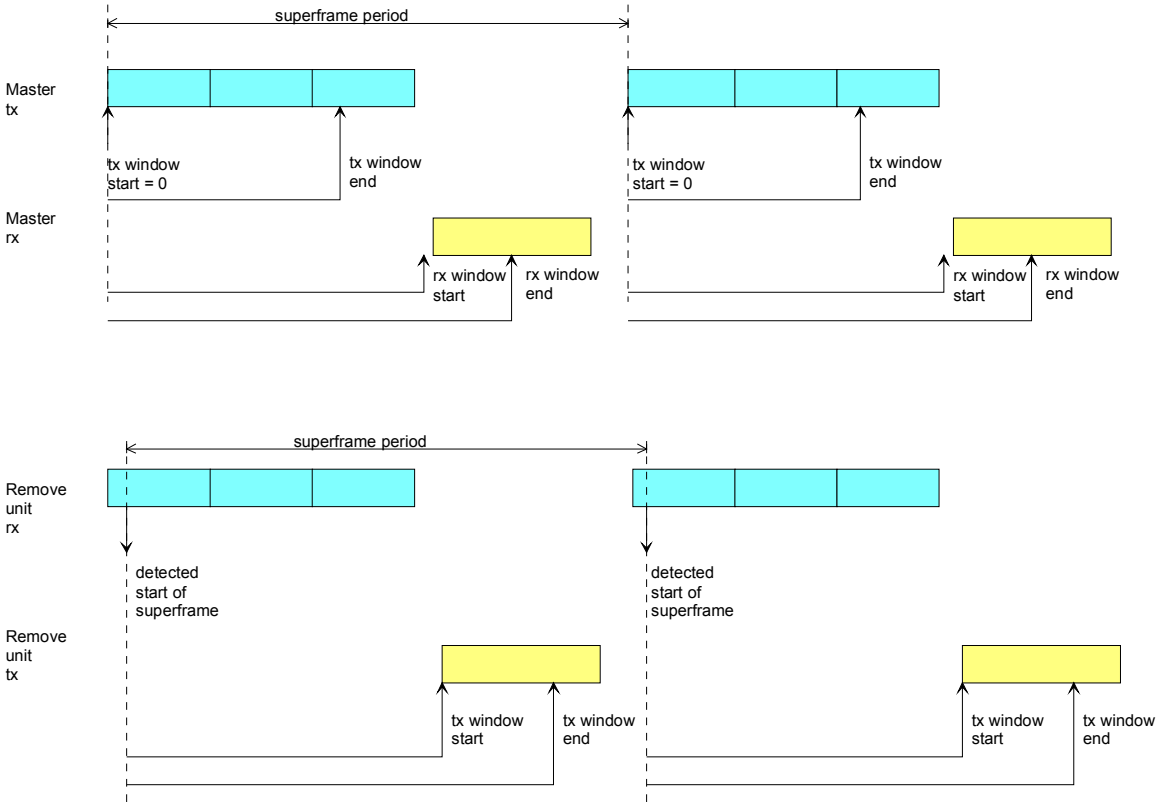


Superframe/Frame

The modulator segments the input stream into fixed-length frames. A frame will not be transmitted until at least Npl bits are queued for transmission. The application is responsible for flushing any data in the elastic buffer.

Network

A network comprises two types of modems: one acting as network master (base station), the others acting as network remote units. The master unit broadcasts periodic frame synchronization markers. The remote units are configured to transmit data during agreed upon time window.



The remote unit superframe period starts immediately after detecting the inverted preamble. It is therefore slightly delayed with respect to the master superframe period (by the preamble extension + preamble + propagation time + processing time).

Constellation: Symbol Mapping

The packing of serial data stream into symbols is done with the Most Significant bit first.

Symbol Timing

The demodulator is designed to acquire and track timing differences up to +/- 100ppm between the nominal (expected) symbol rate and the actual received symbol rate.

AGC1

The purpose of this AGC is to prevent saturation at the input signal A/D converter(s) while making full use of the A/D converters dynamic range. Therefore, AGC1 reacts to the composite input signal which may comprise not only the useful signal but also adjacent channel interferers and noise. The principle of operations is outlined below:

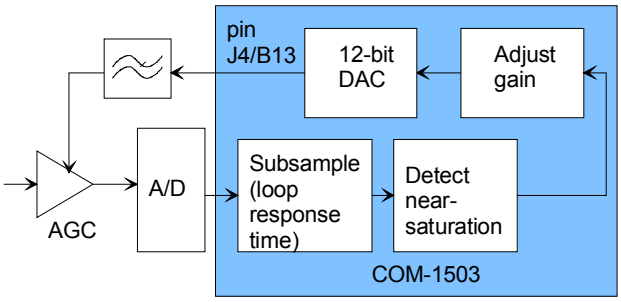
(a) Digital input samples are first subsampled according to the user-defined AGC1 response time.

(b) Near-saturation events are detected from the subsampled digital input samples and the AGC gain is adjusted accordingly.

(c) A 12-bit D/A converter generates the analog gain control signal RX_AGC1 for use by the external variable gain amplifiers. (pin J6/B13 left connector)

(d) Alternatively, the gain is controlled through the COM-3504 auxiliary 12-bit DAC1.

(e) The AGC1 loop can be closed or open, with the gain frozen at a user-specified level, by software command.

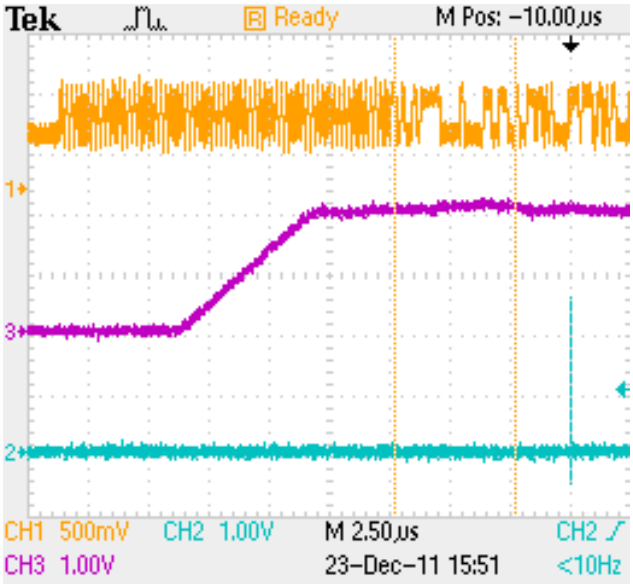


AGC1 principle

The user is responsible for selecting a preamble extension length (see control register REG18) long enough to give the receiver AGC enough time to converge at the beginning of a packet. Selecting the AGC response time time (see control register REG39) is a tradeoff between fast convergence and loop stability.

The figure below illustrates the AGC converging during the 010101 preamble extension and being stable during the 32-bit sync word (delineated by the two cursors).

Orange trace: received signal
Purple trace: receiver gain under AGC control
Blue trace: detected start of frame



Input Modulated Signal Pre-Processing

Prior to being routed to the demodulator, the input signal is subject to AGC1, variable decimation, and frequency translation to near-zero frequency.

The variable decimation consists of two half-band FIR filters and a Cascaded Integrated Comb (CIC) filter.

Output Modulated Signal Post-Processing

Several filters are used to clean the out-of-band output spectrum:

- two 10-taps half-band FIR filters in series
- a CIC interpolation filter.The interpolation factor R is set automatically.

Error Correction

A low (1.2%) overhead error correction can be applied to the full data stream. It cannot be applied to individual frames. When enabled, this long BCH code (16008,16200,12) corrects 12 bit errors in a 16Kbit frame.

USB

The USB port labeled HIGH-SPEED can be used to send and receive high-speed payload data as well as modem monitoring and control information. It is equipped with a mini type AB connector. (G = GND). The COM-1503 acts as a USB device.

The other USB port labeled DEVelopment can be used for modem Monitoring and Control only. It cannot convey payload data.

See http://comblock.com/download/USB20_UserManual.pdf for details.

LAN / TCP-IP

A built-in TCP server can be used to transfer high-speed data over the network. A plug-in 10/100/1000 Mbps Ethernet interface (such as the COM-5102 or COM-5401) is required to use this feature.

Initial Configuration (via USB)

The IP address must first be configured over non-TCP-IP connections such as USB or through other ComBlocks. This network setting is saved in non-volatile memory (see control registers 41 through 44). The TCP-IP connection can be used once the correct network setting is configured and after a power cycle.

TCP-IP

As a Server, the module opens the following sockets in listening mode:

Port 1024: modem data streams
Port 1028: monitoring and control port

Ping

The module responds to ping requests with size up to 470 bytes. Ping can be used to check the module response over the network. Ping can be used at any time, concurrently with other transmit and receive transactions. For example, on a Windows operating system, open the Command prompt window and type "ping –t –l 470 172.16.1.128" to send pings forever of length 470 bytes to address 172.16.1.128.

Concept

The COM-1503 converts a serial data stream into a TCP-IP socket stream. TCP, IP and Network information, and in particular routing information, are not transmitted from one end to the other.

At the receiving end, the network client must first connect to the COM-1503 to receive data.

A key assumption is that the network client is reading as fast as the demodulator(s) can forward demodulated data. If not, an overflow condition will occur and data may be lost.

Format Conversion

Serial to parallel conversion occurs when converting the demodulated data stream into 8-bit byte over the TCP-IP link. The key rule is that the first received bit is placed at the MSb position in the byte.

Timing

Clock Architecture

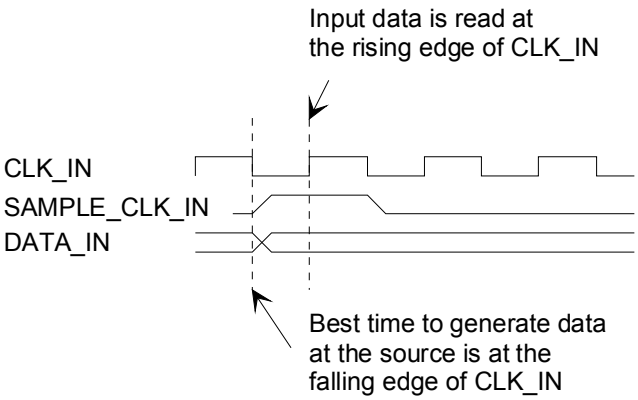
The symbol rate is derived from an internal 60 MHz clock or an external 10 MHz frequency reference.

I/Os

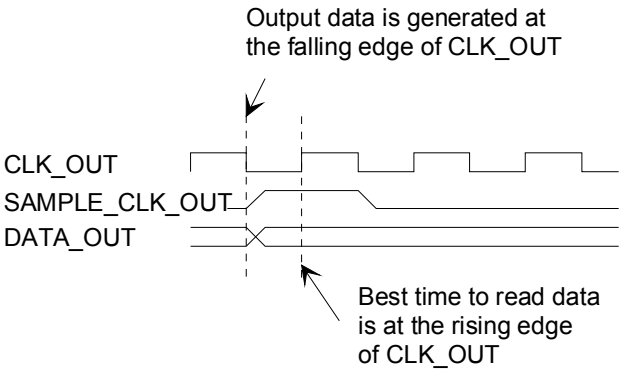
The digital signals on connectors J6 and J9 are LVTTL (0 – 3.3V) single-ended signals by default.

All I/O signals are synchronous with a reference clock located on pin A1. The general rule is that the output signals are generated at the falling edge of the synchronous clock while the input signals are read at the rising edge of the synchronous clock, as illustrated in the simplified timing diagrams below.

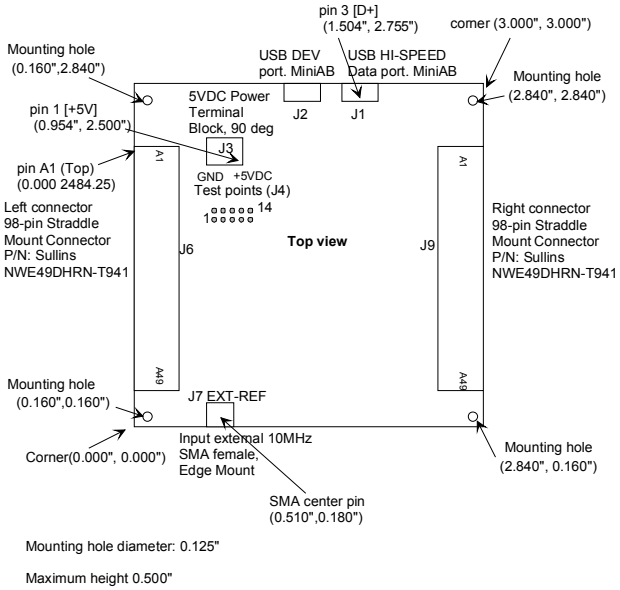
Input



Output

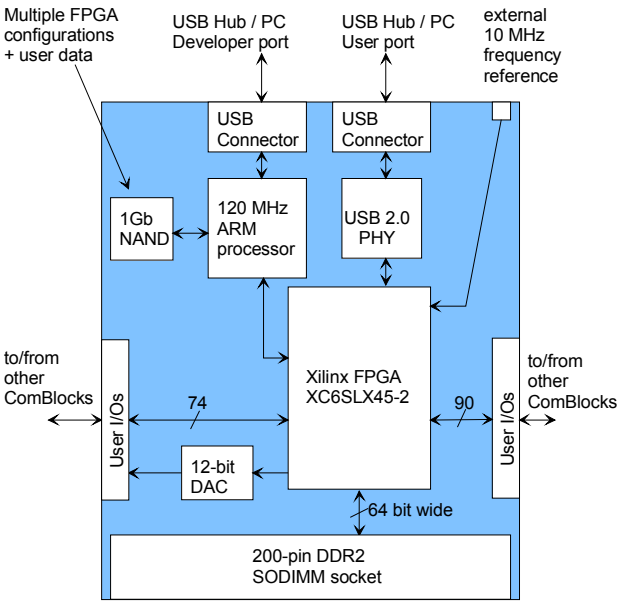


Mechanical Interface



Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1500schematics.pdf

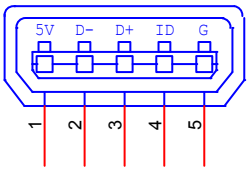


COM-1503 Hardware Block Diagram

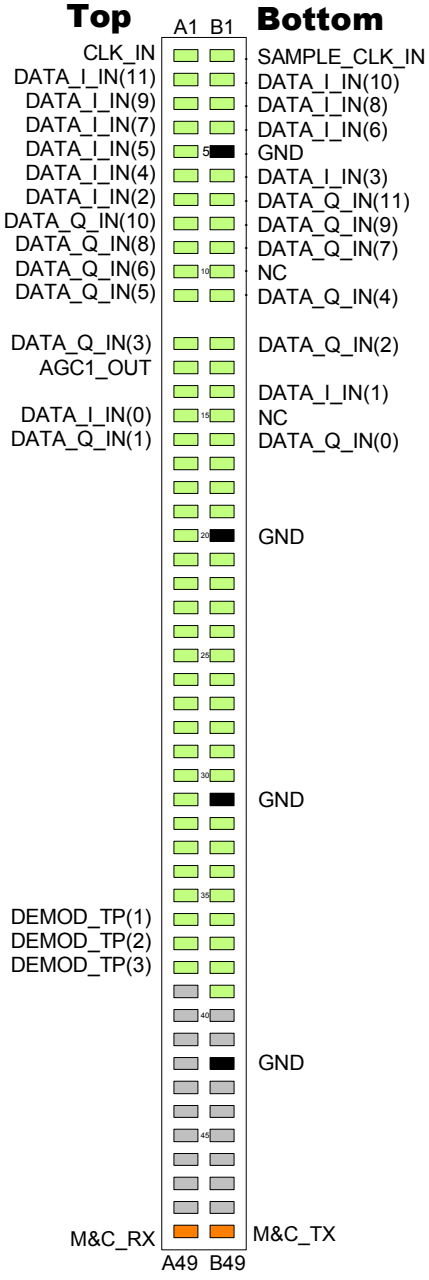
Pinout

USB

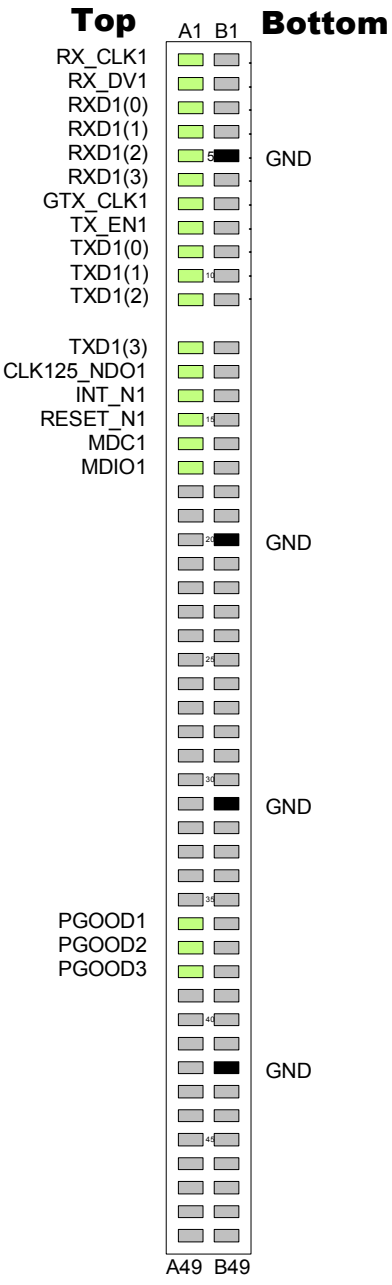
The USB port labeled HIGH-SPEED is equipped with a mini type AB connector. (G = GND).



Left Connector J6

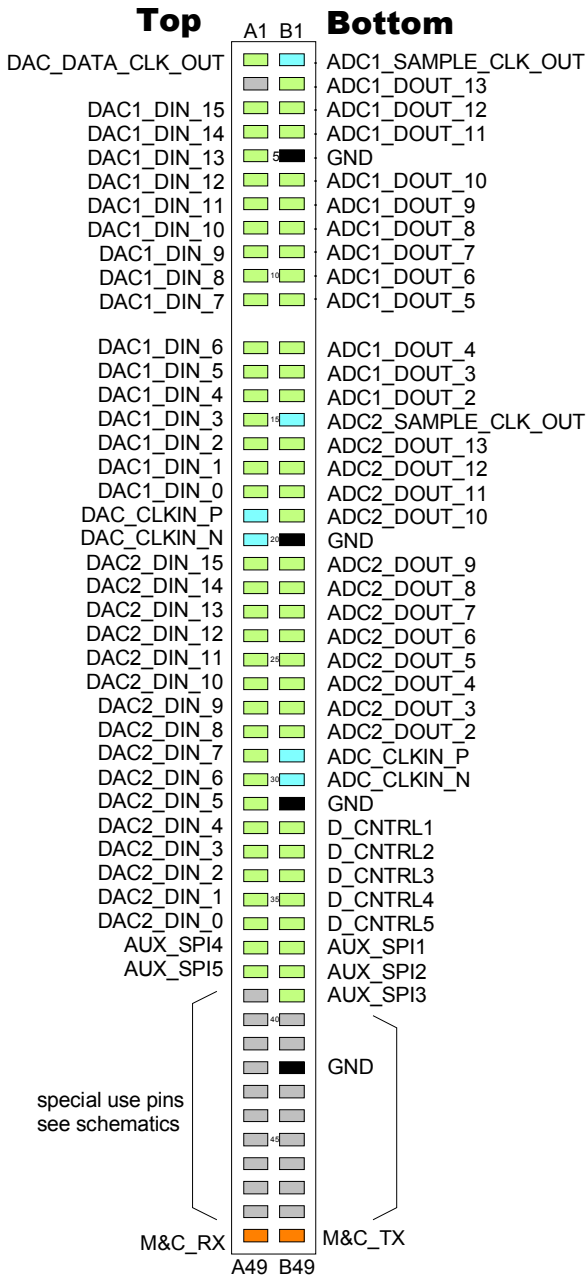


This interface is compatible with the COM-30xx family of RF receivers.

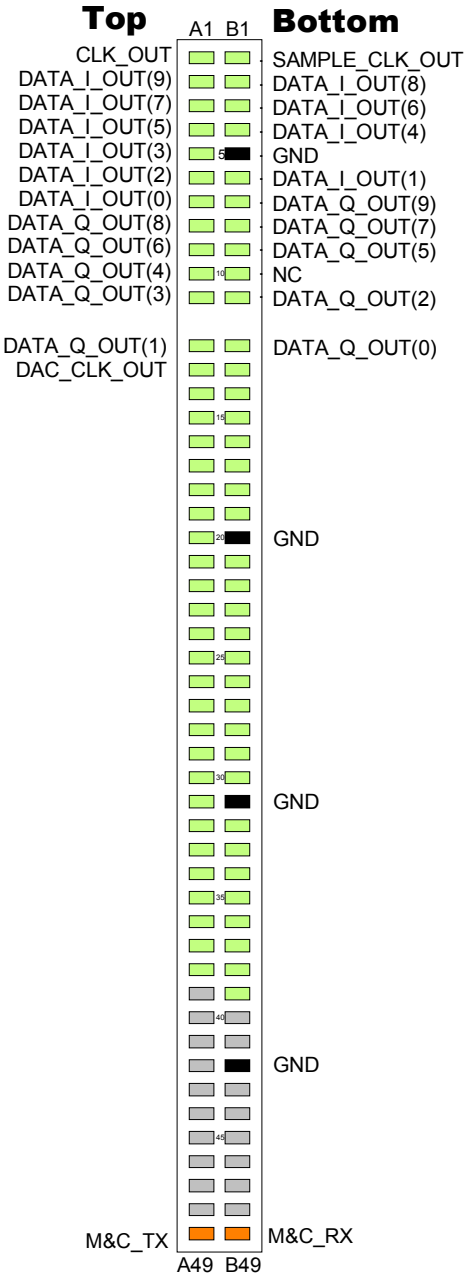


This interface is compatible with the COM-5102/COM-5401
10/100/1000 Mbps Ethernet PHY

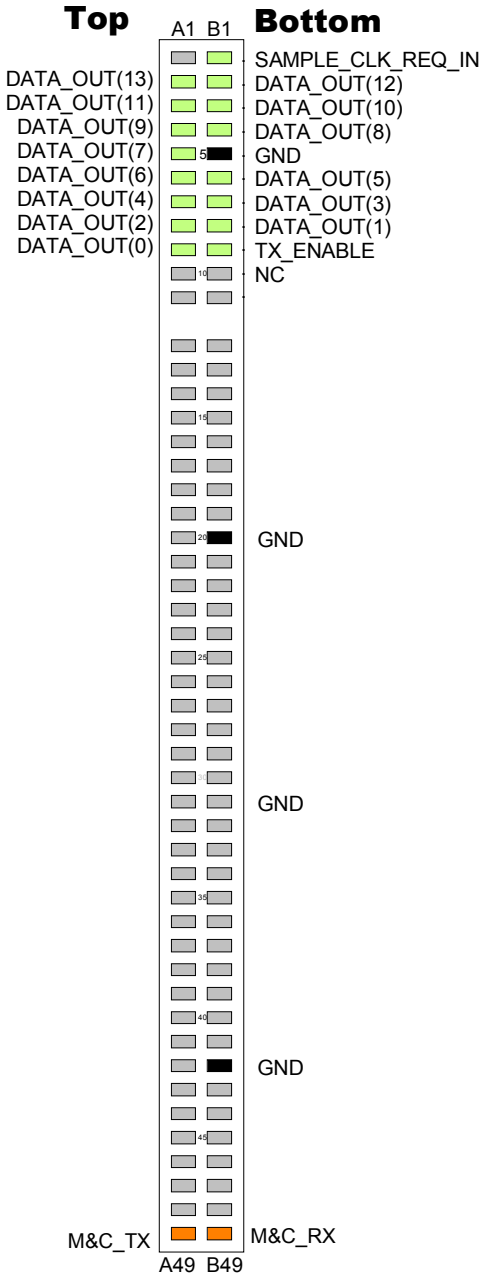
Right Connector J9



This interface is compatible with the COM-3504 dual Analog<->Digital Conversions.



This interface is compatible with the COM-2001 dual DACs.



This interface is compatible with the COM-4004 DDS modulator.

Todo: Add COM-7002

98-pin to 40-pin adapters to interface with other Comblocks are supplied free of charge. Please let us know about your interface requirements at the time of order.

I/O Compatibility List

(Not an exhaustive list)

Analog / RF front-ends
COM-30xx RF receivers [using 98-pin – 40 pin adapter COM-9108
COM-3504 Dual Analog <-> Digital Conversions
COM-2001 digital-to-analog converter (baseband).
COM-4004 70 MHz IF Modulator
Digital interface
COM-7002 Turbo code encoder/decoder
Host PC via USB 2.0
COM-5102 Gigabit Ethernet + HDMI interface
COM-5401 4-port 10/100/1000 Mbps Ethernet Transceivers
COM-1600/1500 FPGA + ARM development platforms

Configuration Management

This specification document is consistent with the following software versions:

- COM-1503 FPGA firmware: Version 0 and above.
- ComBlock Control Center graphical user interface: Revision 3.05d and above.

The option and version of the FPGA configuration currently active can be read from the ComBlock Control Center in the configuration panel (advanced).

Troubleshooting

1. No demodulator lock:
Check the modulated signal for saturation after changing the symbol rate. Saturation in the modulated signal will cause the demodulator to lose lock. Adjust the modulator signal gain accordingly.

2. No demodulator lock:
Check the AGC response with respect to the burst preamble. The burst preamble extension must be long enough for the receiver AGC to converge to a stable stage. Adjust the AGC response time and/or the preamble extension accordingly.

3. Bit error rate is 0xC3500 (all bits wrong):
Invert the spectrum at the receiver.

4. High bit error rate and distorted input signal:
Check that any programmable filter prior to the demodulator (for example the LPF within the COM-3011) is configured to pass the entire modulated spectrum.

ComBlock Ordering Information

COM-1503 FSK/MSK/GFSK Burst modem

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