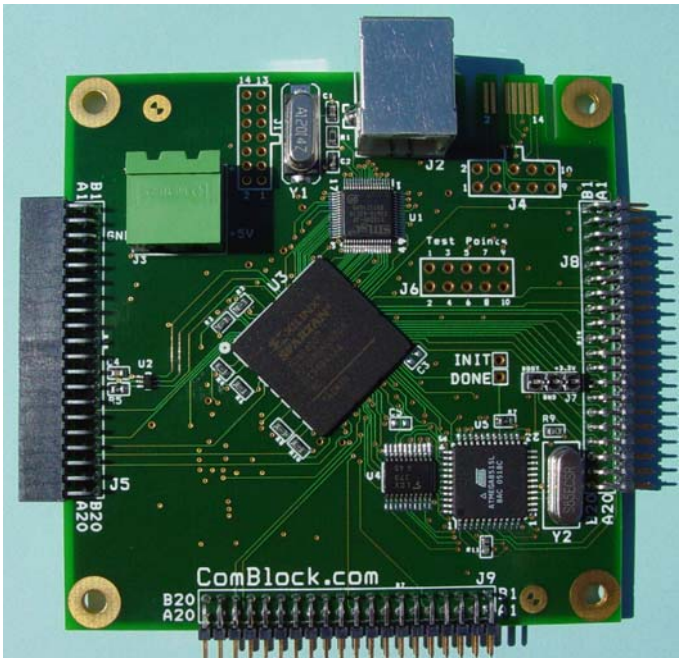
COM-1400
FPGA DEVELOPMENT PLATFORM (Spartan3-400) & USB 2.0 INTERFACE

Key Features

- Low-cost generic platform for custom application development.
- Xilinx Spartan-3 XC3S400-4 FPGA features 400K system gates including 288Kbit of dual port memory and 16 dedicated 18x18 multipliers.
- USB 2.0 interface supports signaling rates of 480 Mbit/s (High Speed) and 12 Mbit/s (Full Speed). Typical sustained data throughputs are 85 Mbit/s (HS) and 6.5 Mbit/s (FS).
- Supports **multiple personalities** and **dynamic reconfiguration**:
  - up to 7 custom FPGA configurations can be stored in non-volatile flash memory.
  - The selected configuration is automatically reloaded at power up or upon software command within 0.4 seconds.
- Graphical User Interface is used for remote monitoring and control over a USB link. This includes loading the FPGA configuration file into non-volatile flash memory.
- This module is interface compatible with other pre-programmed ComBlock modules via standard 2-row 40-pin 2mm connector.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.

Development environment includes
- Graphical user interface
- Hardware schematics
- USB Windows driver (.sys and .inf files),
- VHDL template code
- USB interface Java API and associated .jar and .dll files
- USB interface C++ API and associated .dll file
- USB NGC component

- Tools required (not provided):
- Xilinx ISE (7.1 or later recommended) with XST or other VHDL synthesis tools
- Java development environment or C++ compiler, for custom USB applications



For the latest data sheet, please refer to the **ComBlock** web site: ComBlock.com/download/com1400.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to ComBlock.com/product_list.htm.

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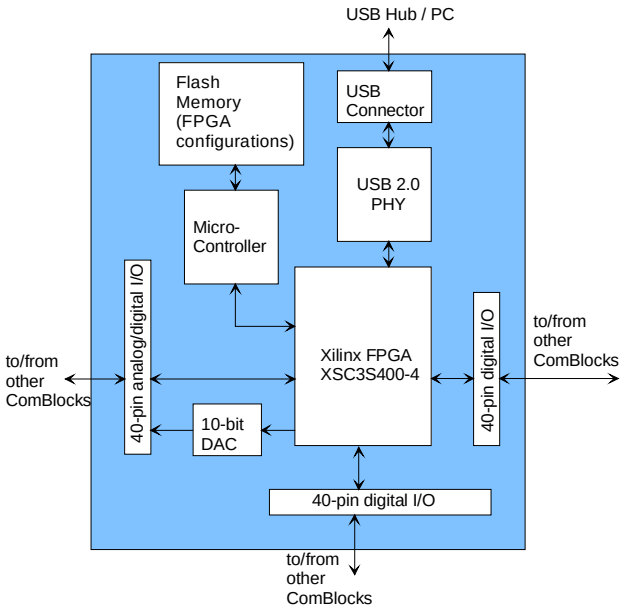


Com-1400 Block Diagram

Standard and Optional Interfaces

Interface	Included	Maximum sustained throughput
Low-voltage TTL 0 – 3.3V LVTTL	Yes	40 Msamples/s per pin
USB 2.0	Yes	86 Mbit/s
LVDS	Yes	90 Msamples/s per pin
LAN TCP-IP	Option COM-5003	50 Mbit/s
RS232C (future)	Option COM-5102	
RS422/485 (future)	Option COM-5102	10 Mbit/s per signal

Absolute Maximum Ratings

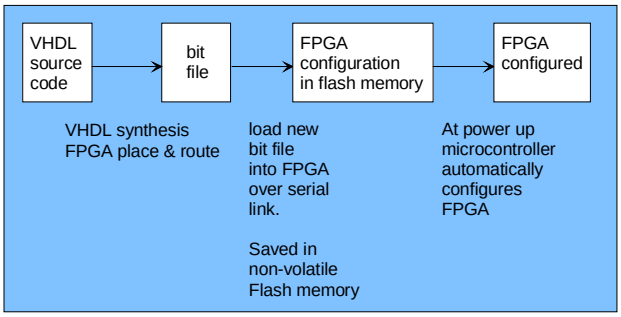
Supply voltage	-0.5V min, +6V max
40-pin connector inputs (when configured as LVTTL)	-0.5V min, +3.6V max
40-pin connector inputs (when configured as LVDS)	TBD

Important:
The I/O signals connected directly to the FPGA or Atmel microcontroller are NOT 5V tolerant!

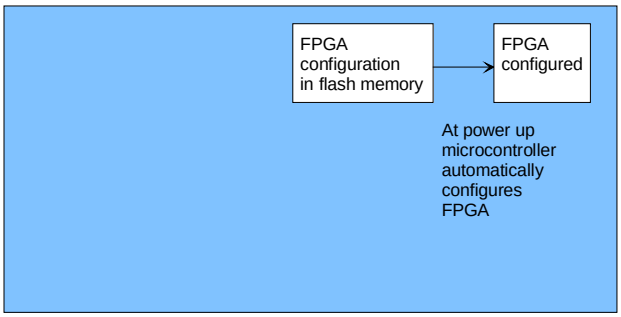
Do not connect LVDS-configured FPGA I/Os to LVTTL-configured external devices and vice versa.

Application Development Process

FPGA/VHDL



Development environment



Run-time environment

Operations

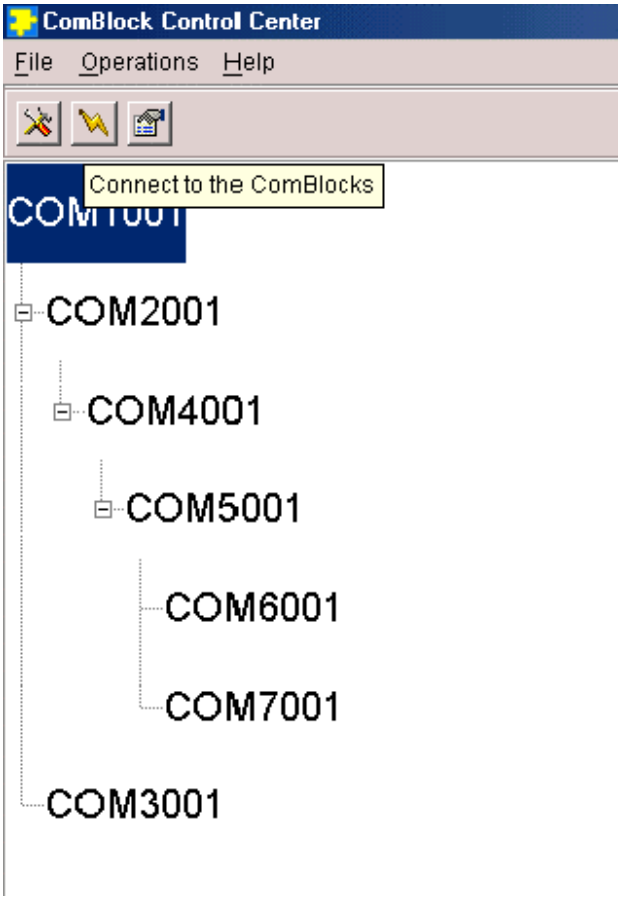
Graphical User Interface

A user-friendly graphical user interface (hereafter named ComBlock Control Center) is supplied with the COM-1400. The ComBlock Control Center runs on a host computer with the Windows XP, 2000 or later operating system. It allows the user to communicate with the COM-1400 over the USB 2.0 interface and when other ComBlocks are connected, via serial link or LAN.

The primary use of the ComBlock Control Center is to:

(a) download new FPGA firmware (into non-volatile Flash memory)
(b) set control registers
(c) monitor status registers
(d) capture and display internal signals (ComScope)

When activated, the ComBlock Control Center enumerates the ComBlock modules within the assembly. The modules are identified by their name in a tree-like structure. Each module can be configured and monitored remotely.



The ComBlock Control Center software is provided with all ComBlock modules. The user's manual can be found at ComBlock.com/download/ccchelp.pdf.

Flash Memory

The FPGA configuration is stored in non-volatile (Flash) memory. The ComBlock Control Center includes the utility to (re)write the FPGA .mcs PROM file into the flash memory over the selected communication link.

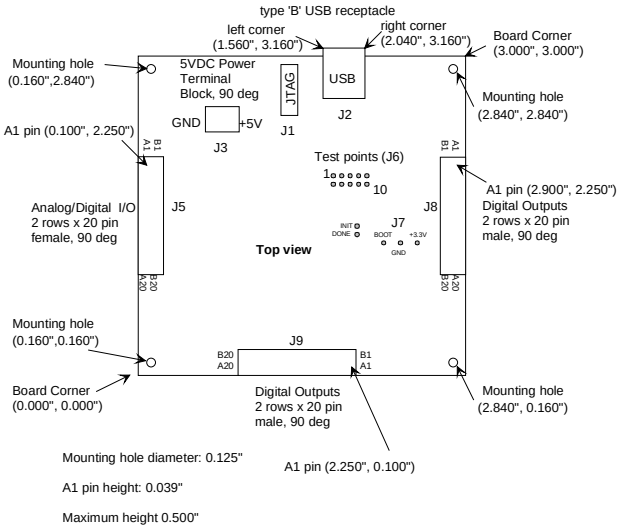
Communication links: the COM-1400, when used as a stand-alone module, communicates with the ComBlock Control Center exclusively over USB. When part of a larger ComBlock assembly, the COM-1400 can communicate over any other communication link supported by the assembly, namely asynchronous serial, USB, LAN or PCMCIA.

The FPGA is automatically configured after power-up or reset with the configuration file stored in Flash memory. The configuration file size for the XC3S400 is 1,699,136 bits. Configuration time is typically 0.4 sec.

Accidental FPGA file corruption

The COM-1400 is protected against corruption by an invalid FPGA configuration file. To recover from such occurrence, connect the BOOT pin to the nearby ground pin using a jumper and power-up the COM-1400. Remove the jumper after 1 second. The COM-1400 will be automatically configured with a default FPGA configuration which restores USB communication. This boot file is un-erasable. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

Mechanical Interface



The front dimensions (plug face) of a type 'B' USB receptacle are 12 mm wide by 11 mm tall (above the board.)

Schematics

The board schematics are available on-line at ComBlock.com/download/com_1400schematics.zip

VHDL code template

A VHDL template project is available from the ComBlock CD or on-line at ComBlock.com/download/com1400_009.zip
The template project includes:

- the VHDL source code (.vhd)
- the constraint file (.ucf) listing all pin assignments
- The Xilinx ISE project with the synthesis and implementation settings
- The resulting bit file (.mcs) is ready to be loaded into flash memory

The sample code describes how the application interfaces with the ComBlock Control Center graphical user interface through control and monitoring registers. Monitoring and control messages and syntax are described in ComBlock.com/download/m&c_reference.pdf.

It also describes how to capture key internal signals in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center.

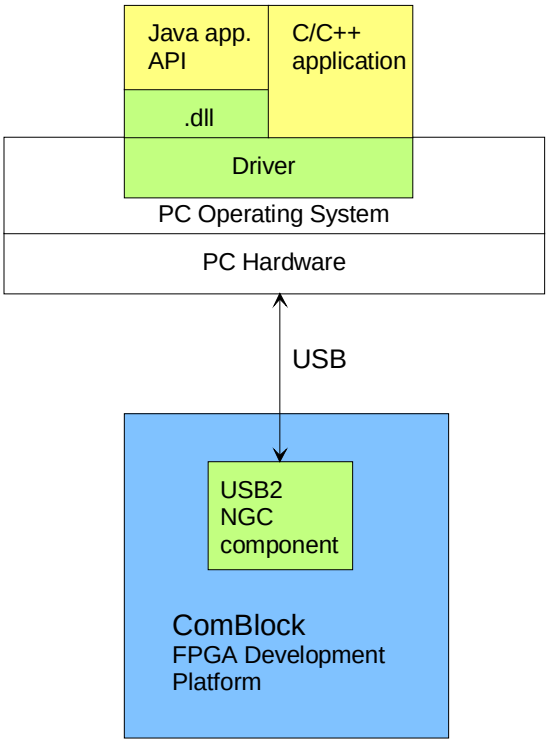
The ComScope user manual is available at ComBlock.com/download/Comscope.pdf.

USB 2.0 Driver

Software to help developers create USB high-speed communications between the COM-1400 platform and a host PC is provided. The **USB 2.0 software package** includes the following:

- USB20 NGC component for integration within the VHDL code (Occupies 23% of FPGA resources)
- VHDL top-level code template
- Windows device driver for XP/2000 (.sys, .inf files)
- Java API, .dll and application sample code
- C/C++ application sample code

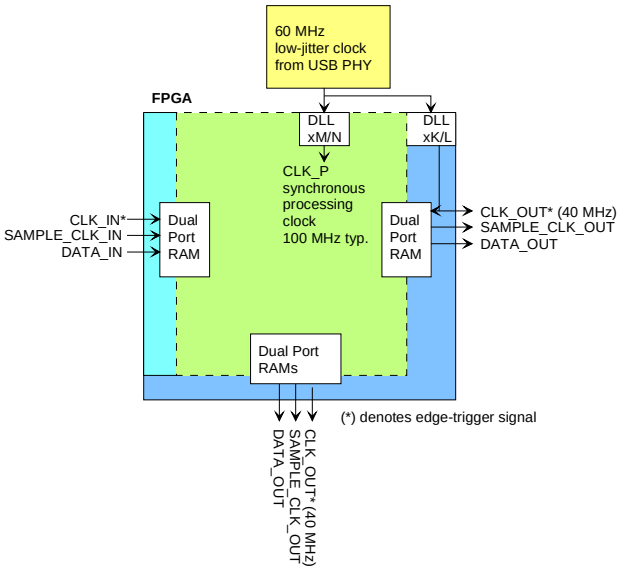
The **USB 2.0 software package** is available in the ComBlock CD and can also be downloaded from ComBlock.com/download/usb20.zip.
The user manual is available at ComBlock.com/download/USB20_UserManual.pdf



Blue: supplied hardware
Green: supplied ready-to-use software
Yellow: source code examples

Clock Architecture

The clock distribution scheme embodied in the VHDL source code template is illustrated below.



The core signal processing performed within the FPGA is synchronous with the CLK_P processing clock. The processing clock frequency is programmable as 60 MHz * M/N, at the time of

VHDL synthesis by settings the M/N ratio in the DCM attribute of the VHDL source code. In practice, a processing frequency around 100 MHz is consistent with the Spartan-3 technology (i.e. timing constraints are met without resorting to excessive pipelining/re-clocking). In order to minimize clock jitter, the CLK_P processing clock is derived from a 60 MHz low-jitter reference clock originating from the USB 2.0 PHY integrated circuit.

The signals at the digital input connector J5 are synchronous with the CLK_IN signal at J5/A1. This clock is typically 40 MHz.

The signals at the digital output connector J6 are synchronous with the 40 MHz CLK_OUT signal derived from the 40 MHz oscillator.

Dual-port RAM elastic buffers are used at the boundaries between I/Os and internal processing area.

Other clock architectures are possible by changing the VHDL source code.

I/O Standards

The digital signals on connectors J5, J8 and J9 are LVTTL (0 – 3.3V) signals by default. However, the COM-1400 is designed to be easily transformed to support LVDS differential signals for higher speed interconnections on connectors J5 and J9 (J8 is always LVTTL). The transformation involves moving several surface mount 0603 0Ω resistors to change the specific V_{CCO} voltages from 3.3V to 2.5V.

Switching between LVTLL and LVDS I/O standards must be implemented concurrently for all signals on connectors J5 and J9 together. The Xilinx ISE will detect as illegal the coexistence of the LVTTL and LVDS I/O standards for signals declared on the same connector (i.e. FPGA I/O banks 0, 6 and 7). The VHDL programmer is responsible for ensuring that banks 0, 6 and 7 are configured for the same I/O standard.

For best performances with LVDS, the internal termination must be enabled by enabling the digitally controlled impedance (DCI) in the Xilinx ISE project.

In addition to VHDL software changes, all 3 surface mount resistors should be moved (soldered) as follows:

J5/J9 as LVTTL	J5/J9 as LVDS
R23: 0 Ω 0603	R23: open
R33: 0 Ω 0603	R33: open
R34: 0 Ω 0603	R34: open
R26: open	R26: 0 Ω 0603
R31: open	R31: 0 Ω 0603
R32: open	R32: 0 Ω 0603

Warning: please make sure that custom FPGA configurations define pins J9/A9 and J9/A19 either as high-impedance or as zero when LVDS is used, to avoid any conflicts with other external devices.

Digital to Analog Converter (DAC)

A 10-bit DAC/Analog output is built-in for gain control. The DAC output is connected to pin "B13" of the J5 connector. The DAC can be disabled in software to a high impedance state or physically disabled by removing the 0Ω R5 resistor.

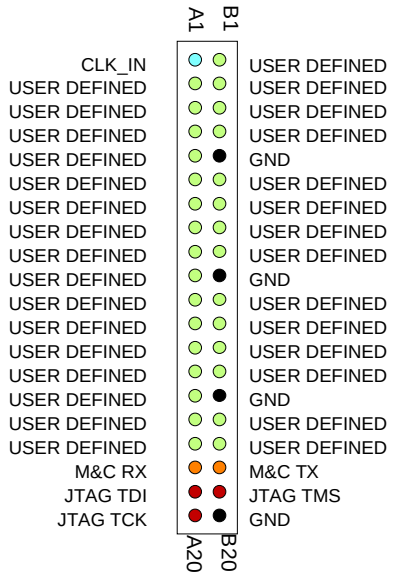
The DAC can typically operate at a 0.5V/µsec slew rate. The output voltage range is from 0 to 3.3 V. The driver provided in the code template allows for approximate refresh rate of up to 1.765 MHz (slew rate limited.)

Pinout

USB

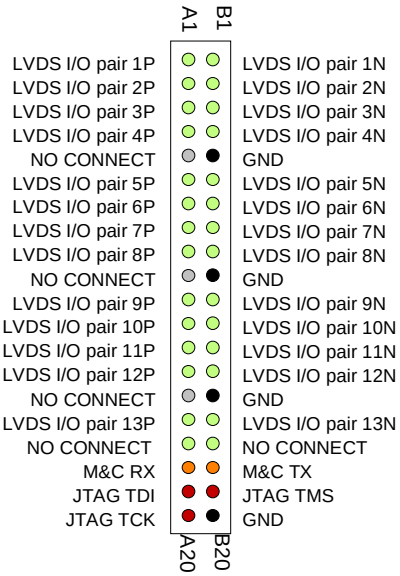
USB type B receptacle, as the COM-1400 is a USB device.

Digital Input Connector J5



(Default LVTTL)

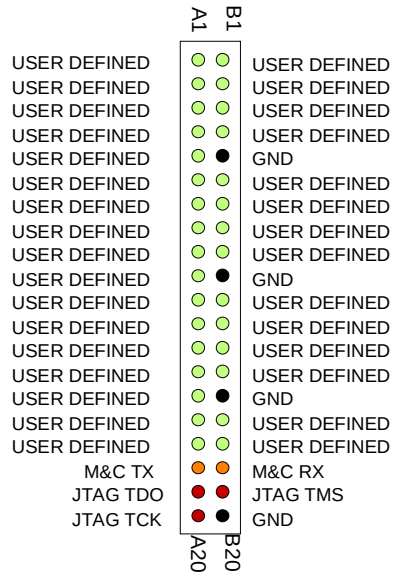
Note: although the J5 connector is generally referred to as 'Input', individual user-defined pins can be configured as 'IN', 'OUT', or 'INOUT' in the user VHDL source code.



(Differential LVDS)

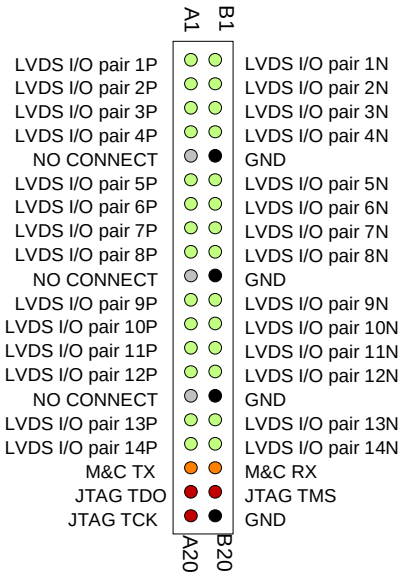
Note: LVDS support requires board modification (moving three resistors for switching the FPGA V_{CCO} supply voltage).

Digital Output Connectors J8/J9



(Default LVTTL)

Note: although the J8 and J9 connectors are generally referred to as ''Output', individual user-defined pins can be configured as 'IN', 'OUT', or 'INOUT' in the user VHDL source code.



(Differential LVDS J9 only)

Note: LVDS support requires board modification (moving several resistors for switching the FPGA V_{CCO} supply voltage).

I/O Compatibility List

(Not an exhaustive list)

Digital Input
COM-3001/2/3/4/5/6 RF receivers.
COM-1002 BPSK/QPSK/OQPSK modulator
COM-1012/1019 Direct-sequence spread-spectrum modulator
COM-1028 FSK/MSK/GFSK/GMSK modulator
COM-8001 Arbitrary waveform signal generator, 256MB/1GB, 40 Msamples/s.
Digital Output
COM-1001 BPSK/QPSK/OQPSK demodulator
COM-1011/1018 Direct-sequence spread-spectrum demodulator
COM-1027 FSK/MSK/GFSK/GMSK demodulator
COM-1008 Variable decimation
COM-8002 High-speed data acquisition. 256MB/1GB, 40 Msamples/s.

ComBlock Ordering Information

COM-1400 FPGA development platform

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