COM-1008 VARIABLE DECIMATION (1:1024) & PILOT TONE DETECTION VHDL SOURCE CODE OVERVIEW

Overview

The COM-1008 ComBlock Module comprises two pieces of software:

- VHDL code to run within the FPGA for all signal processing functions
- C/Assembly code running within the Atmel AT90S8515 or ATMega8515L microprocessor for non application-specific monitoring and control functions.

The VHDL code interfaces to the monitoring and control functions by exchanging byte-wide registers on the Atmel microcontroller 8-bit data bus. The control and monitoring registers are defined in the specifications [1].

The COM-1008 VHDL code runs on the generic COM-1000 hardware platform. The schematics [2] for this platform are available in this CD.

Reference documents

[1] specifications: com1008.pdf

[2] hardware schematics: com_1000schematics.pdf

[3] VHDL source code in directory
com-1008_010\src

[4] .ucf constraint files (-A and –B options)
com-1008_010\src\com1008A.ucf
com-1008_010\src\com1008B.ucf

[5] .mcs FPGA bit files (-A and –B options)
com-1008_010\com1008A_010.mcs
com-1008_010\com1008B_010.mcs

Configuration Management

The current software revision is 10.
Two software options (-A and –B) can be created:

- COM-1008-A Interface with other ComBlocks
- COM-1008-B Interface with a 16-bit data bus.

The option can be selected by:

(a) selecting the root (top level) file as com1008A.vhd or com1008B.vhd.
(b) selecting the relevant –A or –B ucf constraint file.

VHDL development environment

The VHDL software was developed using the Xilinx ISE 4.1 development environment. The synthesis tool is FPGA Express 3.6.

Target FPGA

The VHDL code was synthesized for the Xilinx Spartan-II XC2S200-5PQ208 FPGA.

Xilinx-specific code

The VHDL source code was written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- BUFG
- IBUFG
- RAMB4_S16_S16

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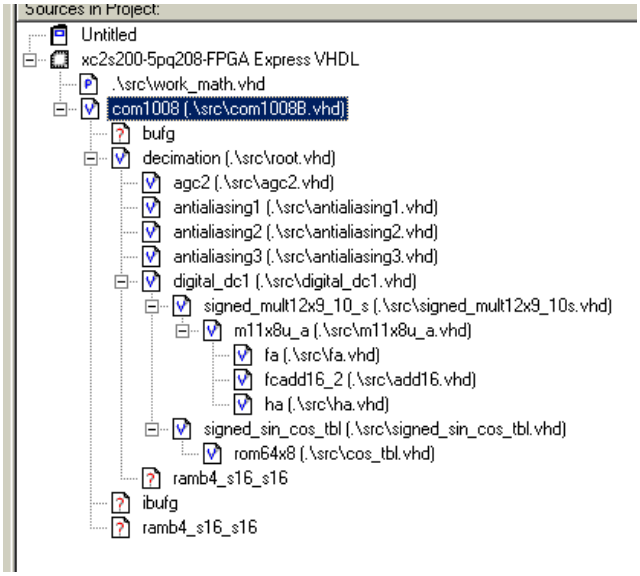
VHDL software hierarchy

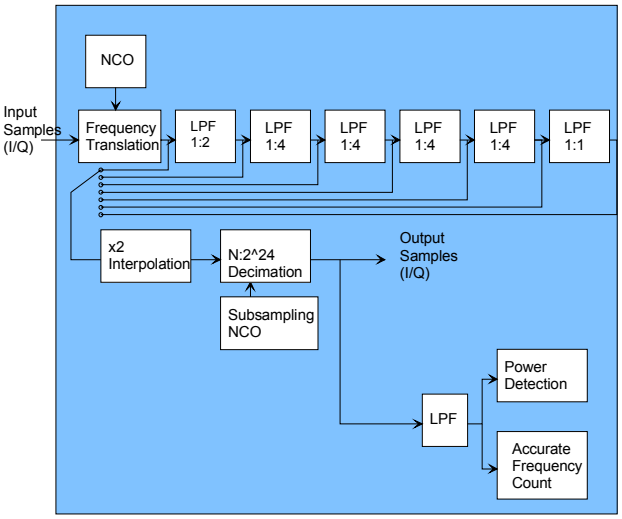


The code is stored with one, and only one, entity per file as shown above.

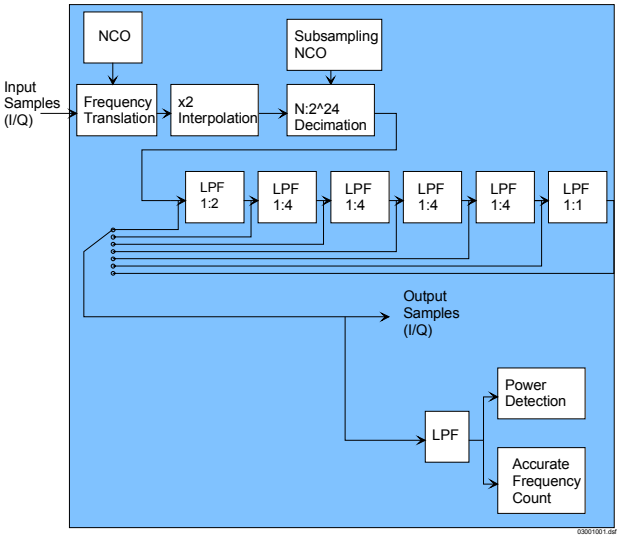
Clock / Timing

The software uses a single master clock (CLK_IN2) which serves as processing clock, input clock and output clock. The code is written to meet the timing requirements on the target FPGA at a speed of at least 40 MHz.

Block Diagram



Variable Decimation + Pilot Tone Detection (Variable decimation stage last)



Variable Decimation + Pilot Tone Detection (Variable decimation stage first)

Contact Information

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