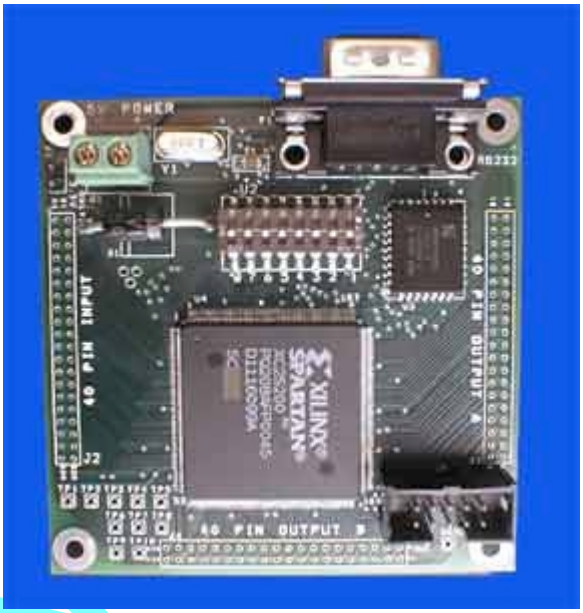
COM-1007A REED-SOLOMON DECODER

Key Features

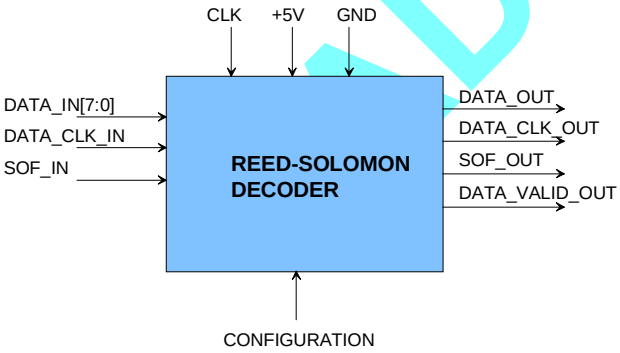
- Reed-Solomon error correction decoder.
- Variable data rates up to 1.4 Mbps input.
- Two commonly used (N,K,t) RS configurations.
  (N,K,t) = (255, 233, 11)
  (N,K,t) = (80, 56, 12)
- Automatic frame synchronization.
- Single 5V supply
- Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom)
- Interfaces with 5V and 3.3V logic.

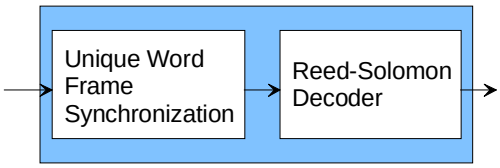


For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1007.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

RS Decoder Inputs / Outputs





Electrical Interface

Input Module Interface	**Definition**
DATA_IN[7:0]	Input data. Select 1-bit serial or 8-bit parallel format. In serial mode, data bit is on pin DATA_IN(0) and the most significant bit is transmitted first.
DATA_CLK_IN	Input bit/byte clock. One CLK-wide pulse. Read input data at rising edge of CLK when DATA_CLK_IN = '1'
SOF_IN	Input Start of RS frame. One CLK-wide pulse, aligned with DATA_CLK_IN. Marks the first byte in the input RS frame. This start of RS frame is generated internally when the unique word synchronization circuit is enabled.
Output Module Interface	**Definition**
DATA_OUT[7:0]	Output data. Select 1-bit serial or 8-bit parallel format. In serial mode, data bit is on pin DATA_OUT(0) and most

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	significant bit is transmitted first.
DATA_CLK_OUT	Output bit clock. One CLK-wide pulse. Read output data at rising edge of CLK when DATA_CLK_OUT = '1'
SOF_OUT	Output start of RS frame. One CLK-wide pulse, aligned with DATA_CLK_OUT. Marks the first bit in the output RS frame.
DATA_VALID_OUT	High when the decoder was able to correct all errors in the RS frame.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Operations

Reed-Solomon Codes

Field Generator Polynomial:
$p(x) = x^8+x^4+x^3+x^2+1$. in GF(8).

Code Generator Polynomial:
$g(x) = (x + \alpha^0).(x + \alpha^1).(x + \alpha^2)\ldots.(x + \alpha^{2t-1})$.
where $\alpha = 02_{HEX}$.

User selectable codeword length N and correction power t:
(N,K,t) = (80, 56, 12)
(N,K,t) = (255, 233, 11)

The maximum throughput depends on the code selection :
1.4 Mbps input rate for the (255,233,11) code.
0.7 Mbps input rate for trhe (80,56,12) code.

Unique Word

A unique word is used for synchronizing the received data stream with the periodic code blocks. The unique word is 32-bit long:
01011010 00001111 10111110 01100110 (binary)
0x 5A 0F BE 66 (hex)
The most significant bit (left-most) is transmitted first.

In order to limit the bandwidth expansion to less than 5%, the unique word transmission frequency depends on the code block size:

Code block size (including RS parity bits)	**UW transmission rate**
≥ 1024 bits	Once every block
≥ 512 bits and < 1024 bits	Once every two blocks

The unique word is not error corrected.

The unique word reception can be disabled by software command. This can be useful in configurations where frame synchronization references are available externally.

If unique word synchronization is enabled, the 32-bit unique word is removed from the received data stream prior to error correction.

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Configuration (via Serial Link / LAN)

Complete assemblies can be monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. The installation default values are highlighted in bold. All control registers are read/write.

Parameters	**Configuration**
RS Code	1100 = code (80, 56, 12) 1101 = code (255, 233, 11) Default value **1101**. REG0 bit 3-0
Internal / External clock selection	0 = internal clock 1 = external clock Default value **0**. REG1 bit 0
Input serial / parallel	00 = 1 bit serial 01 = 8-bit parallel Default value **00**. REG1 bit 2-1
Output serial / parallel	00 = 1 bit serial 01 = 8-bit parallel Default value **00**. REG1 bit 4-3
Rx unique word synchronization and removal.	0 = off 1 = on Default value **1**. REG1 bit 5
RS decoder bypass mode	When set, bypasses the Reed Solomon decoder. 0 = off 1 = on Default value **0**. REG1 bit 6

Monitoring (via Serial Link / LAN)

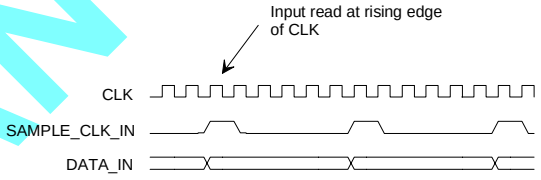
Parameters	**Monitoring**
Version	Returns '1007x' when prompted for version number.
Input Bit Errors	Bit error rate measured at the input of the decoder. The BER is expressed as the number of bit errors in a 100,000 bit window. This information is only available when the unique word detection is enabled. 17 bit unsigned. REG2: error_count[7:0] REG3: error_count[15:8] REG4: error_count[16]
Unique Word Synchronization status	The synchronization status is based on the presence of a periodic unique word. Not applicable if the unique word detection is disabled. 0 = not synchronized. 1 = synchronized REG5 bit 0.

Default configuration at manufacturing:
REG0 = 0x0D
REG1 = 0x20

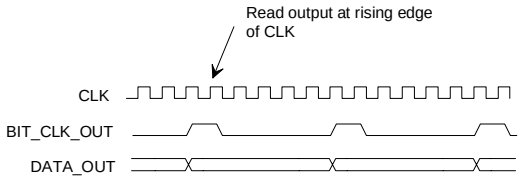
Timing

The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input



Output



Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	**Definition**
TP1	Receiver unique word synchronization. '1' when a unique word is detected with less than 10% bit errors (at least 28 matching bits out of 32).
TP2	Received start of frame, at the decoder output.
TP3	Frame valid signal. '0' when the number of errors exceed the correction capability of the RS decoder.

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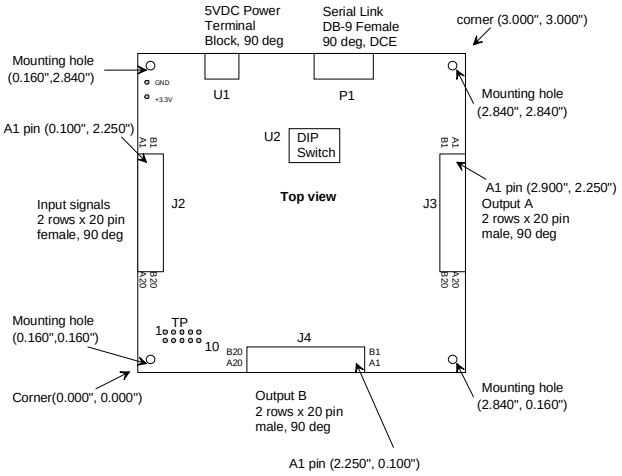
Mechanical Interface

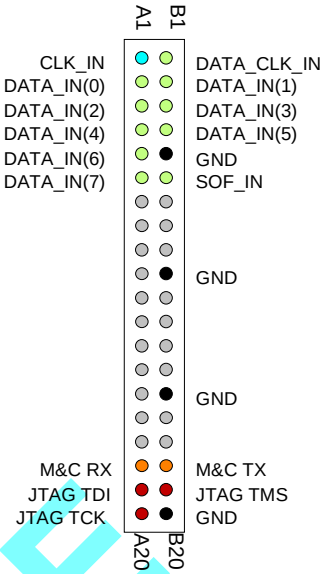


Mounting hole diameter: 0.125"

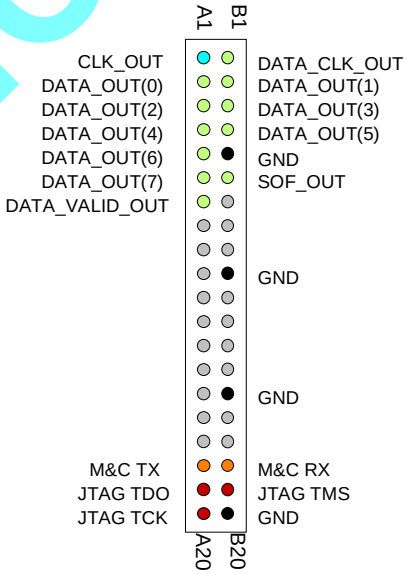
A1 pin height: 0.039"

Maximum height 0.500"

Input Connector J2



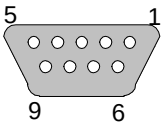
Output Connectors J3, J4



Pinout

Serial Link P1

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



DB-9 Female

2 Transmit
3 Receive
5 Ground

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ComBlock Ordering Information

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