COM-1005
BIT ERROR RATE MEASUREMENT

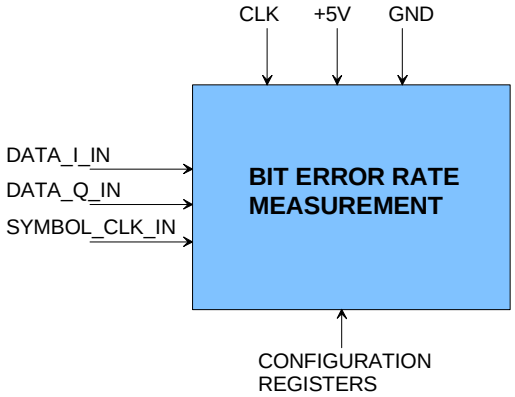
Key Features

- Measures actual bit errors while a known PRBS-11 pseudo-random test sequence is being transmitted.
- Accurate BER measurement downto 10^{-8}.
- Adjustable measurement window from 1,000 bits to 1,000,000,000 bits, to trade off BER range and measurement duration.
- Fast automatic synchronization (n-PSK phase ambiguity removal).
- Cycle slips detection.
- 32-bit cumulative BER counter for long-duration measurements.
- 1 bit serial / 2 bit parallel input selection (I before Q, or I/Q).
- Built-in test pattern generator.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 5V and 3.3V logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1005.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

BER Measurement I/Os



Electrical Interface

Input	Definition
DATA_I_IN	Input data stream, in-phase (real) axis.
DATA_Q_IN	Input data stream, quadrature (imaginary) axis. Unused if BPSK is selected.
SYMBOL_CLK_IN	Input symbol clock. One CLK-wide pulse. Read the input signals at the rising edge of CLK when SYMBOL_CLK_IN = ‘1’.
CLK_IN	Input reference clock for synchronous I/O and processing. Yields internal CLK clock. Maximum frequency $\mathbf{f_{clk}}$ is 40 MHz.

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Output (through mode)	Definition
DATA_I_OUT	Reclocked version of DATA_I_IN
DATA_Q_OUT	Reclocked version of DATA_Q_IN
SYMBOL_CLK_OUT	Reclocked version of SYMBOL_CLK_IN
CLK_OUT	Output reference clock. Same as CLK_IN input clock and CLK internal processing clock. Typically 40 MHz.
Output (test pattern)	**Definition**
DATA_OUT	Bit serial output test pattern. Read at the rising edge of CLK_OUT when SAMPLE_CLK_OUT = '1'.
SAMPLE_CLK_OUT	Output sample clock. One CLK_OUT-wide pulse.
SAMPLE_CLK_OUT_REQ	Optional flow-control input. Requests for samples from the module downstream. Pulled-up.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Configuration

Complete assemblies can be monitored and controlled centrally over a single serial or, when available through adjacent ComBlocks, LAN/TCP-IP, USB 2.0 or CardBus/PCMCIA connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Parameters	Configuration
Input format	0 = 1 bit serial input 1 = 2 bit (I/Q) parallel input REG0 bit 1
Measurement window	Number of bits in the window where errors are counted: 000 = 1,000 001 = 10,000 010 = 100,000 011 = 1,000,000 100 = 10,000,000 101 = 100,000,000 110 = 1,000,000,000 REG0 bits 4-2
Reset cumulative bit error counter	1 = reset the cumulative BER counters every time REG0 is written to. There is no need to clear this bit. 0 = keep the cumulative BER counters running. REG0 bit 5
Pattern generator clock selection	0 = use CLK_IN as external clock reference. '1' = use 40 MHz on-board clock as clock reference. This selection applies only to the built-in pattern generator, not the BER measurement. REG1 bit 0
Internal pattern generation (test mode)	00 = test mode disabled 01 = counting sequence: When set, the baseband input is disabled and a periodic pattern is internally generated at the encoder input. The pattern consists of an 8-bit counter, MSB transmitted first. 10 = PRBS-11. internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream). Useful in measuring BER performances in conjunction with COM-1005. 11 = PRBS-11, alternate output format: read the output bit stream at rising edge of SAMPLE_CLK_OUT (no need to use CLK_OUT) REG1 bits 3-2

Test pattern generator data rate: internal / external selection	The data rate for the built-in test pattern generator can be determined by external modules downstream (for example a modulator)) as part of the flow control mechanism or by an internal Numerically Controlled Oscillator (NCO). 0 = exter nal. Output data rate is based on SAMPLE_CLK_OUT_REQ samples requests from following module. Data is 'pulled out'. 1 = internal. Output data rate is selected internally by the NCO frequency set in REG2/3/4. Sample requests SAMPLE_CLK_OUT_REQ are ignored. Data is 'pushed out'. REG1 bit 4
Output format (NEW)	0 = Input data sent to J3, test pattern sent to J4 1 = Input data sent to J4, test pattern sent to J3 REG1 bit 5
Test pattern generator data rate: internal NCO	Internal generation of the pattern generator bit rate. Ignore this field when the output bit rate is determined by modules downstream. 24-bit unsigned integer expressed as fsymbol rate * 2^{24} / fclk. The internal processing clock fclk is typically 40 MHz. REG2 = bits 7-0 (LSB) REG3 = bits 15 – 8 REG4 = bits 23 – 16 (MSB)

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Monitoring

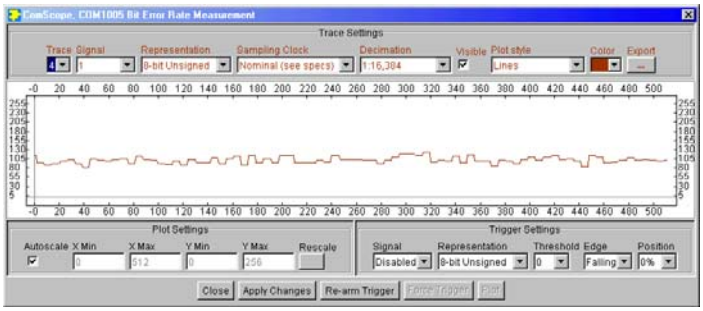
Monitoring registers are read-only.

Parameters	Monitoring
Bit Errors	Number of bit errors in a fixed-length window. 32 bit unsigned. REG1: error_count[7:0] REG2: error_count[15:8] REG3: error_count[23:16] REG4: error_count[31:24] The bit errors counter is updated once every periodic measurement window. Reading the value will not reset the counter.
Synchronization status	0 = not synchronized. 2047-bit pattern is not detected. 1 = synchronized REG5 bit 0.
n-PSK Phase ambiguity. Cycle slip detection.	Number indicating the phase offset between modulated and demodulated data streams. A change in phase offset denotes a cycle slip. The phase offset is expressed as 00 = 0 deg 01 = +90 deg 10 = +180 deg 11 = +270 deg REG5 bit 2-1
Cumulative bit error count	A cumulative bit error counter starts after reset (see REG0 bit 5) and stops as soon as the cumulative bit count reaches 0xFFFFFFFF. The cumulative BER counters are not aligned to the periodic measurement window. REG6 cumulative error count[7:0] REG7: cumulative error count[15:8] REG8: cumulative error count[23:16] REG9: cumulative error count[31:24]
Cumulative bit count	A cumulative bit conter starts after reset (see REG0 bit 5) and stops as soon as the cumulative bit count reaches 0xFFFFFFFF. The cumulative bit counter is not aligned to the periodic measurement window. REG10 cumulative bit count[7:0] REG11: cumulative bit count[15:8] REG12: cumulative bit count[23:16] REG13: cumulative bit count[31:24]

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-1005 signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: DATA_I_IN input	Binary	1 sample /bit	4096
2: Local data stream replica (to be compared with received data stream on Trace3/Signal 1) .	Binary	1 sample /bit	4096
3: Start of PRBS-11 periodic test sequence detected with less than 10% bit errors.	Binary	1 sample /bit	4096
Trace 2 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: DATA_Q_IN input	Binary	1 sample /bit	4096
2: Bit Errors	Binary	1 sample /bit	4096
3: Cycle slips	Binary	1 sample /bit	4096
4: Synchronization	Binary	1 sample /bit	4096
Trace 3 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Received data stream (after QPSK ambiguity removal if needed)	Binary	1 sample /bit	4096
2: Start of PRBS-11 periodic test sequence detected with less than 10% bit errors.	Binary	1 sample /bit	4096
Trace 4 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Bit errors within the specified measurement window 8 Least Significant bits clamped at 255.	8-bit	1 sample /bit	512
2: Bit errors within the specified measurement window Bits 15-8 clamped at 255.	8-bit	1 sample /bit	512
3: Bit errors within the specified measurement window Bits 23-16 clamped at 255.	8-bit	1 sample /bit	512
4: Bit errors within the specified measurement window Bits 31-24	8-bit	1 sample /bit	512
Trigger Signal			**Format**
1: Start of PRBS-11 periodic test sequence detected with less than 10% bit errors			Binary
2: Bit Errors			Binary
3: Cycle slips			Binary
4: Synchronization			Binary



BER plot versus time (ComScope Trace 4)

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock.

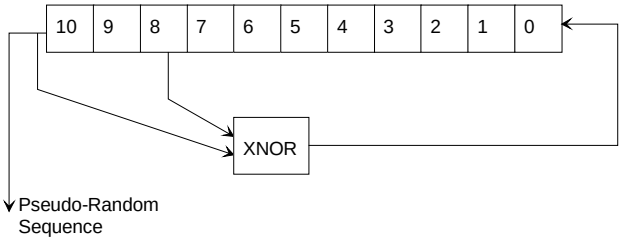
In particular, selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

Operation

PRBS-11 Pseudo-Random Bit Stream

BER measurement is made by counting actual errors in the received bit stream. The received bit stream is compared with a locally generated replica of the reference PRBS-11 sequence.
The reference sequence is a periodic 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:

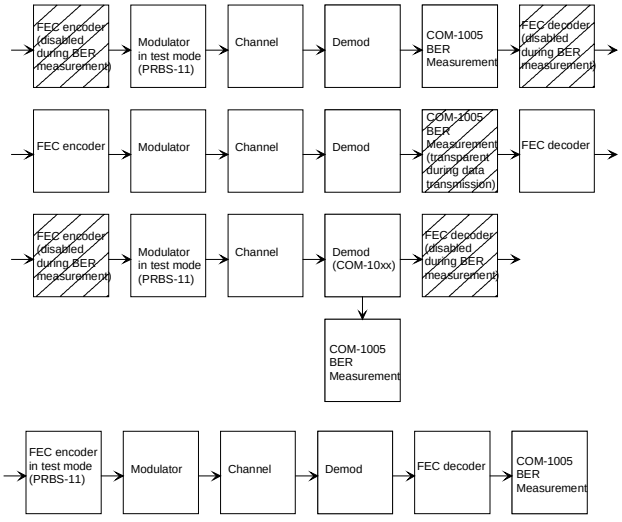


The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100 1100111000 0000010011 1111010001 1110110100 1101001100 0011000001

All ComBlock modulators can be configured in test mode whereby this 2047-bit PN sequence is being transmitted.

Through-Mode

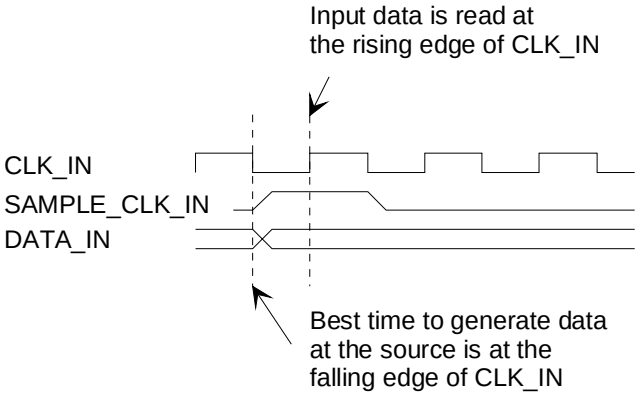
The COM-1005 module can be placed at the end of a transmit-receive chain, or used in a transparent way in the middle of a chain, as illustrated below:



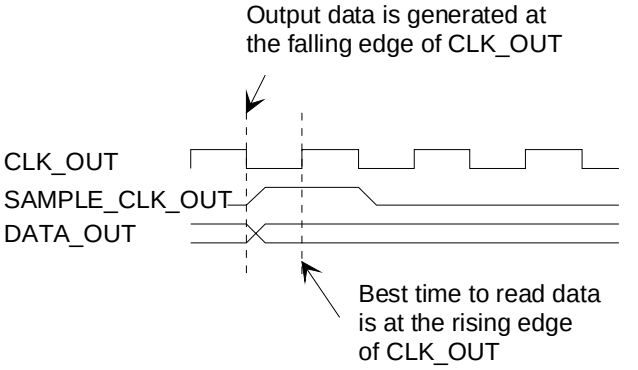
Timing

The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input



Output

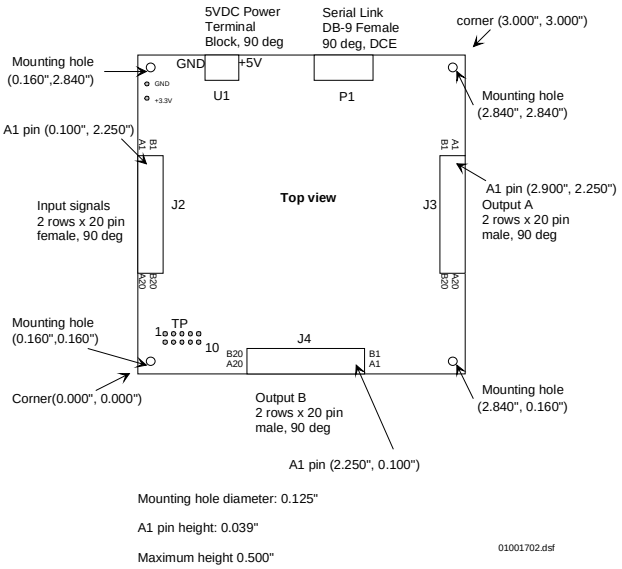


Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	Synchronization
TP2	Cycle slips
TP3	Bit error
TP4	Start of PRBS-11 periodic test sequence detected with less than 10% bit errors.
TP5	Received data stream (after QPSK ambiguity removal if needed)
TP6	Local data stream replica (to be compared with received data stream on TP5)
TP7	Reset command was received to re-initialize the cumulative BER counters

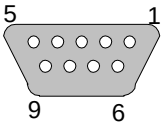
Mechanical Interface



Pinout

Serial Link P1

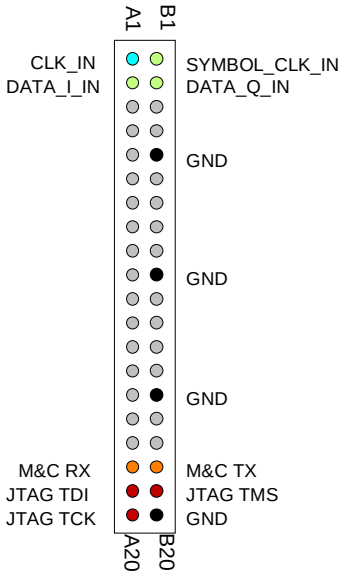
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



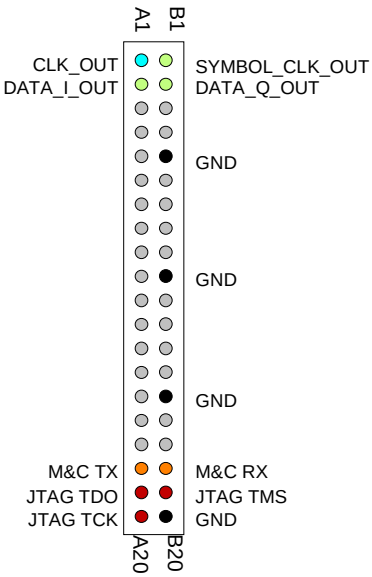
DB-9 Female

2 Transmit
3 Receive
5 Ground

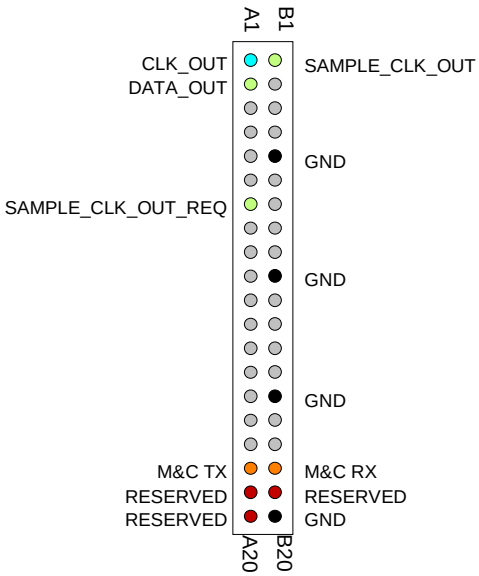
Input Connector J2



Output Connectors J3 / J4



Trough-mode output



Test pattern output

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1001 BPSK/QPSK/OQPSK demodulator	Most Comblocks with bit serial interface
COM-1418 DS spread-spectrum demodulator	COM-5003 TCP-IP / USB Gateway
COM-1027 FSK/MSK/GFSK/GMSK demodulator	
COM-7002 Turbo Code Error correction decoder	
COM-1023 BER generator	

Configuration Management

This specification is to be used in conjunction with VHDL software revision 15.

ComBlock Ordering Information

COM-1005 BIT ERROR RATE MEASUREMENT

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