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TDRSS Narrow-band Simulator and Test System

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Abstract— **Introducing new communication equipment or system to the Tracking and Data Relay Satellite System (TDRSS) ground segment is a complicated process that involves a lengthy development and test cycle. Complexity arises due to the presence of the variety of signaling formats, operation and user constraints, monitor and control parameters, and the requirement to ensure the new piece of ground equipment or system meets the functional and performance requirements for all different combinations of system configuration parameters and operational scenarios. The development cycle starts with extensive software simulations to establish the performance parameters of the new equipment or system followed by a prototyping stage. The prototype system undergoes a battery of tests in a laboratory environment to verify that it is capable of meeting the performance levels derived from the software simulations. Testing must be performed using simulated signals generated either using software or hardware. The current practice is to use a chain of test equipment, each piece in the chain dedicated to a single function. This requires manual setup between different test configurations and test reporting is also handled manually. This is costly both in terms of test hardware investment and the manpower involved. The options available to reduce the cost are to use either a software or hardware simulator that can combine multiple functions in a single unit. Software simulation involves generating signal files that can be played back repeatedly. Depending on the data rate being simulated, each test file can occupy several Terabytes (TBs); in addition, it requires a playback system which tends to be relatively expensive to acquire and maintain. On the other hand, with more advanced signal processing technology the hardware simulation can be achieved with low cost Field Programmable Gate Array (FPGA). A low cost hardware simulator that can support data rates up to 25 Mbps is selected for the simulation system. The simulator supports baseband digital data formats and different modulation and coding schemes used in the TDRSS. Channel impairments applicable for communicating with orbiting platforms and signal impairments generated by the TDRSS itself are also simulated by the system; these include stressing profiles of delay, Doppler, and multipath. Hardware distortions of customer platforms are simulated by a set of software defined distortion filters designed according to the user constraints specified in the Space Network user's guide. In order to reduce the time spent during the prototype testing phase, an automated test system is being developed. Simulator architecture and the test automation approach will be presented.**

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1. INTRODUCTION

The National Aeronautics and Space Administration (NASA) Tracking and Data Relay Satellite (TDRS) System (TDRSS) is a satellite communications system designed to relay command, telemetry, and science data between on-orbit customer spacecraft and the ground. The global TDRS fleet currently consists of three first-generation, three second-generation, and two third generation satellites supported by four tracking stations, two at White Sands, New Mexico, one on the Pacific island of Guam, and the fourth one at Blossom Point, Maryland. The first generation satellites were launched between 1982 and 1995 and the deployment of the third-generation satellites started in 2013. This combination of nine geosynchronous satellites and the four ground stations comprise NASA's Space Network (SN). TDRSS customers currently include low earth orbiting scientific satellites, the International Space Station (ISS), expendable launch vehicles, balloons carrying scientific payloads, aircrafts, and remote terrestrial systems. The SN satellite fleet and the ground stations are illustrated in Figure 1.

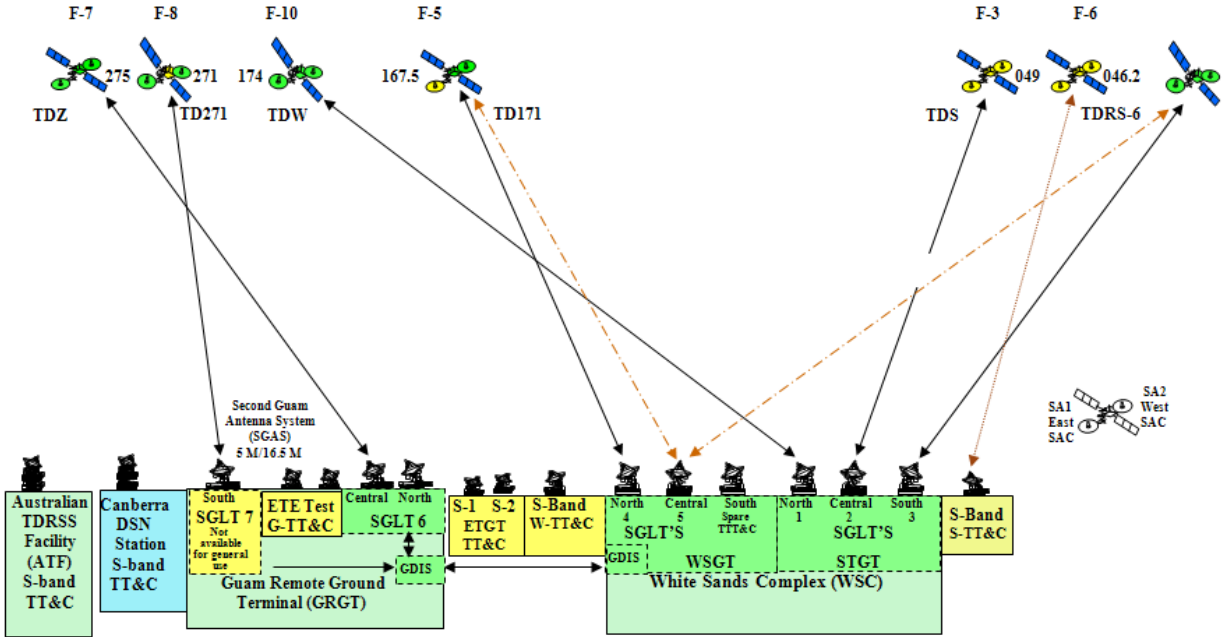

Figure 1 Space Network Elements

Introducing new communication hardware to the TDRSS ground segment is a complicated process that involves a lengthy development and test cycle, which can last several years. Complexity arises due to the presence of a large number of signaling formats and user constraints [1], monitor and control parameters, and the requirement to ensure that all different combinations of these parameters are met by a new piece of ground system hardware [2]. In this context ways of reducing the lifecycle cost of ground hardware is being sought. As part of this effort, acquisition and testing new ground receivers using a simulator that lends to cheaper and faster development cycle is considered in this paper. The proposed approach takes advantage processing power of low cost hardware along with concepts of software defined radio and automated testing. Simulator architecture, monitor and control system, and the test automation approach are discussed.

2. BACKGROUND

The SN ground terminals consists of customized communication hardware that are expensive to procure, sustain, operate, and to modify. As such, a refresh cycle of ground systems tends to be rather lengthy, counted in decades. The last significant work on the SN ground terminals was completed in 1994 and the ongoing ground terminal upgrade is not expected to complete before 2017 [3]. Over the life time of a refresh cycle significant technological advances can occur and it is rather expensive to introduce new technologies without posing a substantial risk to service reliability.

The development cycle starts with extensive software simulations to establish the performance parameters of the new system followed by a prototyping stage. The prototype system undergoes a battery of tests in a laboratory environment to verify that it is capable of meeting the performance levels derived from the software simulations. Testing must be performed using simulated signals generated either using software or hardware. Figure 2 shows the receiver testing setup used in the hardware maintenance depot (HMD) at the White Sands Complex (WSC). The test setup include performance test equipment (PTE) modem,

noise generator, bit error rate test sets (BERTS), automated data processing equipment (ADPE) that simulates the ground system receiver controller at the TDRSS ground station, and a highly stable frequency reference. It is essentially a static test which does not take into account of either the user spacecraft dynamics or the signal distortions caused by the user spacecraft and the TDRSS channel. A second type of testing that includes the TDRSS channel, known as end-to-end testing, is also conducted. It involves dedicated ground equipment including a separate end-to-end test antenna and associated radio frequency (RF) equipment. End-to-end testing requires scheduling of satellite time, which can severely limit the test duration and scope. Similar to the HMD test, the end-to-end test does not account for spacecraft dynamics or signal distortions introduced by the user transmitter.

Both types of testing mentioned above requires manual setup between different test configurations and test reporting is also handled manually. This is costly both in terms of test hardware investment and the manpower involved. The options available to reduce the cost are to use either a software or hardware simulator that can combine multiple functions in a single unit. Software simulation involves generating data files that can be played back repeatedly. Depending on the data rate being simulated, each test file can occupy several TBs; in addition, it requires a playback system which tends to be relatively expensive to acquire and maintain. On the other hand, hardware simulation can be achieved at a much lower cost using field programmable gate array (FPGA) technology. A low cost hardware platform that can support data rates up to 25 Mbps is selected for the simulation system. The simulator supports baseband digital data formats and different modulation and coding schemes used in the TDRSS return service. Hardware distortions of customer platforms are simulated by a set of software defined distortion filters generated according to the user constraints specified in the Space Network User's Guide. Signal impairments applicable for communicating with orbiting platforms and impairments generated by the TDRSS channel itself are simulated by the system; these include stressing profiles of delay, Doppler, and multipath.

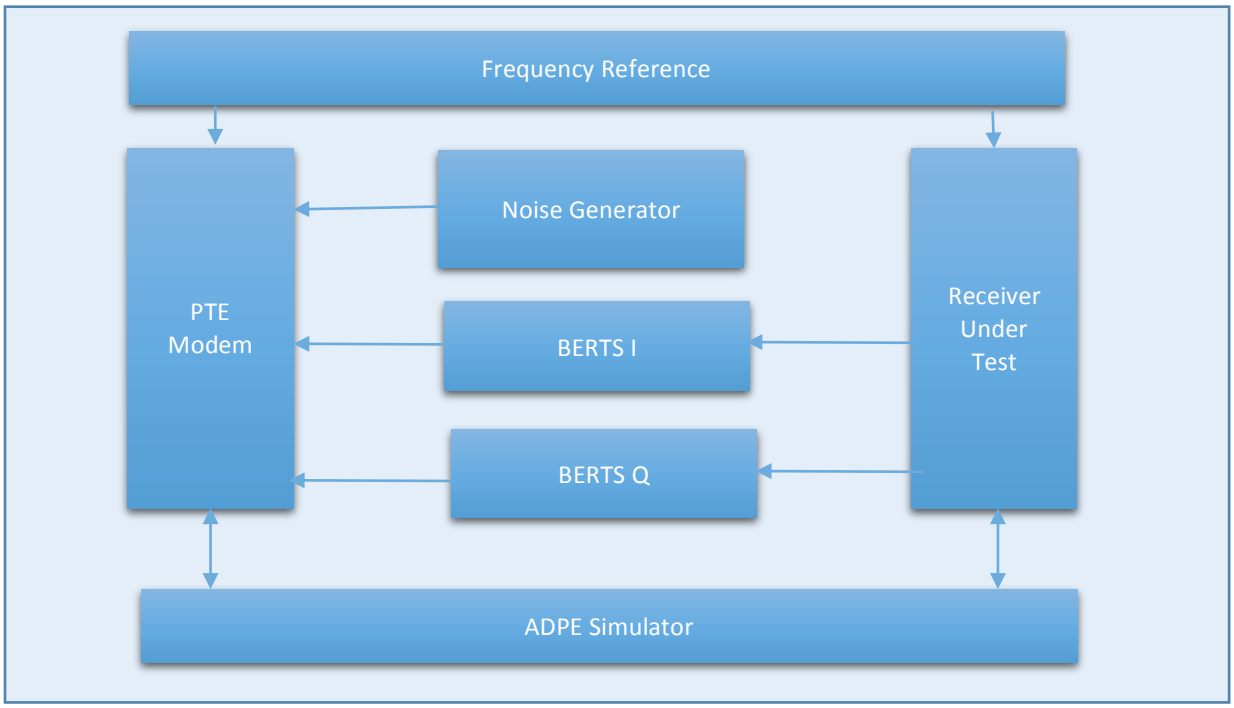

Figure 2 Standard Test Setup used for Receiver Testing at WSC

The following section describes the approach taken in developing a narrow-band simulator and test system. The discussion is descriptive in nature and does not contain analytical details of the simulation process, which can be found in standard communication texts and journal publications.

3. Overview

The basic requirements of the simulator and the test system are:

- Simulate user of platform transmitter
- Simulate TDRSS channel
- Monitor and control
- Test automation

Figure 2 shows the key components of the test setup. The frequency reference is a high fidelity system that is external to the simulator/test system considered in this paper. The simulator is required to generate real time samples packaged in one of the standard packet format, which are sent to the receiver under test. The simulator imparts expected signal distortions attributed to the user platform and the RF channel between the user platform and the receiver at the WSC ground terminal. The simulator and the test receiver are controlled by the monitor and control (M&C) system. The M&C also performs various test functions such as bit error rate (BER) and error vector magnitude (EVM) measurements, and allow for test automation. The SN identifies a number of user platform parameters, which must be constrained according to the specifications given in Ref 1. These parameters, known as user constraints, have values specific to each type of TDRSS return service. User constraints impact bit error performance, acquisition time, and tracking performance. TDRSS return service receivers must accommodate the user transmitter imperfections along with the TDRSS imperfections within a specified amount of implementation loss. The simulator being developed attempts to provide the expected amount of signal degradation due to both types of imperfections.

Table 1 lists the user constraints and channel distortions that have an impact on carrier tracking and BER performance. They are grouped into three categories; transmitter phase distortions, transmitter amplitude distortions, and channel distortions including those due to TDRSS. The user constraints listed are only for suppressed carrier modulation types; those related to residual carrier modulation types are not considered for the current implementation.

The simulator attempts to reproduce most of the distortions in a way that allows observation of the overall impact on system performance. To simulate individual parameters in the phase and amplitude groups in hardware is complex and involves time intensive calculations, which defeats the purpose of the need to operate in real time. Instead, the hardware part of the simulator receives phase and amplitude distortions in the form of probability distribution functions, which can be used to generate time samples without incurring a significant computation time. The probability distribution of the combined effect in each category is generated by the M&C system. Each parameter in the phase and amplitude categories in Table 1 is modelled analytically [4,5,6] and Monte Carlo simulation is used to generate the combined probability distribution of phase and amplitude. The channel parameters listed in Table 1 are simulated individually in the hardware section of the simulator.

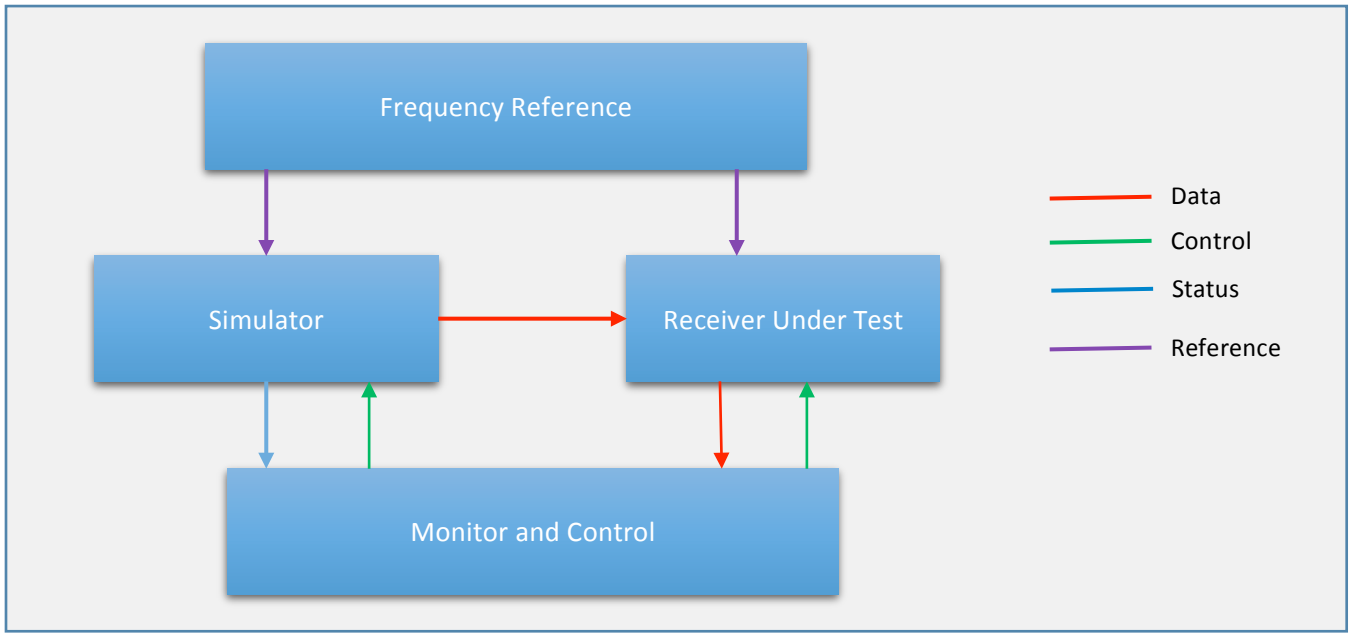

Figure 3 Simulator and Test System

Table 1 User constraints and channel impairments

Parameter Group	Parameter	Comments
Phase	Phase imbalance	Deviation from the reference phase, modelled as a fixed value.
	AM/PM	Caused by amplifier non-linearity; phase degradation is a function of signal amplitude.
	Gain imbalance	Ratio of the actual Q/I power ratio to the ideal Q/I ratio.
	Data transitions induced PM	Modelled as random component of phase imbalance.
	Spurious PM	Unwanted phase modulation due to spikes in phase noise spectrum.
	Coherent phase noise	Unwanted phase modulation due to continuous part of the phase noise spectrum.
Amplitude	Data asymmetry	Modulator spends more time in one amplitude state than the other. Amplitude degradation is proportional to the amount of asymmetry and the nominal amplitude.
	Data jitter	Random component of data asymmetry.
	Data transition	Time required to switch from 90% of the initial data state to 90% of the final data state. Modelled as a fixed reduction in amplitude.
	Incidental AM	Modulation index of sinusoidal amplitude modulation on the data causes a reduction in power available for data detection.
	PN asymmetry	Similar to data asymmetry given above.
	PN jitter	Random component of PN asymmetry.
	Spurious output	Sum powers in all spurs within the specified bandwidth.
Channel	Spacecraft velocity	Sets maximum Doppler frequency
	Spacecraft acceleration	Sets maximum Doppler frequency rate of change
	Spacecraft Jerk	Sets maximum 2^{nd} time derivative of Doppler frequency
	TDRSS	Some of the TDRSS spacecraft and ground system distortions are modelled in terms of a FIR filter.
	AWGN	Additive white Gaussian noise
	Multipath	Dominant multipath reflection added as a delayed and attenuated signal replica.

4. SIMULATOR

Figure 3 shows a functional block diagram of the narrow-band simulator. The simulator ingests external user data via a TCP/IP interface and outputs the modulated samples in the form of UDP/IP packets using either SDDS or VITA 49 format for transporting digitized signal data. It can also generate internal PBRS data in lieu of external data and the internally generated data is used for BER measurements. Data received from the external source are first stored in an elastic buffer to smooth out packet arrival rate variations. The output is a packet stream containing I and Q samples of modulated data including distortions due to user transmitter and TDRSS channel. The output packet rate is determined by the data rate selected for the simulation. The simulator requires a stable external frequency reference to ensure that

distortions induced by the reference source stay well below those generated by the simulator. The same reference source can be used with the test receiver to perform tests that require coherency and time synchronization.

The input data get processed by the following functional blocks prior to appearing at the output:

- Framing and FEC
- Data formatting and shaping
- Modulator
- Phase distortions
- Amplitude distortions
- Channel filter
- AWGN

These processing blocks can be turned on and off individually to suit test conditions.

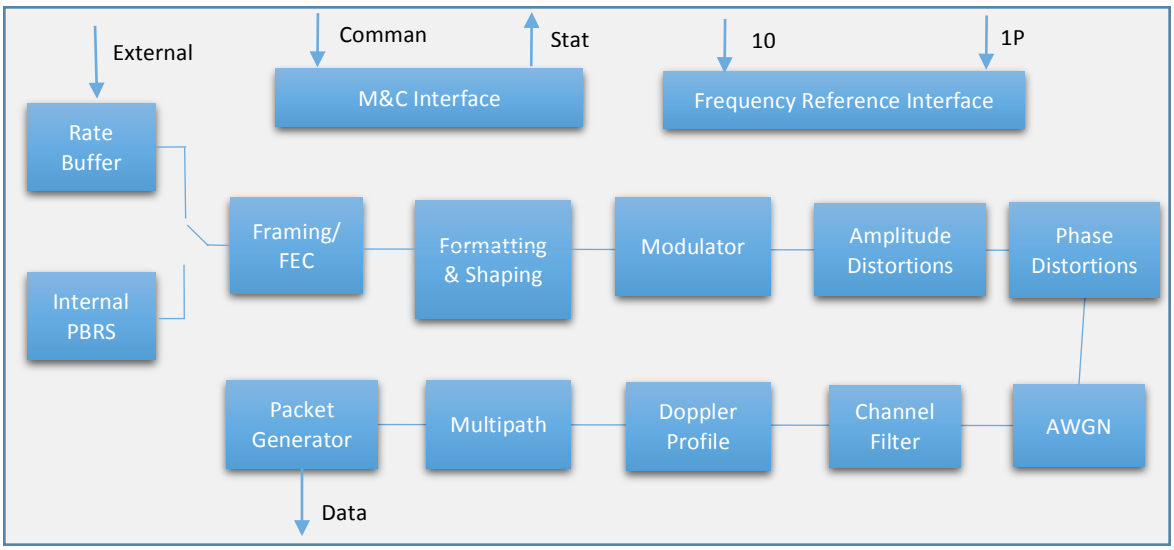

Figure 4 Simulator Block Diagram

Framing and FEC
Framing and FEC block add CCSDS sync markers and FEC parity bits. The following FEC types are supported:

- Convolutional (rates ½ and 1/3)
- Reed-Solomon
- Concatenated RS and Convolutional
- LDPC (rates ½ and 7/8)

Formatting and Pulse shaping
NRZ-L, M, S data formatting and pulse shaping are performed by this block. Pulse shaping includes root raised cosine with roll-off: 20%, 25%, 35%, and 40%.

Modulator
The modulator block supports the following modulation types:

- Spread spectrum: BPSK, SQPN
- Non-spread spectrum: BPSK, QPSK, OQPSK, 8 PSK

Data rates for spread spectrum modulation ranges from: 1 kbps to 300 kps, and those for non-spread modulations range from 1 kbps to 22 Mbps.

Amplitude Distortions
Deterministic and random components of amplitude distortions are generated using tabular data provided by the M&C system. For the random component, a cumulative distribution function is used. The distribution provided is combined with a random number generator to create the random samples.

Phase distortions
Deterministic and random components of phase distortions are generated using tabular data provided by the M&C system. For the random component, a cumulative distribution function is used. The distribution provided is combined with a random number generator to create the random samples.

AWGN
The AWGN block accounts for the noise introduced by TDRS as well as the ground receiving system.

Channel filter
The channel filter is a band bandpass filter that can be customized to replicate spectrum truncation and distortion produced by the analog portion of the spacecraft RF hardware. An FIR filter is used for the simulation. Filter coefficients are provided by the M&C system.

Doppler
Doppler profile, provided in terms time series samples by the M&C system, is used to simulate real world Doppler and Doppler rates experienced by the RF link. In addition, fixed and slowly varying frequency offsets in the transmitter can be modelled.

Multipath
The multipath block simulates a dominant multipath component arising from earth surface reflections. A suitably

attenuated and delayed replica of the modulated signal is used to create a single multipath interferer.

In addition to the distorted I/Q samples, the simulator generates error vector magnitude samples by taking the difference between the output I/Q samples and the ideal I/Q samples generated by the modulator.

The output I/Q samples, quantized to 16 levels, are sent via a dedicated 1 GbE interface. A second 1 GbE interface is used for data input, monitor and control, and error vector data.

5. Monitor and Control

The monitor and control (M&C) system provides the user interface, analytical engine, and test measurements. One of the key design goals of the M&C is to minimize the amount of time required to setup and perform receiver testing. Figure 5 shows the M&C functional architecture of the M&C system, which is based on a standard work station using Windows operating system. The main functional elements of the system are:

- User interface
- Constraint analysis
- Vehicle dynamics
- Simulator interface
- Test data generator
- Configuration
- Frame sync
- BER measurement
- EVM measurement

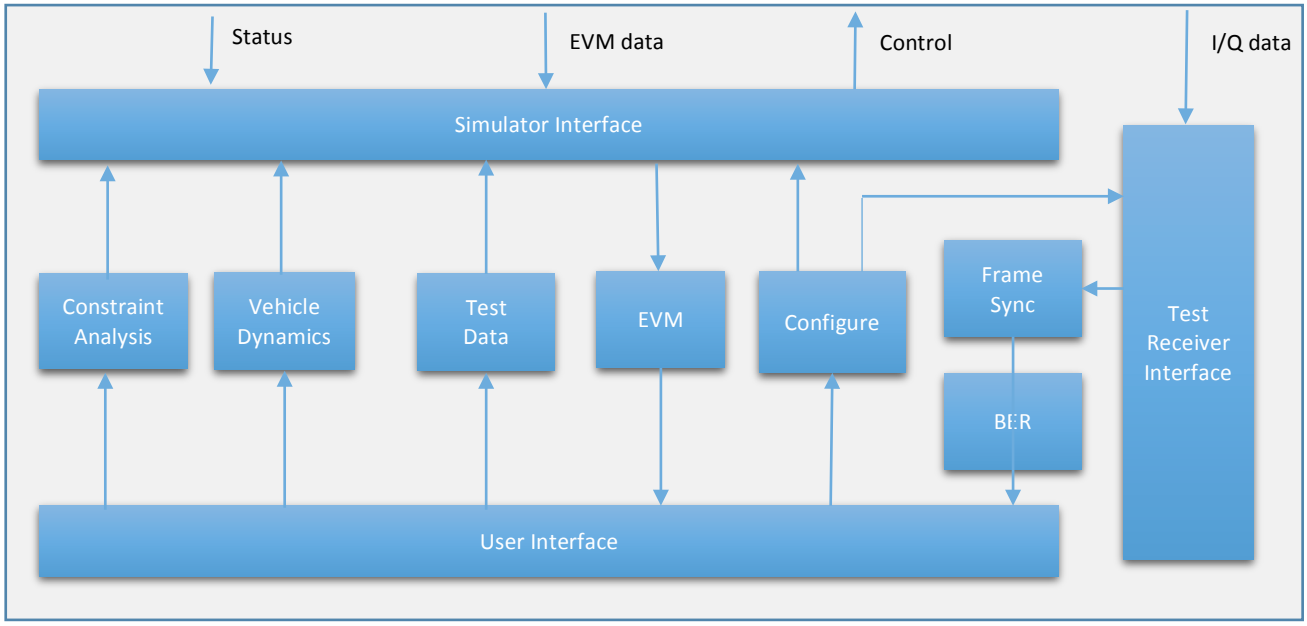

Figure 5 M&C Architecture

User Interface
Two separate graphical user interfaces are provided for setting up the simulator and generating test scripts. GUI for the simulator allows for selecting data rate, IF frequency, modulation, coding, various user constraint parameters, and simulation duration. Feedback from the simulator on successful setup, Doppler and delay profile time series, and EVM plots are available from the GUI. The scripting interface allows selection of the required test and the parameter ranges and step sizes over which the test must be performed. Status of the test currently in progress is available from the GUI.

Simulator interface
The simulator interface is a 1 GbE interface that allows passing control parameters and receiving status and time series samples of the error vector. In additions this interface is used to load the FPGA firmware in terms of multiple personalities to simulate different modulation and coding schemes.

Configuration
The configuration block allows configuration of the simulator as well as the test receiver. Simulator configuration driver is native to the M&C system. An external driver is required to configure the test receiver, and depends on the particular command syntax used for the receiver.

Constraint Analysis
The constraint analysis block performs Monte Carlo simulations to generate probability distribution functions for the random components of amplitude and phase degradations. After setting the user constraint parameters, the number of samples for the simulation or a convergence

criteria can be selected to ensure a stable distribution has been generated by the simulation. In addition to Monte Carlo simulations, filter synthesis to simulate the required channel filter characteristics are handled by this block.

Vehicle dynamics
Vehicle dynamics can be generated using a built in orbit generator or provided through an external file. The internal orbit generator requires either two line elements or standard Keplerian elements of the user vehicle. In order to test extreme cases of vehicle dynamics a sinusoidal model is also provided. With the sinusoidal model, the maximum specified values of Doppler and Doppler rate can be simulated.

Frame sync and BER
The frame sync block provide frame synchronization of incoming data from the test receiver. The BER block performs error checking of each frame including errors in the ASM. BER is performed using a preassigned PBRS sequence. A running count of the BER and the frame errors are displayed in the GUI.

Test Data
Test data generation can be generated using files stored in the work station (e.g. multimedia files) or in terms of PBRS to support BER measurements. The data rate is controlled by the built in throttling feature of TCP/IP.

EVM
Error vector data from the simulator are processed to generate the standard EVM measurement parameters and plots. These include: EVM average, EVM standard deviation, constellation, EVM vs time, error phase vs time, error spectrum, and frequency response.

6. TEST AUTOMATION

The main objectives of test automation are to improve test repeatability, reducing test time, increasing measurement accuracy, and lowering the cost of report generation and troubleshooting. The M&C system is designed to meet these objectives, while providing a friendly user interface to setup and monitor test activities.

Test automation uses XML to develop test scripts and MySQL database to store various forms of test data. Test scripts written in XML can be created relatively easily and the results generated from a test are saved on the database for easy retrieval and processing. Figure 5 shows a typical flow diagram of automated testing. At the end of each test a test report is generated which describes the test procedure, test parameters used, and the appropriate plots depicting results obtained. In addition, the specification of the test and how far the measurement deviated from the specification are also reported. In the event of a test failure adequate diagnostic information is provided to enable troubleshooting the test configuration.

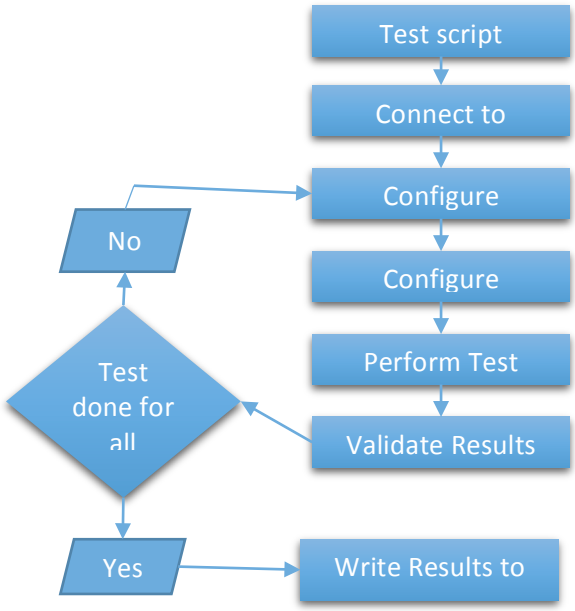

Figure 6 General flow diagram for test automation

Presently only non-coherent return services can be simulated and tested. Coordination between the modulator (simulator) and the test receiver that is necessary to simulate coherent services is not supported by the M&C. However, the functionality required to configure test receivers via receiver specific driver software is supported. Capability to perform the following tests are supported:

- Acquisition time
- PN tracking
- One-way Doppler
- BER
- EVM

Details of each test case including test objectives, test procedure, parameter list, required outputs and their formats are stored in the database. Additional test cases can be created by following a recipe that defines each stage of the test scenarios.

7. SUMMARY

The simulator and test system has the potential to accelerate the development of narrow-band receivers utilized in the TDRSS while providing significant cost benefits to the SN project.

The simulator uses a low-cost FPGA platform that can be replicated easily at various test locations and provides a means of conducting standardized testing. User constraints are simulated in a realistic manner without over stressing the hardware when supporting data rates as high as 22 Mbps. The simulator can assume multiple personalities that can be uploaded easily from the M&C system. Different personalities can represent unique combinations of functional blocks representing TDRSS services. The system can be upgraded easily to accommodate new modulation/coding schemes through firmware change.

The PC based monitor and control system provides the user interface, analytical engine, test measurements, and test automation capability. The analytical engine is key to modelling the various user constraints in terms of amplitude and phase degradations. BER testing can be performed relatively easily without dedicated test hardware. The EVM measurement facility can be used to characterize the user constraints in a simplified way. Test automation helps eliminate much of the manual processes involved in the current test practices.

For the SN the cost savings come from the use of low-cost hardware and reduced effort to achieving test objectives through automation. The test system allows testing of new receiver designs as well as troubleshooting problems in existing designs. Low cost hardware allows replicating the system across multiple locations such as ground station sites and test labs. The overall architecture provides many options for a low-cost, highly scalable, and highly automated test system. It also provides excellent flexibility in configuring the simulation blocks in various ways to support investigating advanced concepts and new technologies.

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BIOGRAPHY

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