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Low-cost Receiver Development for TDRSS DAS Sustainment and CubeSat Applications

Keith Hogie
 Computer Sciences Corporation
 12401 Mount Pleasant Dr.
 Laurel, MD 20708
 301-286-3685
 Keith.Hogie@nasa.gov

Bruce Flanders
 Harris Corporation
 7855 Walker Drive
 Greenbelt, MD 20770
 301-823-2667
 Bruce.Flanders@harris.com

Daniel Paulson
 Harris Corporation
 7855 Walker Drive
 Greenbelt, MD 20770
 301-286-3164
 Daniel.A.Paulson@nasa.gov

Alain Zarembowitch
 Mobile Satellite Services
 845-N Quince Orchard Blvd
 Gaithersburg, MD 20878-1676
 240-631-1111
 info@comblock.com

Haleh Safavi
 NASA/GSFC
 8800 Greenbelt Road
 Greenbelt, MD 20771
 301-284-5610
 Haleh.Safavi@nasa.gov

Jeffry Lubelczyk
 NASA/GSFC
 8800 Greenbelt Road
 Greenbelt, MD 20771
 301-286-0994
 Jeffrey.T.Lubelczyk@nasa.gov

Abstract—Tracking and Data Relay Satellite System (TDRSS) Demand Access System (DAS) sustainment is aimed at modernizing the existing DAS using low-cost hardware components as well as a more robust monitor and control architecture. A key part of the system is the DAS receiver, which supports the Pseudo Noise (PN) modulation waveforms of the TDRSS. The receiver in the current DAS system is a custom design that has been increasingly difficult to maintain, due to hardware obsolescence and a lack of sufficient inventory of spare units. In addition, the receivers suffer from performance issues, which tend to limit the customer base subscribing to the DAS service. The DAS sustainment effort attempts to rectify the performance shortfall of the current receiver and address hardware obsolescence by making software portability a key design goal. As part of the DAS sustainment effort, two low-cost receivers were developed: one of them based on a commercial spread-spectrum receiver implemented on a Field Programmable Gate Array (FPGA), and the other a Software Defined Radio (SDR) implemented on a server class computer. The two receiver prototypes underwent extensive testing in a laboratory environment as well as on-air testing with orbiting customers. Receiver design details and test results are presented. The potential usages of such TDRSS compatible, low cost and small footprint of receivers in CubeSat are discussed.

that can provide continual coverage of any mission in low-earth orbit. The entire Space Network (SN) system consists of 9 spacecraft located in three oceanic regions around the earth. NASA’s White Sands Complex (WSC) provides the ground communication support for TDRSs located over the Atlantic and Pacific Oceans. Another TDRSS ground station in Guam supports the TDRS’s over the Indian Ocean. The TDRSS can provide continuous coverage of satellites in low-earth orbit from one or more TDRSs as shown in figure 1. The system also provides communication for lower altitude vehicles such as balloon missions as well as launch and early orbit support.

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1. INTRODUCTION

NASA’s TDRSS [1] [2] provides multiple geosynchronous communication relay satellites located around the equator
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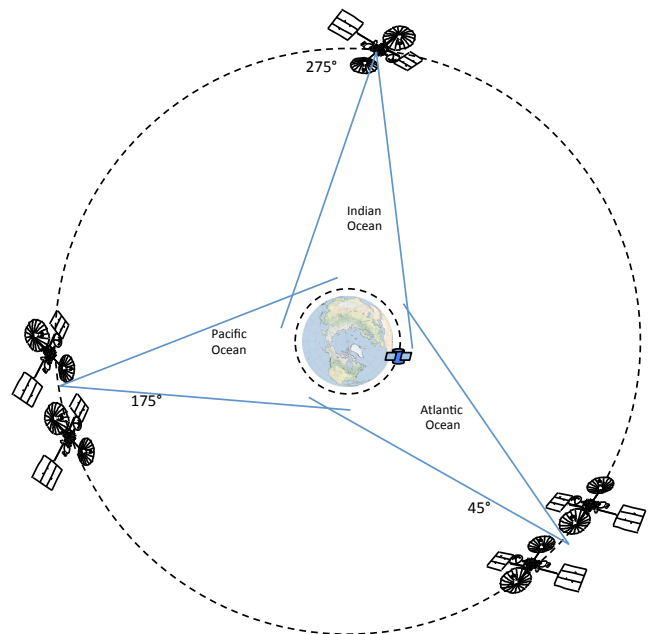


Figure 1 – Continual TDRS MA view capability

Each TDRS has multiple antennas as shown in figure 2. There are two single access (SA) antennas on each TDRS that are steerable to point and track satellites and provide high-rate communication. In the center of the spacecraft, shown in figure 2, there is an array of 30 helical antenna

elements that form a multiple access (MA) system. The 30 elements form a phased array antenna and signals from all 30 elements can be delayed and combined to form beams and track spacecraft. In the case of the first and third generation TDRSS, all 30 antenna signals are sent to the ground and there is a beamformer systems at the WSC ground station that can be commanded to form multiple beams based on orbital information for each spacecraft to be tracked.

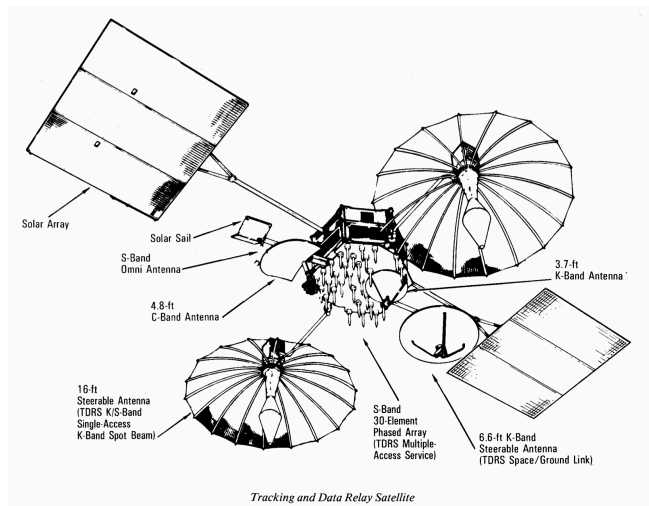


Figure 2 – TDRS spacecraft antennas

The SA antennas can provide high-rate communication but since there are only two per TDRS, they are a very limited resource. The MA antennas can provide many simultaneous communication links at data rates up to 300 Kbps. Since the MA antennas on each TDRS can support multiple spacecraft, they provide a capability for many spacecraft to have continual communication with their control centers. This is very useful for providing continual, low-rate telemetry monitoring and also for missions looking for intermittent events such as gamma ray bursts. When a satellite detects a gamma ray burst, the goal is to immediately get pointing information down to its control center so it can be relayed to other spacecraft and ground observing facilities. Then those systems can then aim their detectors to monitor the event. This requires a continual communication link from a user spacecraft to its control center.

The current TDRSS DAS Sustainment (DAS-S) activity is prototyping new receiver and frame synchronization components to investigate options for augmenting the current system with very low-cost replacement components. The DAS Sustainment activity is also examining ways to utilize these low-cost components to develop a new, highly automated DAS system capable of supporting more users. The initial focus is on the prototype and demonstration activities to verify that the new, low-cost components can support the critical DAS data processing functions for beamforming, demodulation, and frame synchronization. No deployment will be considered until the basic

components have been successfully demonstrated using live signals from an SN customer’s orbiting spacecraft.

2. NEW ARCHITECTURE COMPONENTS

A digital IF system was recently installed at the SN ground stations that digitizes IF signals at the base of the ground antenna and then distributes the digitized IF signals over 10 Gbps fiber optic Ethernet links using UDP/IP multicast. One part of this system includes new digital beamformers that can support up to 32 simultaneous beams each with a minimum of 3 beamformers at each TDRSS ground site. These beamformers provide greatly increased communication resources and can simultaneously track enough spacecraft to provide continual low-rate telemetry to current DAS customers with capacity for many more. The current DAS system only has 16 beamformers and receivers and they are all very old and cannot be expanded.

The current DAS Sustainment activity is analyzing options for adding very low-cost receivers and frame synchronizers to these new beamformers to provide a complete system for supporting continual communication between spacecraft and control centers. With greatly increased communication resources, it will be possible to provide automated communication and continual coverage for a larger SN customer base. This could result in greatly reduced need for missions to submit schedule requests, provide increased coverage, support automated operation, and lower overall operation costs for the SN and users.

The new architecture makes extensive use of digitized signals and Ethernet networking instead of RF cabling, IF switches, and serial links. This allows implementing the new system using commercial-off-the-shelf modern hardware, modern operating systems, and low-cost, high-speed network equipment.

The following sections provide details of the beamformers and the receivers being investigated for an augmented DAS system. These components are the foundation on which a low-cost, highly automated DAS system can be built.

Digital Beamformer

The digital beamformers are FPGA based devices that receive digitized IF signals for all 30 MA antennas on a TDRS and combine them to form up to 32 simultaneous beams tracking separate spacecraft. The digitized IF stream from each MA antenna consists of 210 Mbps of digitized samples. Each beamformer receives all 30 antenna streams in over 6 Gbps of data. The beamformer uses two-line element (TLE) orbital data to determine the location of the TDRS and user satellite, applies weights, and forms receive beams on satellites. The resulting digitized IF samples for the beam are output in time-stamped UDP multicast packets for ingest by one or more digital receivers.

The use of digitized data in IP multicast packets from the antenna, to the beamformer, and on to the receiver eliminates all the current waveguides, IF switches, coax cables, serial cables, and serial switches to connect devices. All digitized data is distributed using standard commercial-off-the-shelf network equipment. This provides much simpler interconnection, automated switching, and eliminates any signal loss or distortion that can occur over copper cables.

In operation, the each beamformer continually receives all 30 MA signal streams from the TDRS it is supporting. They also receive updated TDRS orbital information in TLEs on a daily basis. Forming a beam requires sending the beamformer both the TDRS and user spacecraft TLEs so the beamformer can properly track the user spacecraft. This information needs to be updated every few days due to orbital decay and spacecraft maneuvers.

The beamformer output uses the signal data distribution standard (SDDS) packet format with digitized IF

information transmitted over Ethernet using UDP/IP multicast packets. Using multicast packets simplifies connecting streams from the beamformer to receivers. Commanding a receiver to join a multicast group address results in the network switches automatically sending the proper data to the receiver. It also allows multiple receivers to receive the same data stream. The ability to have multiple receivers process identical digitized IF samples has been used extensively in testing. Tests can directly compare the performance of various versions of receiver firmware and software. It also allows direct comparison between different types of receivers.

The digitizer feeding the beamformers supports multiple TDRSS signals and performs analog to digital (A/D) conversion at different rates and sample sizes for the TDRS signals. For the MA system, the signal is sampled at 6.25 mega-samples per second (MS/s) with 16-bit I and 16-bit Q values per sample. This results in a total of 256 I/Q samples per SDDS packet.

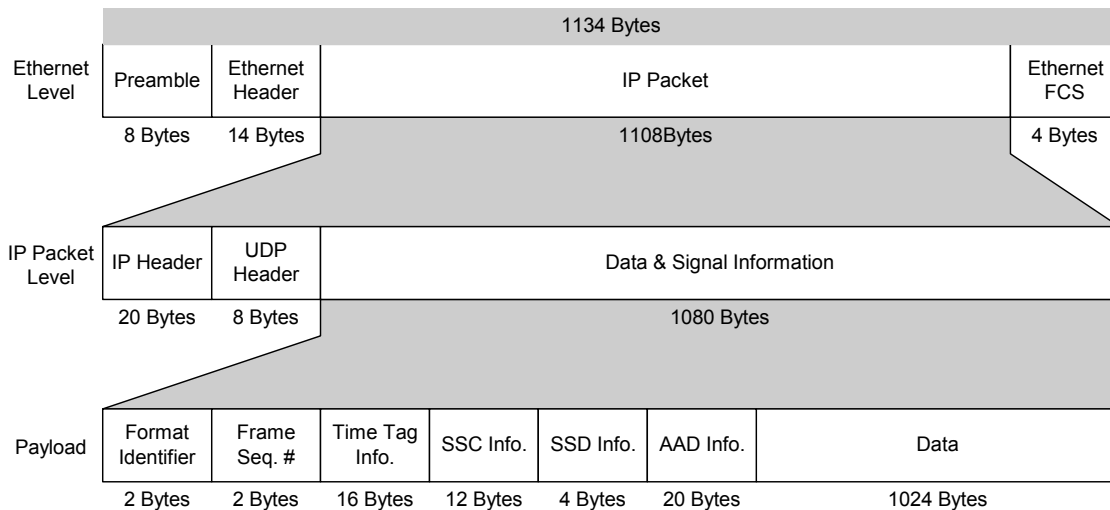


Figure 3 – SDDS Packet Format

New hardware and software receivers

Once a beamformer has produced a beam that contains the desired digitized IF signal, the signal must be processed by a receiver to synchronize with and track the spread spectrum signal, demodulate it, and output the resulting data bits. In the current DAS Sustainment project, two different receiver options are being investigated. One option is a very low-cost hardware based receiver and the other is a completely software based receiver or Software Defined Radio (SDR). The receivers support TDRSS MA non-coherent return signal formats defined in Reference [3].

Both receiver options will receive the same digitized IF beam samples, process them, and output the resulting data bits in the same format. The output format consists of

unicast UDP/IP packets with a sequence number, length of data in the packet, SDDS timestamp of the first bit in the packet, and the demodulated data bytes. The data packets consist of a maximum of 1024 bytes of data. At lower data rates, the receivers output data packets at least every half second as long as they have at least one byte of data available. The half-second forced output option minimizes latency for frame synchronization processing of the output data. The receivers support convolutional decoding but any Reed-Solomon forward error correction coding is handled in the following software frame synchronization process.

Both receivers are provided with Doppler frequency profiles of the customer satellites to aid in fast signal acquisition. Both receiver options are very low-cost and much easier to replicate in large quantities than the legacy DAS equipment.

3. HARDWARE RECEIVERS

The hardware receiver is a modified COTS product consisting of a FPGA signal processing card and a multi-port Ethernet card. It uses a Xilinx Artix-7-100T FPGA clocked at 125 MHz. One interface on the Ethernet card provides a dedicated port to receive digitized IF data samples in UDP/IP multicast packets at a rate of 210 Mbps. A second Ethernet port is used to output demodulated data bits and provide a monitor and control interface.

The FPGA is programmed to input digitized IF samples in UDP/IP packets, perform Doppler processing, acquire the carrier and spreading code, track the signal, demodulate the signal, perform convolutional error correction, and output the processed, time stamped data bits in UDP/IP packets. It can demodulate spread spectrum signals with both binary phase-shift keying (BPSK) and staggered quadrature phase-shift keying (SQPN) modulation and output one or two data streams as appropriate. It is programmable to handle all NASA Gold codes and process data at rates from 1 Kbps up to 150 Kbps per channel.

The FPGA receiver cards are small enough that 3 full receivers and a power supply fit into an enclosure that takes 1U of rack space. The following figure shows a chassis with one receiver and a power supply.

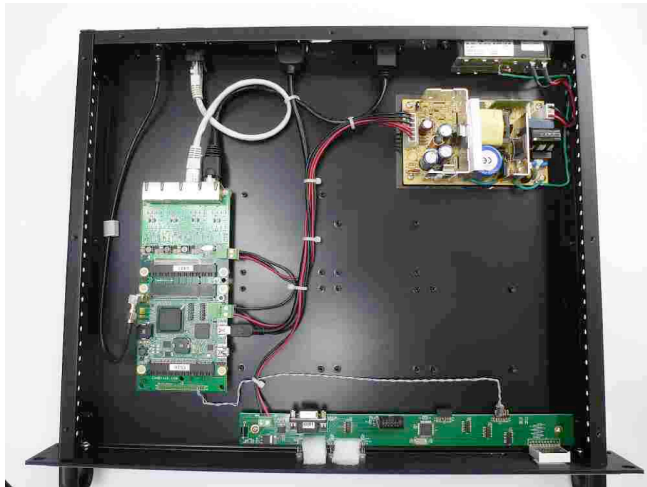


Figure 4 – ComBlock 1826 Single Receiver Chassis

The receiver entire digital signal processing is implemented within a single Xilinx Artix-7-100T FPGA running at 125 MHz along with a Gigabit ethernet MAC, IP network protocol, Doppler profile compensation, spread-spectrum demodulation and forward error correction. It processes digital IF samples at a rate of 6.25 million samples per second (MS/s) and can potentially handle sample rates up to 25 MS/s. One of the challenges of processing spread spectrum signals is the process of locating the signal and the current location in the chip sequence. The FPGA implementation in this receiver is able to acquire spread

signals rapidly by running 150 parallel searches spaced $\frac{1}{2}$ chip apart.

Once the spreading code is acquired, the received signal is despread and undergoes low-pass filtering, squaring, and a 2048 point FFT. The coarse acquisition time for this process is 86 ms. This produces either one signal for BPSK or two signals for QPSK. A second order Costas loop performs carrier tracking. Two symbol timing tracking loops (2nd order Gardner type) recover the symbol boundaries for the I and Q channels independently.

Satellite signals received by the TDRSS DAS system can have Doppler frequency offsets that start around +50 KHz and end up around -50 KHz at the end of their contact time. In order to acquire these signals that have significant amounts of Doppler the receiver needs to be given a Doppler profile table so it can perform its acquisition search in the correct carrier frequency range. The receiver ingests a Doppler profile table with 1-second entries of the predicted carrier center frequency. The table also includes the packet time for the first frequency in the table. The receiver begins using the 1-second frequency predictions when the digitized IF packet times match the table start time. The receiver breaks the 1-second frequency predictions into 64 steps per second to provide smoother tracking.

As baseband data bits are demodulated, they are gathered into an output buffer with an integer number of bytes in each UDP output packet. That buffer is output when either 1024 bytes have accumulated or at a minimum of every half second as long as there is at least one byte available. The buffer of output data also contains a time stamp of the first bit of data in the packet. This time is derived from the time in the digitized IF packet being processed at the time the bit is demodulated. This time reflects the time the IF signal was digitized at the base of the antenna.

A small ARM processor in the FPGS provides ancillary services such as non-volatile memory management for FPGA configuration files and user controls and FPGA programming at power up. This processor handles command and status packets for monitor and control of the receiver.

Receiver operation is configured by setting control registers. These register settings include modulation type, the spreading chip rate, the center frequency, and settings for the I and Q channel such as spread code and symbol rate. They also include the IP addresses for the receiver such as the addresses for receiving the digitized IF packets from an IP multicast group, and the destination address for the output packets.

Receiver status is monitored by sending requests to read the contents of the receiver status registers. These registers can be read individually or all in one request.

4. SOFTWARE RECEIVERS

The software receiver is a purely software-based (C++) receiver running on a standard (Linux) server platform. A dual processor quad-core 1U server (e.g. Dell R630) supports 5 or more simultaneous receivers (more at low data rates). The receiver was developed to process TDRS MA direct sequence spread spectrum (DSSS) signals and is highly-parameterized to provide the ability to process various signal formats under a variety of conditions. For this application, the receiver processes each of the MA DG1-Mode 2 signal formats specified in Reference [3]. Most of the parameters are specified as default values or are determined by other specified values, but all may be specified externally. In addition, a limited set must be specified through a remote monitor and control interface (e.g. PN code, data rate, symbol format).

The receiver is a multi-threaded application, with the threads communicating via internal message queues. The processing occurs sequentially, and is driven by the rate of data arriving at the front-end of the processing. For this application, these incoming data are the digitized beam-formed IF data, packetized into packets and distributed via multicast UDP/IP. The timestamps from these incoming packets are used to timestamp the data bits that are distributed by the receiver; the time for each outgoing bit corresponds to the (interpolated) timestamp of the first sample used to extract the bit.

The receiver communicates with external processes via several UDP/IP interfaces. These include the monitor-and-control interface, the (multicast) input-data interface, an interface to a frame processor and an interface on which it receives estimates of the Doppler-frequency offset. The input-data interface is via multicast digitized IF packets; the other interfaces use ASCII-formatted packets to transmit the information.

The processing sequence starts with the receipt of the IF data samples; these are re-sampled to two-samples-per-chip and passed to the acquisition thread. After acquisition of the PN Code and Carrier, tracking of the PN Code, Carrier and data symbols proceeds, resulting in demodulated data symbols. These symbols are decoded into data bits with a Viterbi decoder and distributed as bytes to a frame processor via UDP/IP packets. Each step occurs in a separate thread and the processing in each thread is driven by the rate of data in its input message queue. For this application, each thread is able to process the data faster than real-time for each of the MA DG1-Mode 2 signal formats specified in Reference [3].

The first step in the processing is the re-sampling of the data samples to approximately two-samples-per-chip. This resampling occurs at a continuously variable rate to account for a Doppler profile, and is relative to any specified nominal chipping rate and input sampling rate. For this application, the incoming sampling rate is 6.25 MS/s, but

the receiver will operate at any rate from twice the chipping rate to about 10 MS/s. Prior to acquisition, estimates of the current Doppler frequency offset are received in messages transported via UDP/IP; these estimates are used to update the resampling rate. After acquisition, the currently tracked Carrier is used to update the resampling rate.

Acquisition of the PN Code occurs in a non-coherent manner. The receiver generates PN sequences using the NASA Gold Code generator algorithm, comprising three single-shift registers with feedback taps. The number of PN epochs over which data are accumulated for the PN acquisition is determined by the expected SNR and the specified acquisition mode, which also determine the acquisition threshold. Three modes are available, wherein the threshold must be achieved in one-of-one, two-of-three or three-of-five attempts. The PN acquisition attempt occurs in parallel at 8 frequency offsets from the Doppler-modified carrier to increase the range of frequency uncertainty.

Following acquisition of the PN Code, the input data are despread, filtered, squared (to remove data transitions) and accumulated over $\frac{1}{2}$ symbols. These accumulations are input to an FFT to make a coarse determination of the carrier frequency. As part of this process, the PN code is slipped a few chips (\pm) in order to confirm the PN acquisition.

After the PN Code and Carrier are acquired, the resampled data are processed through the demodulator. The demodulator despreads the data samples and integrates the samples to accumulate soft symbols. At the same time it is tracking the symbol transitions with a second-order loop, the carrier in a (selectable) second- or third-order loop and the PN code in a second-order loop. The soft symbols are processed through a Viterbi decoder to produce the data bits. The decoded data bits are distributed via UDP packets, which include timing data from the incoming data stream.

The performance of the Receiver has been measured in other applications of a similar nature. Acquisition within 1 second has been confirmed for a variety of data rates between 640 bps and 150 kbps and signal levels at an E_s/N_0 between -4 and +20 dB.

5. INITIAL RECEIVER TESTING

Both receivers have undergone initial testing in a laboratory environment and they have also been connected to live TDRS signals at White Sands. Initial lab tests consisted of replaying files of recorded digitized IF packets. These files were recorded at White Sands and transported to Goddard on 2 terabyte disk drives. Some software was developed to read the packets and transmit them as UDP/IP multicast packets. One issue with these tests was the need for the packets to be transmitted at a steady rate similar to the 24,414 packets per second of the live TDRS packet stream. The hardware receiver only has a limited amount of packet buffer space and the FPGA processes packets at a fixed rate

that matches the standard rate of the digitized packets. If the packet flow is not very close to the proper packet rate, the FPGA input buffer will either overflow or underflow. Both conditions will result in the receiver dropping lock and losing data.

The software receiver runs on a server with many gigabytes of memory and has a much larger packet buffer. This allows the software receiver to cleanly handle much larger variations in the digitized packet rate.

However, replaying files only provides relatively short duration packet flows and is limited to test cases based on the recorded files. A live packet source was developed to do more extensive lab testing.

The development lab has a TDRS compatible modulator that can generate the full range of TDRS modulations, coding schemes, and data rates required for a DAS receiver. However, this modulator only generates a 370 MHz analog IF signal and the new DAS receivers only process digitized IF packets over Ethernet. This was handled by building a low-cost digitizer to turn the analog IF signal into properly formatted digitized IF packets. This consisted of using an Ettus Universal Serial Radio Peripheral (USRP) to digitize the analog signal and then GNU Radio software to turn the digitized samples into properly formatted SDDS packets.

Once the modulator and digitizer combination was functional, it was possible to generate any DAS signal format desired and run that signal for as long as desired. Along with testing receiver performance, this test configuration was used during development of the monitor and control system. It provided a wide range of different signals while the monitor and control system was used to configure the receivers for the different signal formats and then monitor receiver performance.

After lab testing verified basic functionality of both receivers, they were taken to White Sands for testing with live TDRS signals. Beamformers were configured to track the Hubble Space Telescope (HST), the Swift Gamma-Ray Burst satellite, and to point at the ground based WSC test transmitter. Since the digitized IF packets are sent using UDP/IP multicast, both a hardware and software receiver could be configured to listen to the same packet stream. This allowed direct comparison of the two different types of receivers processing identical packet streams.

6. SUMMARY

Initial testing has shown that these receivers have the potential to provide future DAS support for the TDRS System. With their low cost of about \$1K per receiver, it is very feasible to deploy a large number of receivers to connect to the new beamformers that can support up to 30 beams per beamformer. This was not possible with legacy receivers costing at least \$50K to \$100K per receiver.

Further testing is still needed to fully characterize the performance of both types of receivers under all possible signal conditions. Current plans are to deploy 3 receivers of each type at WSC in January 2016. This deployment will include a monitor and control system to provide continuous automated support for missions such as HST and Swift. This will allow for long duration testing of both receiver types in real world conditions.

Discussions are also underway with cubesat projects to determine if the expanded DAS-S capacity can be used to provide very low-cost and possibly no-cost support to cubesat missions. The DAS-S system can be expanded, at a very low cost, to simultaneously support 90 communication links across the three primary TDRSS ground stations. This provides a significant increase in capacity over the current DAS system that can only simultaneously support 16 communication links across two TDRSS ground stations.

The MA element signals are coming down to the ground 24 hours a day and there is no need for any special antenna pointing by the TDRSS spacecraft. This allows the DAS-S system to operate independent of other TDRSS scheduled services without any impact on normal operations. With this increased capacity, beams, receivers, and frame synchronizers could be dedicated to individual cubesats. They would be constantly listening for signals. Any time a signal was received, the demodulated data would be delivered to the end user. There is also an option for user spacecraft to send IP packets in HDLC framing and have the packets routed to their Internet destination address.

Another cubesat options being considered is combining digitized signals from multiple TDRS's to provide signal gain. This can allow either higher data rates or lower transmit power from cubesats. Any potential users are welcome to contact the SN if they are interested in helping test the evolving system or become future customers.

ACKNOWLEDGEMENTS

The authors would like to thank Michael Flynn at NASA's White Sands Complex for his support in understanding the IF signal processing details related to TDRSS. Also Spencer Lunbeck, Mark Hibner, and Robert Verstraete at WSC for their support in helping understand the operational details and issues of the current DAS system and supporting WSC tests. The Space Network Project, Code 452, at NASA's Goddard Space Flight Center, sponsored this work.

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- [3] Space Network Users Guide; Rev 10

BIOGRAPHY



Keith Hogie received a B.S. in Electrical Engineering from the University of Minnesota in 1974. He has an extensive background in designing and building satellite data processing systems, control centers, and networks at NASA/GSFC. He has developed ground data processing systems and control

centers for over 14 spacecraft over the last 40 years at NASA/GSFC. He was the technical leader of the Operating Missions as Nodes on the Internet (OMNI) project at GSFC where he developed and demonstrated new IP based communication technologies for future space missions. He is currently working on projects in NASA's Space Network to upgrade older systems and introduce new data processing concepts.



Bruce Flanders received a B.S. in Physics from Rensselaer Polytechnic Institute and a Ph.D. in Nuclear Physics from Kent State University. He has been developing algorithms, software and hardware for communications systems since 1996.

He was a member of the ITT team that developed the DAS system for NASA. He has developed and demonstrated new satellite communications technologies for NASA, as part of the TDRS Arraying program, including a software-based TDRS MA receiver. He is currently working on satellite communications projects for NASA and other customers.



Dan Paulson received B.S. in Electrical Engineering in 2006 from Johns Hopkins University, and is currently working towards his Ph.D. in Electrical Engineering at the University of Maryland with a focus on free space optical communication systems. He has worked in communications system development for the NASA/GSFC

since 2007, and helped develop and deploy multiple ground based systems combining both analog RF and digital signal processing elements. His current areas of focus are test bed deployment, coherent receiver performance characterization, and working with commercial vendors to ensure receivers meet Space Network requirements.



Alain Zarembowitch received a M.S. in EE & CS from MIT in 1981. He designs modular communication building blocks (ComBlock), hardware and VHDL components, for creating complex communication systems. Recent projects include spread-spectrum modems and high-speed low-latency Internet

protocols implementation in FPGAs.



Haleh Safavi received a B.S. in Electrical Engineering from Tabriz University, Iran, in 1996, a M.S. in Telecommunication Engineering from Azad University, Iran, in 1999, and Ph.D. in Electrical Engineering from University of Maryland Baltimore County in 2010. She is a Lead Electrical Engineer with

Digital Signal Processing and Image Processing background working in Space Network Project. She has designed and developed software and Hardware DSP Algorithms for Software Define Radio. She is currently the lead Engineer for Digital Architecture Testing and Demand Access System Augmentation project.



Jeffrey Lubelczyk received a B.S. in Electrical Engineering from Oral Roberts University, in 1989, a M.S in Electrical Engineering from Johns Hopkins University in 1995. As a NASA employee for over 26 years, he has designed and developed data communication systems, science data

processing software, spacecraft communication systems, and served as a lead system engineer for many large NASA projects and programs. He is currently the Mission System Engineer for the Space Network Project.