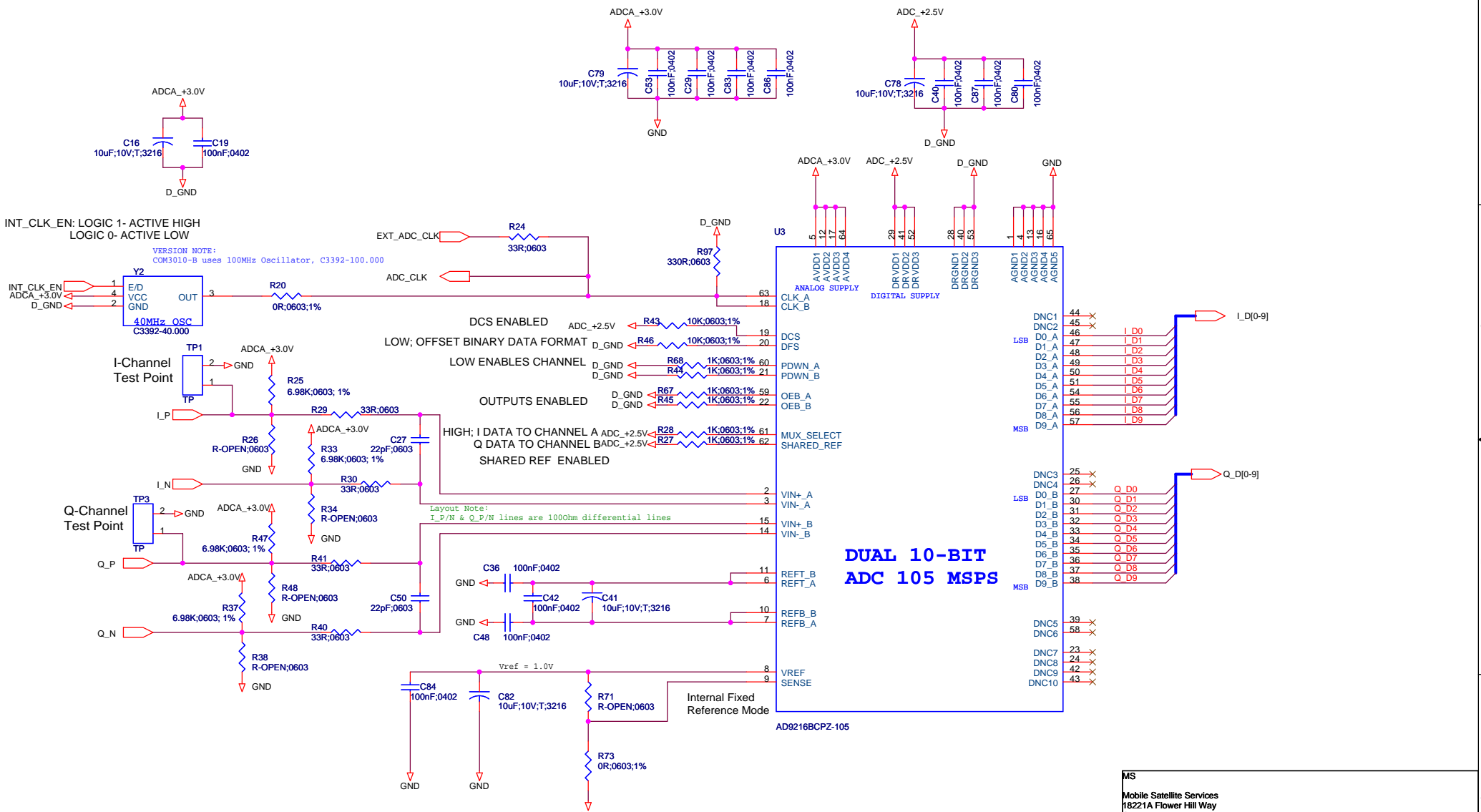


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External ADC sampling clock (input)
EXT_ADC_CLK ← EXT_ADC_CLK

Input AGC (input)
AGC_IN ← AGC_IN

ADC sampling clock (output)
ADC_CLK → ADC_CLK

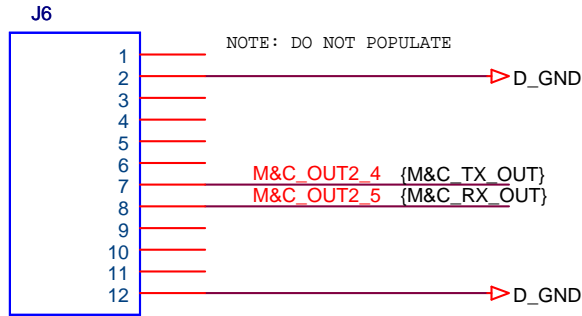
PLL_REF → PLL_REF

M&C_OUT1_[4-5] → M&C_OUT1_5
M&C_OUT1_4

M&C_OUT2_[4-5] → M&C_OUT2_5
M&C_OUT2_4

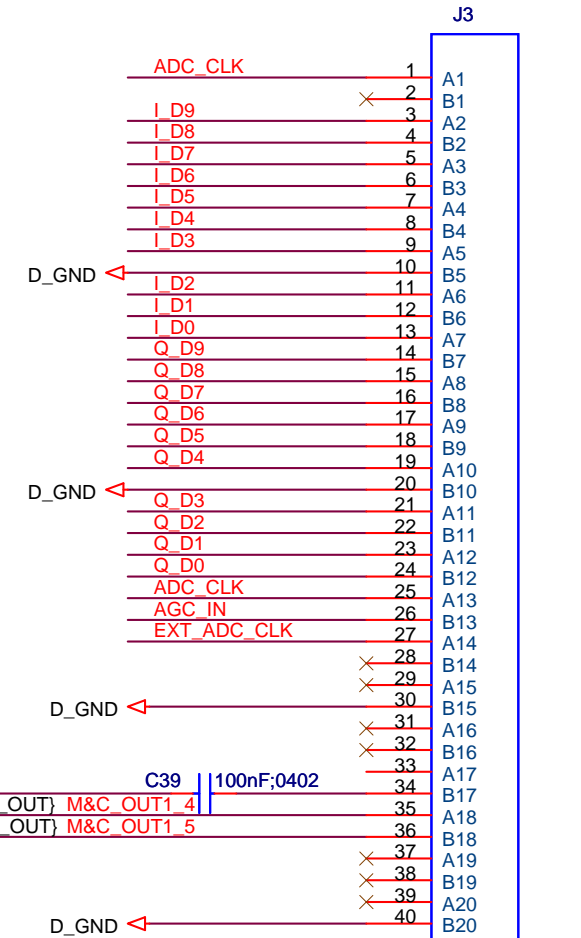
I_D[0-9] → I_D9
I_D8
I_D7
I_D6
I_D5
I_D4
I_D3
I_D2
I_D1
I_D0

Q_D[0-9] → Q_D9
Q_D8
Q_D7
Q_D6
Q_D5
Q_D4
Q_D3
Q_D2
Q_D1
Q_D0



TMMH-106-01-L-D-RA

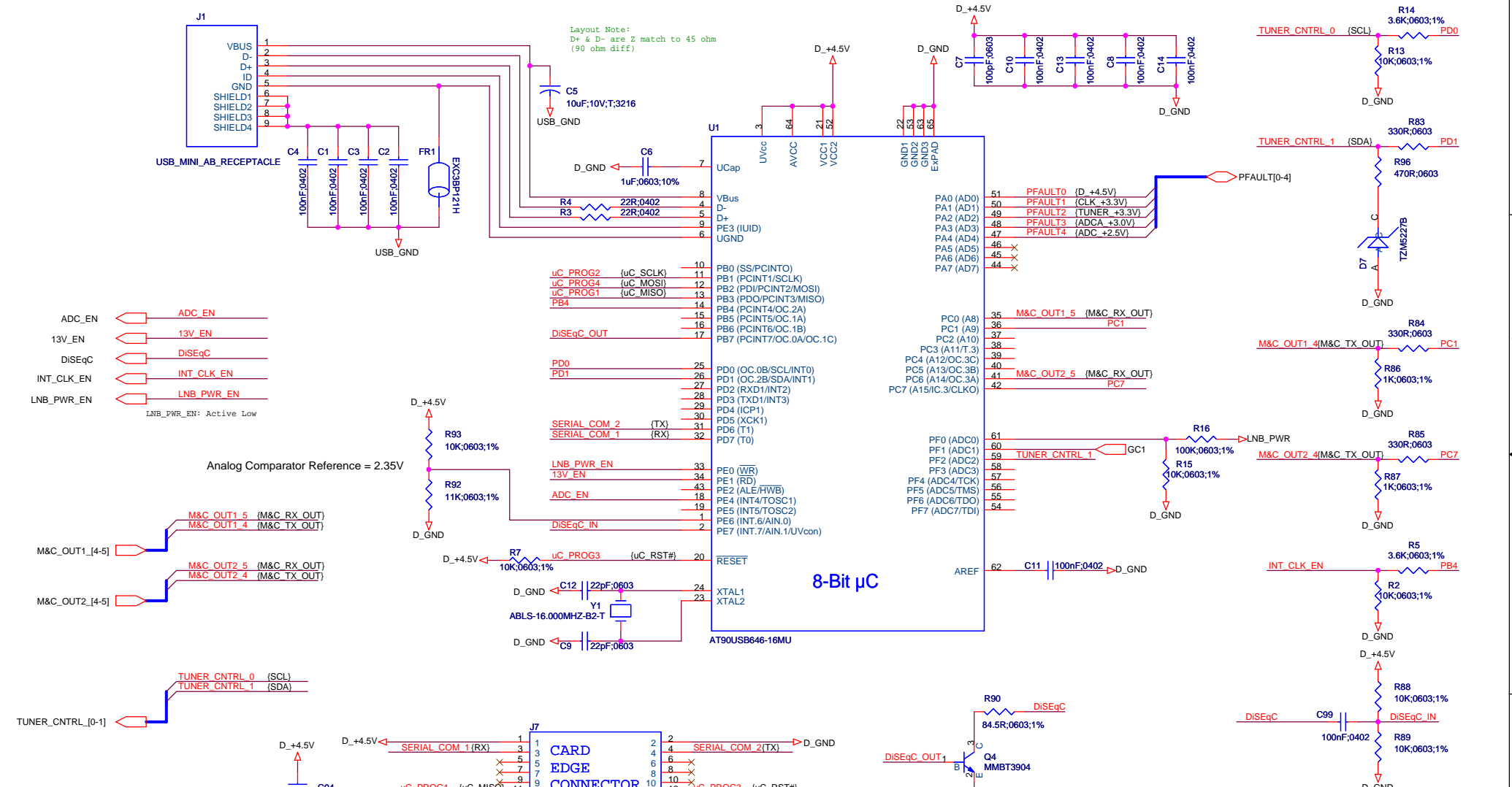
M&C OUTPUT TO
EXTERNAL FREQ. REF
MALE CONNECTOR



TMMH-120-01-L-D-RA

RIGHT OUTPUT
CONNECTOR

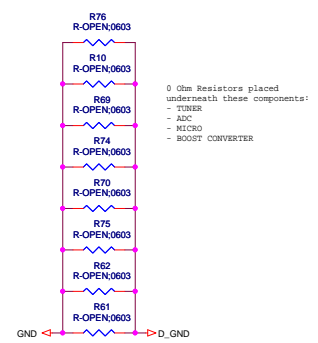
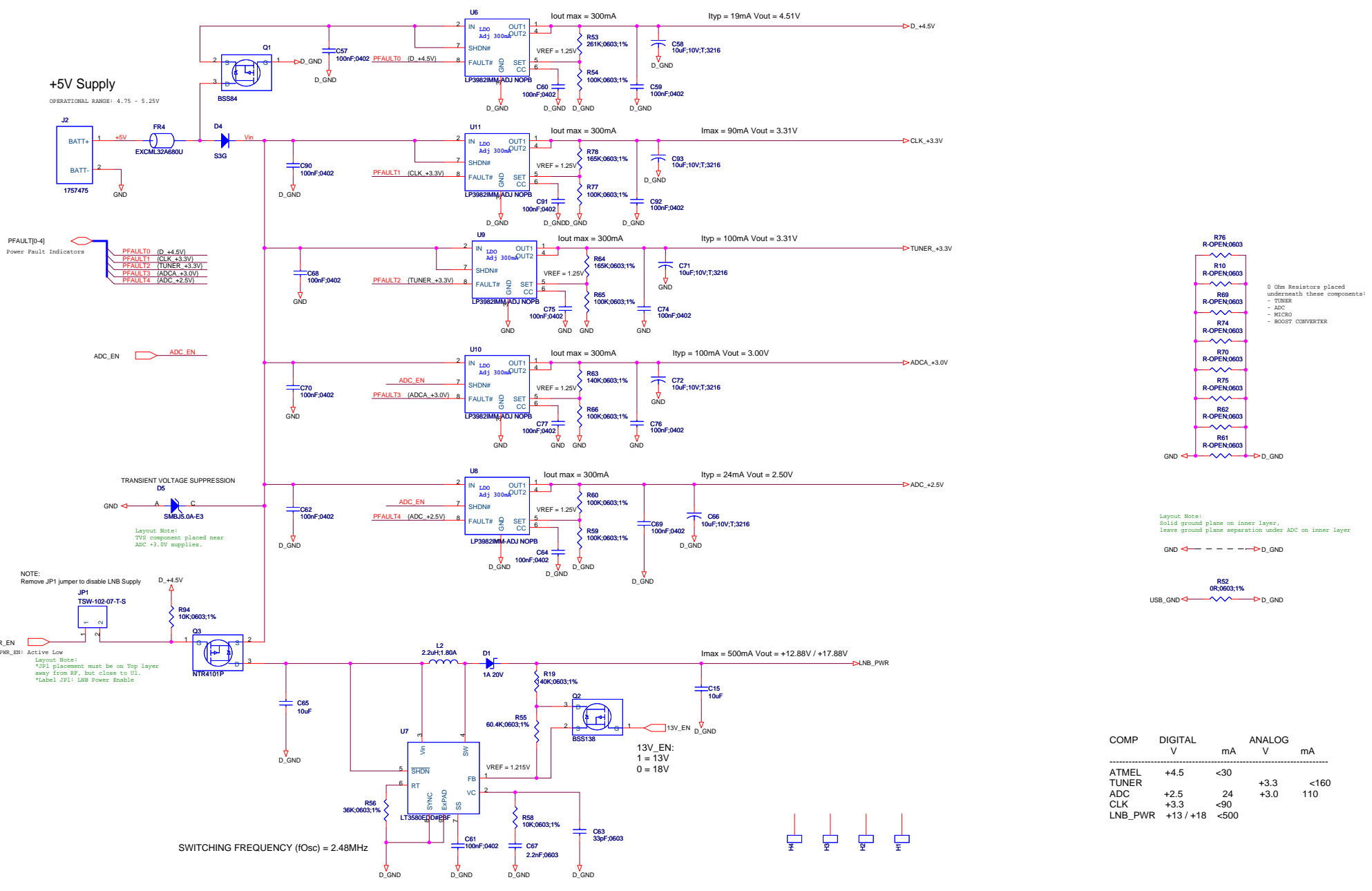
MS		
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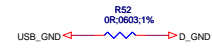
+5V Supply

OPERATIONAL RANGE: 4.75 - 5.25V



0 Ohm Resistors placed underneath these components:
- TUNER
- ADC
- MICRO
- BOOST CONVERTER

Layout Note:
Solid ground plane on inner layer,
leave ground plane separation under ADC on inner layer



COMP	DIGITAL V	mA	ANALOG V	mA
ATMEL	+4.5	<30		
TUNER			+3.3	<160
ADC	+2.5	24	+3.0	110
CLK	+3.3	<90		
LNB_PWR	+13/+18	<500		

SWITCHING FREQUENCY (f_{osc}) = 2.48MHz

NOTE:
Remove JP1 jumper to disable LNB Supply



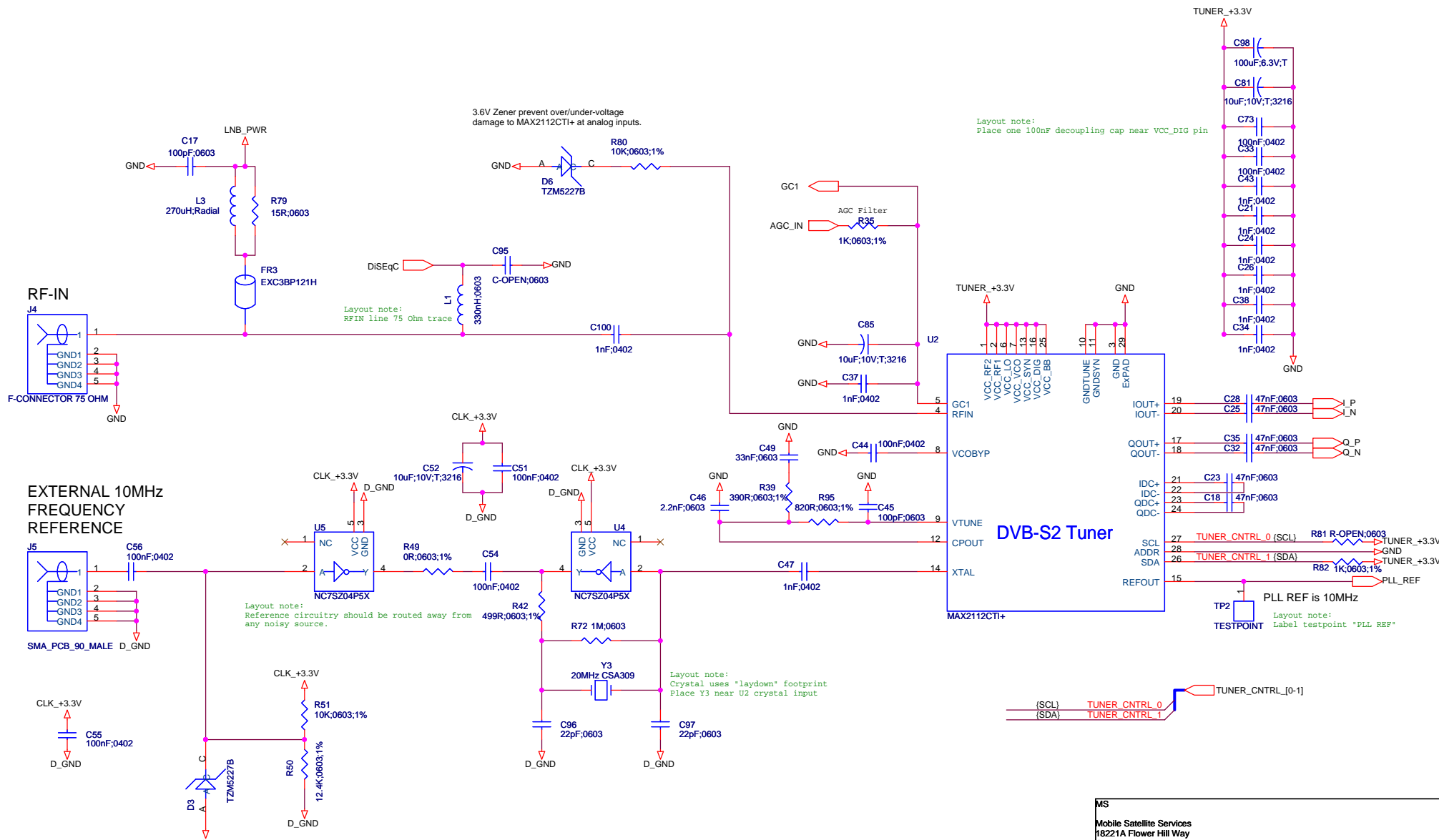
LNB_PWR_EN: Active Low
Layout Note:
*JP1 placement must be on Top Layer away from RF, but close to U1.
*Label JP1: LNB Power Enable

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USA

Title
COM-3010 / POWER

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