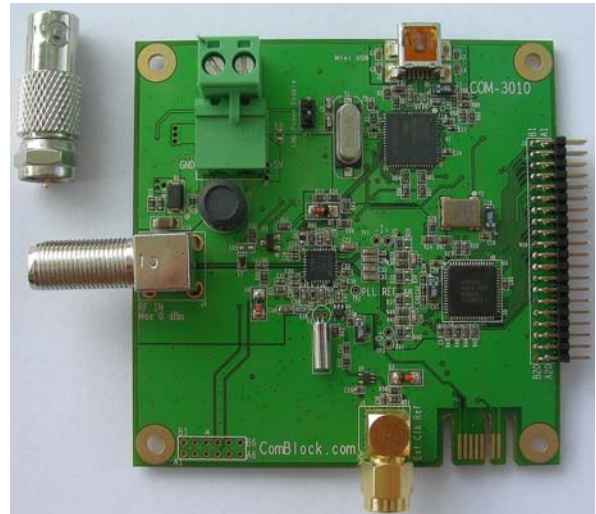


Key Features

- [925 – 2175 MHz] Receiver for direct broadcast satellite applications or other broadband I/Q demodulator applications
- Designed for direct connection to K_a band, K_u band and C band LNBs
 - Type F female connector
 - 75Ω input impedance
 - -63 dBm to 0 dBm input level
 - $+13 / +18\text{V}$ LNB supply provided
 - Bi-directional DiSEqC™ control
- Built-in IF AGC, 73 dB dynamic range
- Low phase-noise frequency synthesizer can be tuned over entire range by steps of 19Hz
- Optional external SMA, 10 MHz frequency reference for the frequency synthesizer
- Fixed $40 \text{ MSamples/second}$ (MSPS) option -A or 100 MSPS option -B internal or variable external sampling clock
- Dual 10-bit Analog-to-Digital Converter (ADC), up to 105 MSPS
- Programmable baseband filtering bandwidth between 4 and 40 MHz
- USB Monitoring & Control Interface
- Only single $+5\text{V}_{\text{DC}}$ supply required
- Connectorized 3" x 3" module for ease of prototyping

Typical Applications

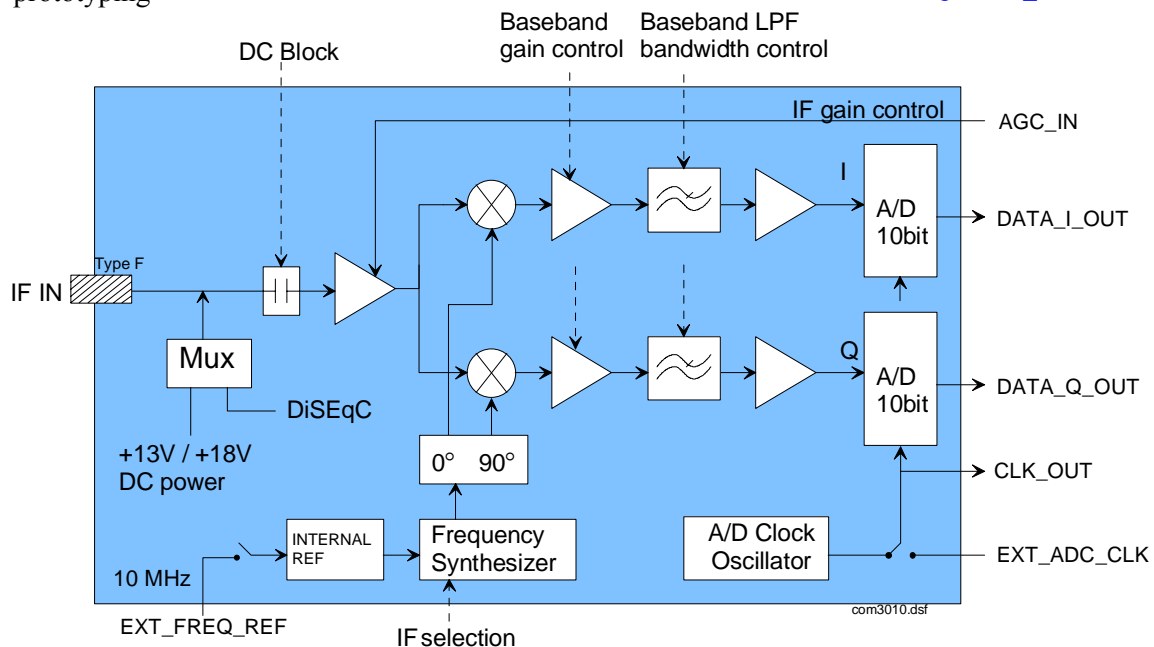
- Direct to home satellite TV set-top box
 - DVB-S2 or DVB-S
- Software Defined Radio Front End
- VSATs



COM-3010 [925 – 2175 MHz] RECEIVER

For the latest data sheet, please refer to the **ComBlock** Web site: www.comblock.com/download/com3010.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm




Block Diagram

Electrical Interface

Inputs / Outputs

Inputs	Definition
IF_IN	925 - 2175 MHz; J4, Type F connector, female, 75 Ω impedance; Receiver sensitivity (worst case): -63 dBm at IF input for full scale signal (1V _{pp}) at A/D converter; Maximum input (operating): 0 dBm Maximum input (no damage): +10 dBm IF AGC range: 73 dB typ. Baseband Gain range: 15 dB; Multiple signals are sent in the reverse direction (from the COM- 3010 receiver to the external LNB) over the same coaxial cable: <ul style="list-style-type: none"> LNB power supply 22 KHz control, DiSeqC™
EXT_REF_CLK	Optional Input: External 10 MHz frequency reference for frequency synthesis; Sine, clipped sine or square wave; J5, SMA male connector, 50 Ω Minimum level: 2.0V _{pp} Maximum level: 3.3V _{pp}
Digital I/Os	Definition
DATA_I_OUT[9:0]	In-phase baseband signal; 10-bit digital samples; Unsigned format: <ul style="list-style-type: none"> 0x3FF the most positive signal 0x200 represents a zero 0x000 the most negative signal 40/100 MSPS Unsigned
DATA_Q_OUT[9:0]	Quadrature baseband signal; Same characteristics as above
CLK_OUT	Digital sampling clock output; Up to 105 MSPS; Read the samples at the rising edge of CLK_OUT
AGC_IN	Input: Control the analog gain prior to A/D conversion; Digital (pulse-width modulated) or analog; The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter; Maximum gain: 0.0V Minimum gain: +3.0V



EXT_ADC_CLK	Optional input: Externally supplied ADC sampling clock; Clock supplied to Analog-to-Digital converter sampling input; Level: LVTTTL, 0V to +3.3V Supply this clock at J3, pin A14 Enabled by  software control Selecting sampling rates less than half the baseband filter bandwidth may result in aliasing. Minimum Rate: 10 MSPS Maximum Rate: 105 MSPS
USB Monitoring & Control	Mini-USB connector (type AB); Full speed / Low Speed
Power Interface	4.75 – 5.25V _{DC} ; Terminal block; Power consumption is 300mA typ. (excluding internal LNB supply)

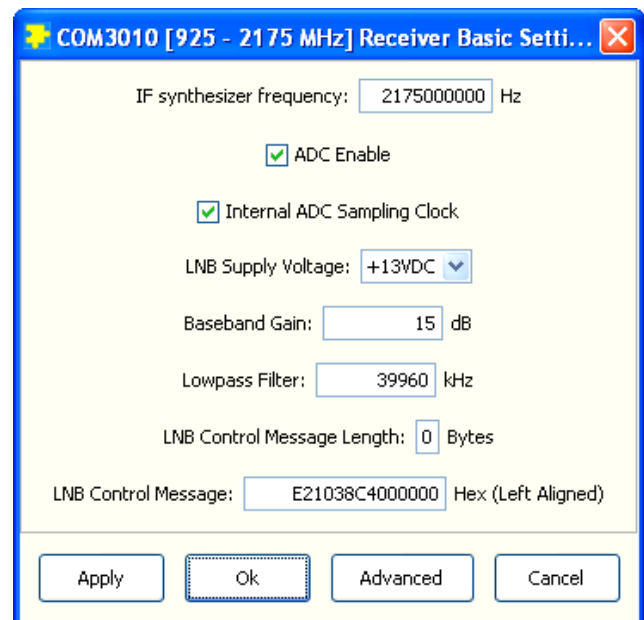
Electrical Interface

Configuration (via USB)

Complete ComBlock assemblies can be monitored and controlled centrally over a USB connection using the **ComBlock Control Center** software. A mini-USB cable is required.

Configuration (Basic)

The easiest way to configure the COM-3010 is to use the **ComBlock Control Center** software supplied with the module on CD. In the ComBlock Control Center window detect the ComBlock module(s) by clicking the  *Detect* button, next click to highlight the COM-3010 module to be configured and click the  *Settings* button to display the *Basic Settings* window shown below.



Settings Window

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

The module configuration parameters are stored in non-volatile memory. All control registers are read/write. Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Programmers developing custom applications (using the [ComBlock API](#) instead of the supplied ComBlock Control Center graphical user interface) should know that frequency changes and DiSEqC™ are enacted upon (re-)writing to the last valid register of the parameter. REG3 & REG6, respectively for frequency and typically REG10 for DiSEqC™ depending on the Message length (see *Note 2*)

Parameters	Configuration
IF Synthesizer Frequency	Valid range: 925– 2175 MHz; Steps of ~19 Hz ¹ ; Expressed in Hz; REG0: bit 7:0 (LSB) REG1: bit 15:8 REG2: bit 23:16 REG3: bit 31:24 (MSB)
ADC Sampling Clock Source Select	0 = Internal 1 = External REG4: bit 0
Analog-to-Digital Converter (ADC) Enable	0 = Disable 1 = Enable REG4: bit 1
LNB Supply Voltage Warning: Enabling LNB supply may cause damage to test equipment.	00 = off 01 = +13V _{DC} 10 = +18V _{DC} 11 = off REG4: bits 3-2
Baseband Gain Setting	Gain range 0 – 15 dB Expressed in dB REG4: bits 7-4
Lowpass Filter: –3 dB cutoff frequency	Valid range: 4 – 39.96 MHz; Steps of 290 kHz; Expressed in kHz; REG5: bits 7:0 (LSB) REG6: bit 15:8 (MSB)
LNB Control Message Length	Message length in bytes; Valid range: 0 – 7; 0 = no message sent Reset to 00 after a message sent ² REG7: bits 2-0

Optional LNB Control Message (DiSEqC™)	Up to 7 bytes: frame sync, family of devices, command byte, data; Parity bits are automatically inserted; Bytes are transmitted LSB (REG8) 1 st ; Sequence is sent upon writing to last REG in message ² ; REG8: bits 7-0: Frame byte REG9: bits 7-0: Address byte REG10: bits 7-0: Command byte REG11: bits 7-0: Data byte 1 REG12: bits 7-0: Data byte 2 REG13: bits 7-0: Data byte 3 REG14: bits 7-0: Data byte 4
--	---

Configuration Registers

Note 1: REG3:0 is a whole number *Hertz* approximation, using an internal step size of

$$19.0735 \text{ Hz} \text{ or } \frac{20 \times 10^6}{2^{20}} \text{ Hz}$$

Note 2: The LNB Control Message sequence is sent upon writing to the last valid register of the message. Last REG# = 7 + REG7₁₀ (Message length)
Last REG# Valid Range: REG8 – REG14
(Ex: REG7 = 03, sequence sent upon REG10 write)

Monitoring ⓘ (via USB)

Monitoring the status of the COM-3010 is performed by viewing the ⓘ *Status* window in ComBlock Control Center. All register values are displayed in a hexadecimal, but other formats are displayed by hovering over the hex value with the cursor.

Custom applications can monitor module status again, by using the [ComBlock API](#).

Parameters	Monitoring
Reserved	SREG0: bits 0
Internal Power Supply Fault <i>(see schematics for reference)</i>	0 = Normal Operation 1 = Fault Condition SREG0 Bit 7: ADC_+2.5V SREG0 Bit 6: ADCA_+3.0V SREG0 Bit 5: TUNER_+3.3V SREG0 Bit 4: CLK_+3.3V SREG0 Bit 3: D_+4.5V
LNB Supply Voltage	$V_{LNB} = \text{SREG1}_{10} * \frac{49.5}{255} V_{DC}$ SREG1: bit 7-0
AGC Voltage	$V_{AGC} = \text{SREG2}_{10} * \frac{4.5}{255} V_{DC}$ SREG2: bit 7-0
Reserved	SREG3: bit 7-0
LNB Response Message Length	Message length in bytes; Valid range: 0 – 3; 0 = no message received Reset to 0 upon sending an

	<i>LNB Control Message</i> SREG4: bits 1-0
LNB Response Message Parity Check	Odd Parity Byte Check; 0 = No Error 1 = Error Reset to 0 upon sending an <i>LNB Control Message</i> SREG4: bit 7: Frame byte SREG4: bit 6: Data byte 1 SREG4: bit 5: Data byte 2
LNB Response Message (DiSEqC™) If available ³	Up to 3 bytes: Frame/OK status byte and up to 2 data bytes; Parity bits not included; SREG5: bits 7-0: Frame byte SREG6: bits 7-0: Data byte 1 SREG7: bits 7-0: Data byte 2

Monitoring Registers


Note 3: The *LNB Response Message* is only available after an *LNB Control Message* has been sent and will be indicated by a non-zero value for SREG4 bits 1-0. If SREG4=0, then none of the values in SREG5–7 are valid. If SREG4=1 then only SREG5 is valid, etc.

Operations


LNB Control


The COM-3010 is capable of controlling the RF front-end polarity, satellite and frequency band over a single coaxial cable. The control method is compliant with the Digital Satellite Equipment Control protocol, DiSEqC™, an industry standard.

The polarization is selected by supplying either +13V or +18V. How to enabling this supply is described below, under [LNB Power Supply](#). The LNB frequency bands and/or low-noise block down-converters (LNB) on a multi-feed system are selected by generating a binary DiSEqC™ message in the form of a modulated 22 kHz tone.

The use of the LNB Control Message is optional. No message will be sent by entering a value of ‘0’ in the *LNB Control Message Length* text field, found in the **ComBlock Control Center**  *Settings* window. A value from 1 to 7 will send a message upon the next *Apply* or *Ok* button click, assuming the message field below it is valid. Two hex characters are required for each byte sent in the *LNB Control Message* text field. The text field is left aligned, the left most byte is the “Frame,” and is sent first. DiSEqC™ standard calls for at least 3 bytes sent (in order): Frame, Address, Command and then any optional “Data” bytes. Up to 4 more “Data” bytes may be appended to the end of a message for a maximum total of 7 bytes sent. Bytes



to the right of the last byte sent are ignored and their values are not updated in the internal registers. All parity bits are automatically inserted in the appropriate locations within the message framework.

DiSEqC™ messaging functionality with a DiSEqC™ compatible LNB switch can be verified by entering the appropriate message below. After which the DC voltage (+13/18V) can be observed switching from one switch port to another, typically from port 1 to 2.  Valid DiSEqC™ messages to change LNB switch position, for a two and four position switch respectively: (Either +13V or +18V must be enabled)
LNB Control Message Length: 03 / 04 (2 / 4 pos.)
LNB Control Message: E21026 / E21038C4 (2 / 4)

The *LNB Response Message*, seen in the  *Status* window of ComBlock Control Center is only available after an outgoing *LNB Control Message* has been sent. The COM-3010 will poll for a response from a DiSEqC™ 2.0 or higher compatible device, for up to 150ms after sending any outgoing *LNB Control Message*. During this polling period no other microcontroller activities can be performed. Each incoming message bit should be 1.50ms (±15%) long for accurate decoding. The *LNB Response Message* can be viewed in SREG5 up to SREG7, depending on the message length indicated in SREG4. See the [Monitoring](#) section for additional information.

LNB Power Supply

The COM-3010 is capable of supplying either +13V_{DC} or +18V_{DC} to an LNB through the J4, Type F connector. The maximum supply current is 500 mA.

In addition to the  software control, the provided jumper must be populated on JP1 to enable the supply. JP1 is labeled “LNB Power Enable” and located near the +5V terminal block. An accurate LNB supply voltage measurement can be viewed at any time in SREG1 of the  *Status*.

Warning: Enabling the LNB supply may cause damage to test equipment such as a signal generator.

Internal vs. External Frequency Reference for Frequency Synthesizer

An external 10 MHz frequency reference can be used when the user application requires precise frequency stability. In this case, simply connect a 10 MHz sine, clipped sine or square wave to the J5 EXTERNAL_FREQ_REF male SMA connector.

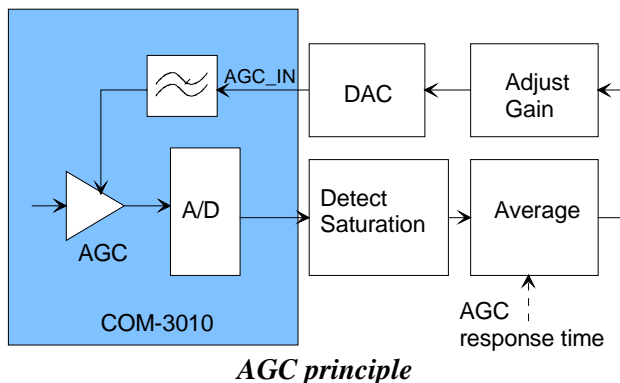
Detection is automatic, thus no configuration change is needed. Upon removal of the external 10 MHz frequency reference signal, the module reverts to the internal frequency reference.

Internal vs. External ADC Sampling Clock

The source for the Analog to Digital converter clock can be selected as internal (fixed: 40 or 100 MSPS) or external (variable: 10 min. to 105 max. MSPS.) External clock is enabled by software command and connecting an external clock to EXT_ADC_CLK, supplied at the J3 connector, pin A14.

Automatic Gain Control

The default Automatic Gain Control (AGC) mechanism assumes that an external circuit (a demodulator for example) detects saturation conditions at the Analog-to-Digital converter output and adjusts the receiver gain, AGC_IN accordingly, as illustrated below.



The AGC_IN signal can be a simple pulse-width modulated (PWM) digital signal or an analog signal from a DAC. The AGC_IN signal undergoes low-pass filtering within the COM-3010 in order to average out a PWM control signal. By default, the AGC response time is limited to approximately 63 ms, by the RC low-pass filter where $R = 1\text{k}\Omega$ and $C = 10\mu\text{F}$.

For applications requiring a faster AGC response time, a few μs in the case of burst receivers for example, the RC low-pass filter bandwidth can be greatly increased by changing the R35 resistor and/or the C85 capacitor. The COM-3010 AGC response time can be specified at the time of order.

AGC_IN's DC voltage can be monitored real time in SREG2 of the Status.

Test Points

Test Points are provided for easy access by an oscilloscope probe.

Test Point	Definition
I+ (TP1)	Baseband signal, I-channel, at A/D converter input; The nominal amplitude is $1V_{pp}$ (single ended) when the AGC loop is closed by a following demodulator (COM-1203 or equivalent)
Q+ (TP3)	Baseband signal, Q-channel, at A/D converter input. Nominal amplitude is $1V_{pp}$ (single ended) when the AGC loop is closed
I-, Q-	Ground
PLL REF (TP2)	10 MHz synthesizer reference clock

Hardware Test Points

Performance

Internal Receiver Clock Reference

The internal crystal performance is as follows:

- Tolerance: ± 10 ppm max. @25°C
- Temperature stability (-10° to +60°C): ± 50 ppm max.
- Aging: ± 5 ppm/year max. (1st year) @25°C

I/Q Frequency Down-Conversion

Quadrature phase error: 3.5° (Max.)

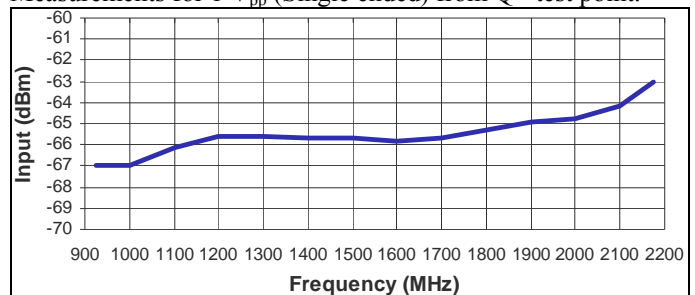
Quadrature gain error: ± 1.0 dB (Max.)

Baseband Low-Pass Filters

The 7th order Butterworth baseband lowpass filters are programmable. The filters' -3 dB (single sided) cutoff frequencies can be adjusted from 4 to 39.96 MHz in steps of 290 kHz. Power consumption is a function of the filter bandwidth setting, the higher the bandwidth, the higher the current use.

Input Sensitivity

Measurements for $1V_{pp}$ (Single ended) from Q+ test point.



Input Sensitivity at 1 V_{pp}

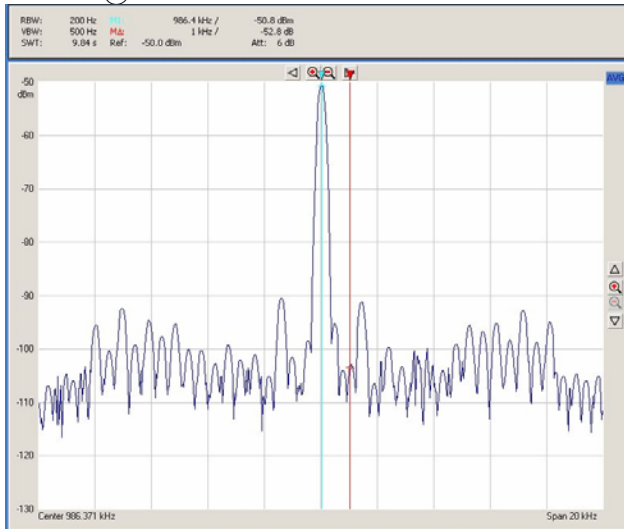
Phase Noise

Typical phase noise performance at 2.175 GHz:

-76 dBc @ 1 kHz away from the carrier

-82 dBc @ 10 kHz

-94 dBc @ 100 kHz



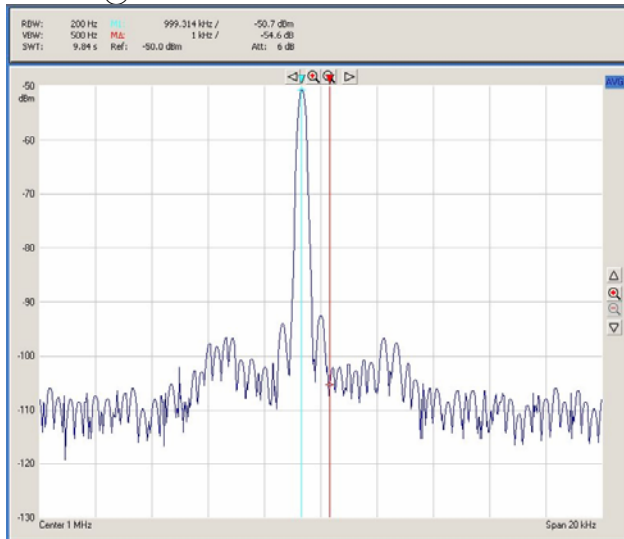
$F_{IN} = 2176 \text{ MHz}$ $F_{LO} = 2175 \text{ MHz}$

Typical phase noise performance at 2.175 GHz with 10 MHz reference:

-78 dBc @ 1 kHz away from the carrier

-85 dBc @ 10 kHz

-94 dBc @ 100 kHz



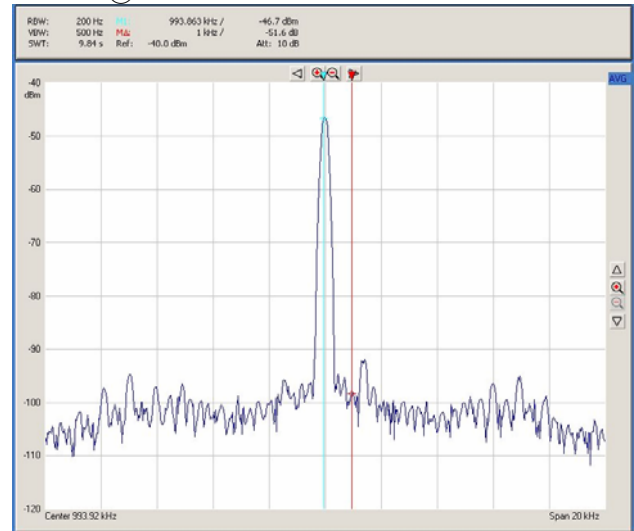
$F_{IN} = 2176 \text{ MHz}$ $F_{LO} = 2175 \text{ MHz}$ w/ Ext. Ref.

Typical phase noise performance at 925 MHz:

-75 dBc @ 1 kHz away from the carrier

-82 dBc @ 10 kHz

-92 dBc @ 100 kHz



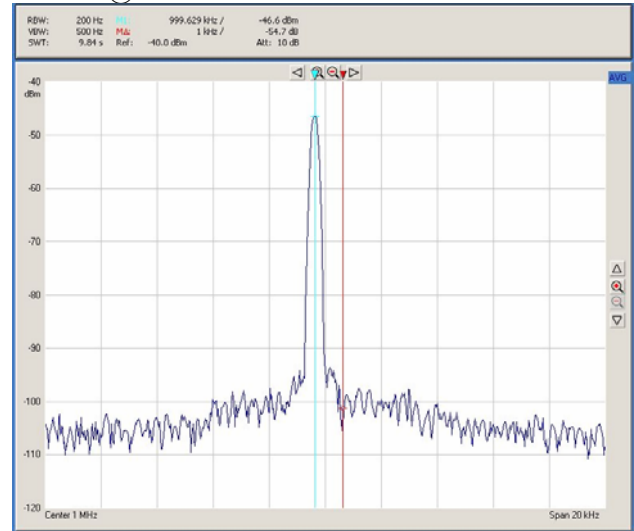
$F_{IN} = 926 \text{ MHz}$ $F_{LO} = 925 \text{ MHz}$

Typical phase noise performance at 925 MHz with 10 MHz reference:

-70 dBc @ 1 kHz away from the carrier

-82 dBc @ 10 kHz

-92 dBc @ 100 kHz



$F_{IN} = 926 \text{ MHz}$ $F_{LO} = 925 \text{ MHz}$ w/ Ext. Ref.

Spectral spurious lines are at -60 dBc or lower.
(TBC)

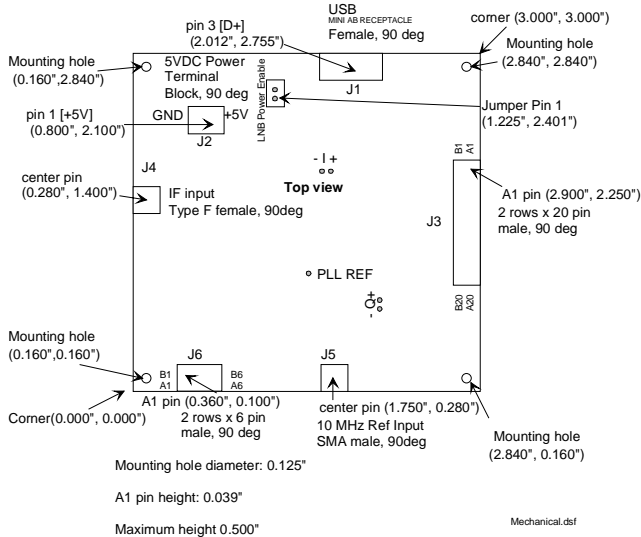
Noise Floor

Measured at 25°C and maximum IF & baseband gain

-159 dBm/Hz @ $F_{LO} = 925 \text{ MHz}$

-154 dBm/Hz @ $F_{LO} = 2175 \text{ MHz}$

Mechanical Interface

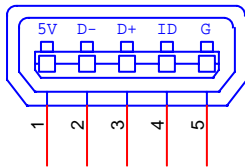


Mechanical Specification (not to scale)

Pinout

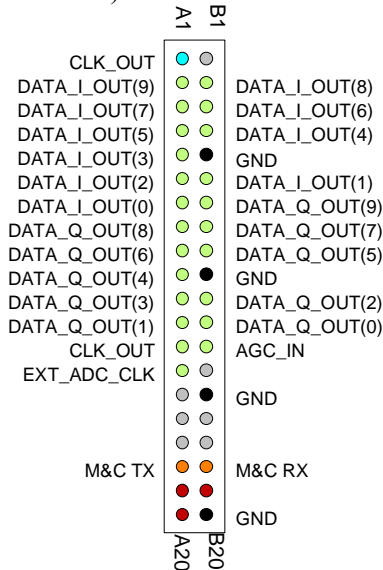
Mini USB Connector J1

The COM-3010 is a USB device with a mini type AB connector. (G = GND)



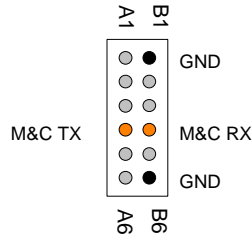
Output Connector J3

40-pin (2 rows x 20) 2mm male connector



Output Connector J6

12-pin (2 rows x 6) 2mm male connector
[Not Populated]



I/O Compatibility List

(Not an exhaustive list)

Input	Output
C / K _u / K _a bands LNBS	COM-1200 VHDL/FPGA development platform, Spartan3-2000 & USB 2.0
	COM-1400 VHDL/FPGA development platform, Spartan3-400 & USB 2.0
	COM-1202 / COM-1203 PSK/QAM/APSK Modem
	COM-1418 Direct sequence spread-spectrum demodulator
	COM-1027 FSK Demodulator
	COM-8002 High-speed data acquisition
	COM-1008 Variable Decimation
	COM-2001 Dual D/A converter (baseband)

Input and ComBlock Compatibility List

ComBlock Ordering Information

COM-3010-A [925 – 2175 MHz] Receiver, AGC, Dual 40MSPS A/D converter

COM-3010-B [925 – 2175 MHz] Receiver, AGC, Dual 100MSPS A/D converter

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