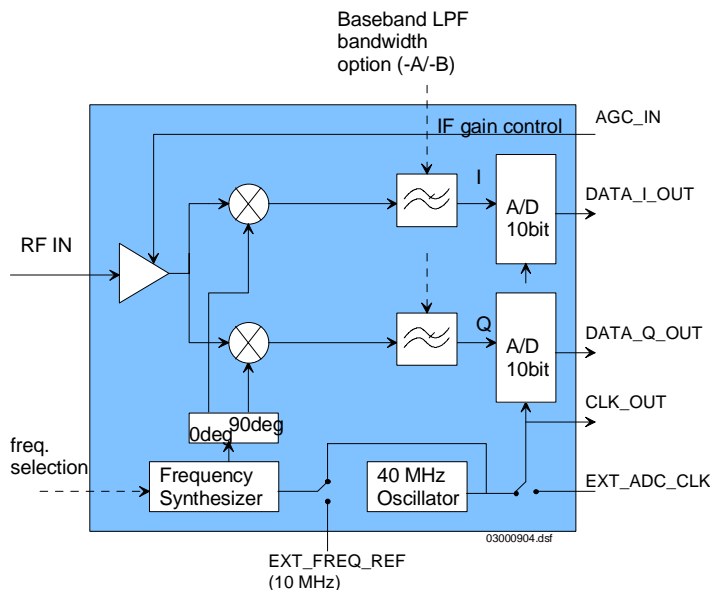


Key Features

- [20-90 MHz] receiver.
- Sensitivity: -64 dBm RF input for full scale 10-bit output samples.
- Built-in RF AGC, 40 dB dynamic range.
- Extremely low-phase noise frequency synthesizer can be tuned over entire range by steps of 0.04Hz.
- Selectable internal / external 10 MHz frequency reference for the frequency synthesizer.
- 8 preset frequencies for fast (<2ms) local oscillator frequency tuning.
- Dual 10-bit Analog-to-Digital converters, 40 Msamples/s.
- Selectable internal 40 MHz / external ADC sampling clock (to synchronize multiple receivers).
- Three baseband filtering options:
 - -A : 280 KHz passband
 - -B 12 MHz passband
 - -C 3 MHz passband
- SMA connectors. Single 5V supply. Connectorized 3"x 3" module for ease of prototyping.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com3004.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm.



Electrical Interface

Inputs / Outputs

Inputs	Definition
RF_IN	20 - 90 MHz. SMA male connector (J3). 50 Ohm impedance. Receiver sensitivity: -59 dBm at RF input for full scale signal at A/D converter (frequency dependent, see plot below). Maximum input (operating): -14 dBm Maximum input (no damage): +10 dBm AGC range: 40 dB.
EXT_FREQ_REF	Optional input. External 10 MHz frequency reference for frequency synthesis. Sinewave, clipped sinewave or squarewave. SMA male connector (J8). Input is AC coupled. Minimum level 0.6Vpp. Maximum level: 3.3Vpp. Note: when selecting external reference clock, the local oscillator phase noise depends on the input signal level: the larger the signal, the better the phase noise.
EXT_ADC_CLK	Optional input. Externally supplied Analog-to-Digital converter sampling clock. Enabled or disabled by software control. LVTTTL 0 – 3.3V. Selecting sampling rates less than half the baseband filter bandwidth may result in aliasing.

Digital Output Signals	Definition
DATA_I_OUT[9:0]	In-phase baseband signal. 10-bit digital samples. 40 Msamples/s. Unsigned (straight offset binary) 10 0000 0000 = 0V ADC input 11 1111 1111 = +0.5V input 00 0000 0000 = -0.5V input
DATA_Q_OUT[9:0]	Quadrature baseband signal. 10-bit digital samples. 40 Msamples/s. Same format as DATA_I_OUT.
CLK_OUT	Digital clock. 40 Msamples/s if internal selection, otherwise EXT_ADC_CLK's frequency. Read the samples at the rising edge of CLK_OUT.
ADC_CLK_OUT	Same as CLK_OUT.
AGC_IN	Input signal to control the analog gain prior to A/D conversion. Can be digital (pulse-width modulated) or analog. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain. Without any subsequent module, the COM-3004's gain is set at its maximum and may thus saturate.
Control Lines	Definition
PLL_STROBE	Low-voltage (3.3V / 0V) TTL input control. Used to increment the modulo- N_{freq} frequency pointer (where N_{freq} is defined in Register 35) in a round-robin sequence. Rising edge triggered. Minimum pulse width: 10 μ sec. Connector J6 Pin A3.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.9 – 5.25VDC. Terminal block. Power consumption is 950mA (200 MHz DDS clock)

Important: digital I/O signals are 0-3.3V LVTTTL. Inputs are NOT 5V tolerant!

Configuration

Complete assemblies can be monitored and controlled centrally over a single asynchronous serial connection or, when available through adjacent ComBlocks, LAN/TCP-IP, USB, or CardBus connection.

The module configuration is stored in non-volatile memory.

Configuration (Basic)

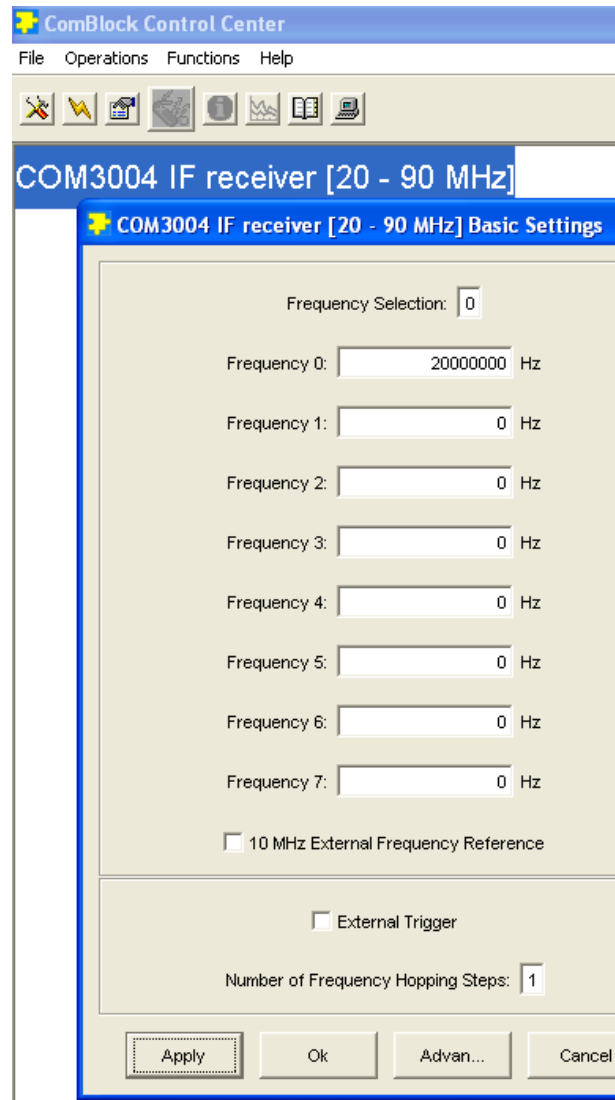
The easiest way to configure the COM-3004 is to use the ComBlock Control Center software supplied with the module(s). After detecting the ComBlock modules (2nd button from left), highlight the COM-3004 module to be configured. Then press the settings button (3rd button from the left).

Up to eight frequencies can be stored within each module at any given time. The current frequency is selected by an index in the range 0 to 7. Frequencies are expressed in Hz.

A basic frequency hopping scheme can be enabled by

- (a) enabling the external trigger
- (b) entering the number of frequency hopping steps in the round-robin arrangement.

For example, by specifying 4 steps, the receiver center frequency will follow the following index sequence: 0,1,2,3,0,1,2,3,0,1, etc., the index being incremented at the rising edge of each external PLL_STROBE pulse.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Programmers developing custom applications (using the [ComBlock API](#) instead of the supplied ComBlock control center graphical user interface) should know that frequency changes are enacted upon (re-)writing to the last register (REG35).

Parameters	Configuration
RF frequency 0 f_0	Valid range 20 MHz – 90 MHz, expressed as $f_0/f_{dds} * 2^{32}$. The DDS frequency f_{dds} is typically 200 MHz. Thus the frequency increment is 0.046 Hz REG0: bit 7:0 (LSB) REG1: bit 15:8 REG2: bit 23:16 REG3: bit 31:24 (MSB)
External/Internal DDS frequency reference	0 = internal 40 MHz clock. 1 = external (10 MHz typ.) frequency reference. REG4 bit 0
External/Internal ADC sampling clock	Select the external ADC sampling clock EXT_ADC_CLK or the internal 40 MHz sampling clock. Selecting sampling rates less than half the baseband filter bandwidth may result in aliasing. 0 = internal 40 MHz ADC clock 1 = external ADC clock. REG4 bit 1
DDS clock multiplier	Multiplies the frequency reference to obtain the DDS processing clock f_{dds} . For $f_{dds} = 200$ MHz, select 05 in conjunction with the 40 MHz internal clock or 20 (enter hexadecimal x14) when the external 10 MHz frequency reference is used. Valid range 4 to 20. REG5 bits 4-0
External controls enabled/disabled	Enable or disable the PLL_STROBE external control on the J6 connector. 0 = external control disabled 1 = external control enabled REG6: bit 1
Frequency selection	Use to switch local oscillator frequency among preselected values. Range 0 through 7 REG6 bits 7-5.
RF frequency 1	Preselected frequency 1. Same format as RF frequency 0. REG7: bit 7:0 (LSB) REG8: bit 15:8 REG9: bit 23:16 REG10: bit 31:24 (MSB)
RF frequency 2	Preselected frequency 2. Same format as RF frequency 0. REG11: bit 7:0 (LSB) REG12: bit 15:8 REG13: bit 23:16 REG14: bit 31:24 (MSB)
RF frequency 3	Preselected frequency 3. Same format as RF frequency 0. REG15: bit 7:0 (LSB) REG16: bit 15:8 REG17: bit 23:16

	REG18: bit 31:24 (MSB)
RF frequency 4	Preselected frequency 4. Same format as RF frequency 0. REG19: bit 7:0 (LSB) REG20: bit 15:8 REG21: bit 23:16 REG22: bit 31:24 (MSB)
RF frequency 5	Preselected frequency 5. Same format as RF frequency 0. REG23: bit 7:0 (LSB) REG24: bit 15:8 REG25: bit 23:16 REG26: bit 31:24 (MSB)
RF frequency 6	Preselected frequency 6. Same format as RF frequency 0. REG27: bit 7:0 (LSB) REG28: bit 15:8 REG29: bit 23:16 REG30: bit 31:24 (MSB)
RF frequency 7	Preselected frequency 7. Same format as RF frequency 0. REG31: bit 7:0 (LSB) REG32: bit 15:8 REG33: bit 23:16 REG34: bit 31:24 (MSB)
Number of RF frequencies N_{freq} in the scanning list	Each time a PLL_STROBE pulse is received, the frequency pointer increments modulo N_{freq} . N_{freq} is in the range 1 – 8. REG35: bit 7:0.

Monitoring

Parameters	Monitoring
Option / Version	Returns '3004Av or 3004Bv' when prompted for option and version (v) numbers

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1 / ADC_CLK	Selected ADC sampling clock.
TP2 / PLL_REF	Reference clock (10 MHz external or 40 MHz internal)
TP3	Baseband signal, I-channel, at A/D converter input. The nominal amplitude is 1V _{pp} when the AGC loop is closed with the following demodulator (COM-1001, COM-1011, or equivalent).
TP4	Baseband signal, Q-channel, at A/D converter input. Nominal amplitude is 1V _{pp} when the AGC loop is closed.

Operations

Internal vs External frequency reference for frequency synthesizer

The 20-90 MHz oscillator frequency generated by the direct digital frequency synthesizer (DDS) is frequency-locked onto a 10 MHz external or 40 MHz internal clock. The internal versus external frequency references are user-selected by software through control register REG4 bit 0.

In order to use the external frequency reference, connect a 10 MHz sinewave, clipped sinewave or square wave to the SMA connector J8. Then select external frequency reference using the control register REG4 bit 0. The DDS clock multiplier in control REG5 must be multiplied by a factor of 4 to account for the decrease in reference frequency from 40 to 10 MHz.

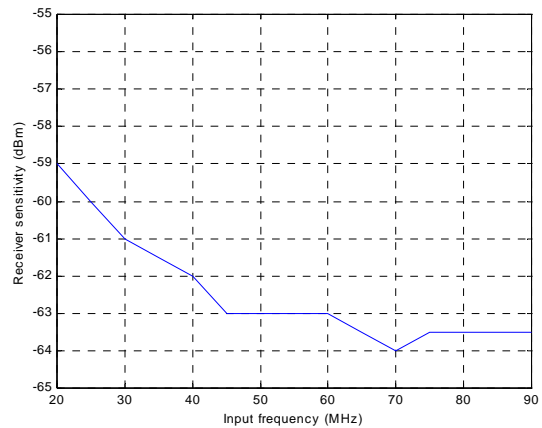
There is no need to remove the external 10 MHz cable connection when operating with the internal 40 MHz frequency reference. Thus, the internal/external reference clock selection can be implemented quickly under software control.

Internal vs External ADC sampling clock

The source for the Analog to Digital converter clock can be selected to be internal (fixed 40 Msamples/s) or external (up to 40 Msamples/s) by software command.

Performance

Receiver Sensitivity



Minimum input level for full 10-bit dynamic range at the baseband A/D converters (1Vpp)

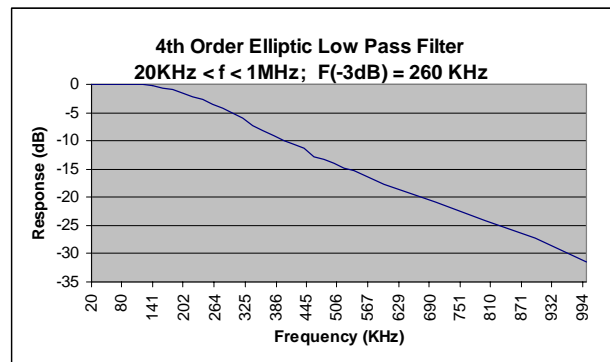
Internal Clock Reference

The internal crystal performance is as follows:

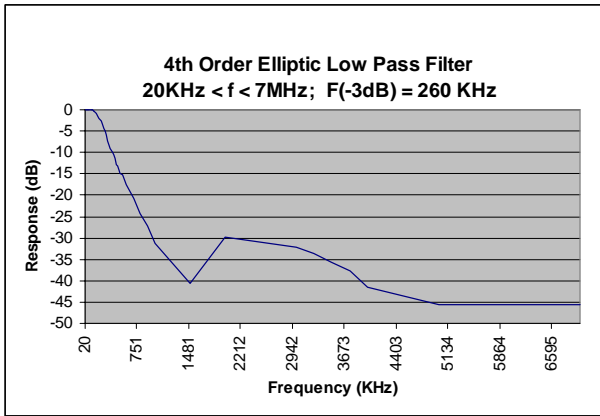
- tolerance: ± 75 ppm max @25C
- temperature stability (-10C to +60C): ± 50 ppm max
- aging: ± 5 ppm/year max @25C

Low Pass Filter (-A Option)

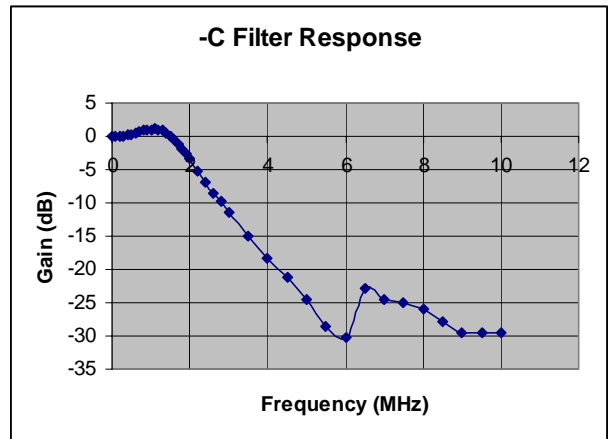
Each A/D converter is preceded by a 4th order elliptic low-pass filter. The one-sided -3 dB cutoff frequency for model COM-3004-A (Narrow-band applications) is 255 KHz. Within the [0-140 KHz] band, the maximum in-band ripple ± 0.15 dB.



COM-3004-A baseband low-pass filter frequency response(typ.). Span 1 MHz, 5dB/div.



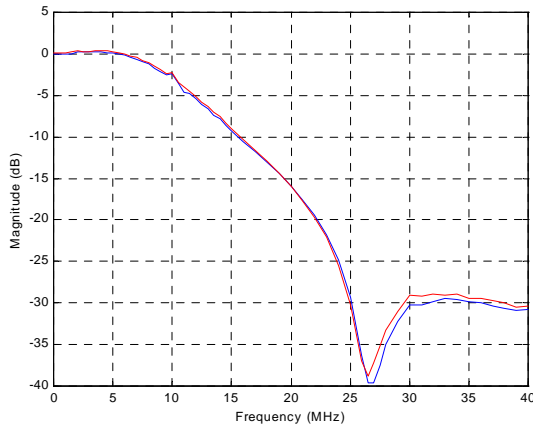
COM-3004-A baseband low-pass filter frequency response(typ.). Span 7 MHz, 5dB/div.



COM-3004-C baseband low-pass filter frequency response(typ.). Span 10 MHz

Low Pass Filter (-B Option)

Each A/D converter is preceded by a 4th order elliptic low-pass filter. The one-sided -3 dB cutoff frequency for model COM-3004-B (wideband applications) is 10.4 MHz. Within the [0-6 MHz] band, the maximum in-band ripple ± 0.2 dB.



COM-3004-B baseband low-pass filter frequency response(typ.). Span 40 MHz, 5dB/div.
 I channel (blue), Q-channel (red)

Low Pass Filter (-C Option)

Each A/D converter is preceded by a 4th order elliptic low-pass filter. The one-sided -3 dB cutoff frequency for model COM-3004-C is 1.93 MHz. Within the [0-1.5 MHz] band, the maximum in-band ripple ± 0.55 dB (including all effects: baseband filter response, front-end gain stability).

Phase Noise

Typical phase noise when using internal frequency reference is:

- 90 dBc/Hz @ 1 KHz, typ.
- 96 dBc/Hz @ 10 KHz, typ.
- 114 dBc/Hz @ 100 KHz, typ.

When selecting external frequency reference (2V_{pp} input 10 MHz sinewave), the typical phase noise is:

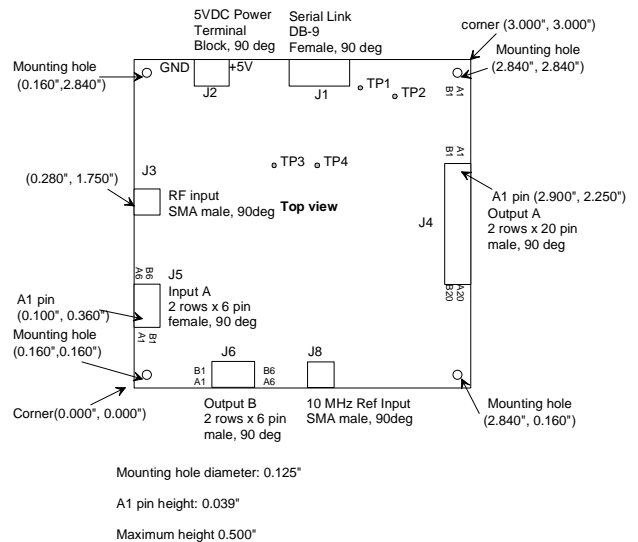
- 85 dBc/Hz @ 10 KHz, typ.
- 99 dBc/Hz @ 100 KHz, typ.

Other Specifications

Input noise figure: 6 dB typ.

LO Out-of-band spectral spurious lines: < - 55 dBc.

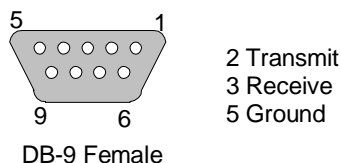
Mechanical Interface



Pinout

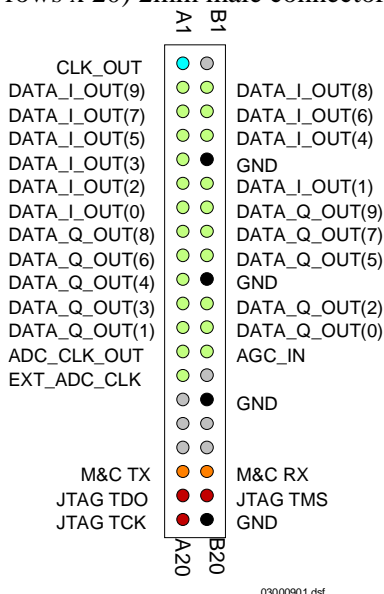
Serial Link J1

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



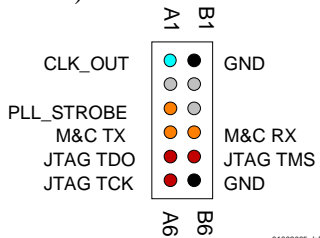
Output Connector J4

40-pin (2 rows x 20) 2mm male connector.



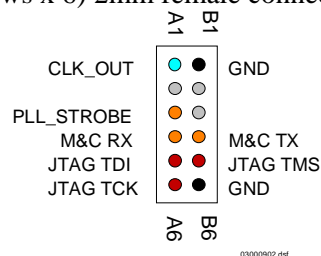
Connector J6

12-pin (2 rows x 6) 2mm male connector.



Connector J5

12-pin (2 rows x 6) 2mm female connector.



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-4004 [0-80 MHz] IF modulator, in back-to-back mode with attenuators.	COM-1008 Variable decimation
	COM-1001 BPSK/QPSK/OQPSK demodulator
	COM-1011/1018 Direct-sequence spread-spectrum demodulator
	COM-1027 FSK/MSK/GFSK/GMSK demodulator
	COM-8002 High-speed data acquisition. 256MB, 1Gbit/s, 50 Msamples/s.
	COM-2001 Dual D/A converter (baseband)

Configuration Management

This specification is to be used in conjunction with Atmel microcontroller software revision A.

ComBlock Ordering Information

COM-3004-A [20-90 MHz] Receiver. 280 KHz passband

COM-3004-B [20-90 MHz] Receiver Receiver. 12 MHz passband.

COM-3004-C [20-90 MHz] Receiver Receiver. 3 MHz passband.

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