

### Key Features

- High-speed Digital to Analog Conversion, 12-bit precision. Converts
  - 8 Real channels, or
  - 4 Complex (I & Q) channels
- Synchronization across channels for sampling clock, up-conversion phase and frequency.
- Configurable as
  - **Maximum bandwidth:**  
 $f_s = 600$  Msamples/s out  
 150 Msamples/s in  
 240 MHz maximum output frequency,  
 120 MHz max modulation bandwidth  
 or
  - **Maximum frequency:**  
 $f_s = 900$  Msamples/s out  
 112.5 Msamples/s in,  
 360 MHz maximum output frequency  
 90 MHz max modulation bandwidth
- Independent controls for each complex channel:
  - Frequency up-conversion
  - Amplitude
  - Interpolation
- 8 preset frequencies for fast (<500 $\mu$ s) up-converter frequency hopping
- Output filtering for images rejection
- Sampling clock and up-conversion frequency can be locked onto an external 10 MHz ultra-stable oscillator (frequency reference).
- Monitoring & Control over USB.
- Only single +5V<sub>DC</sub> supply required.  
Connectorized 3"x 3" module for ease of prototyping



For the latest data sheet, please refer to the **ComBlock** web site: [comblock.com/com2802.html](http://comblock.com/com2802.html).

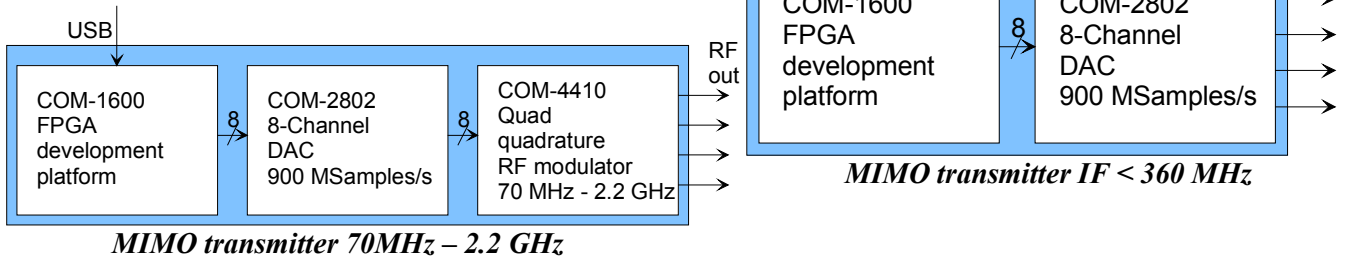
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to [comblock.com/product\\_list.html](http://comblock.com/product_list.html)

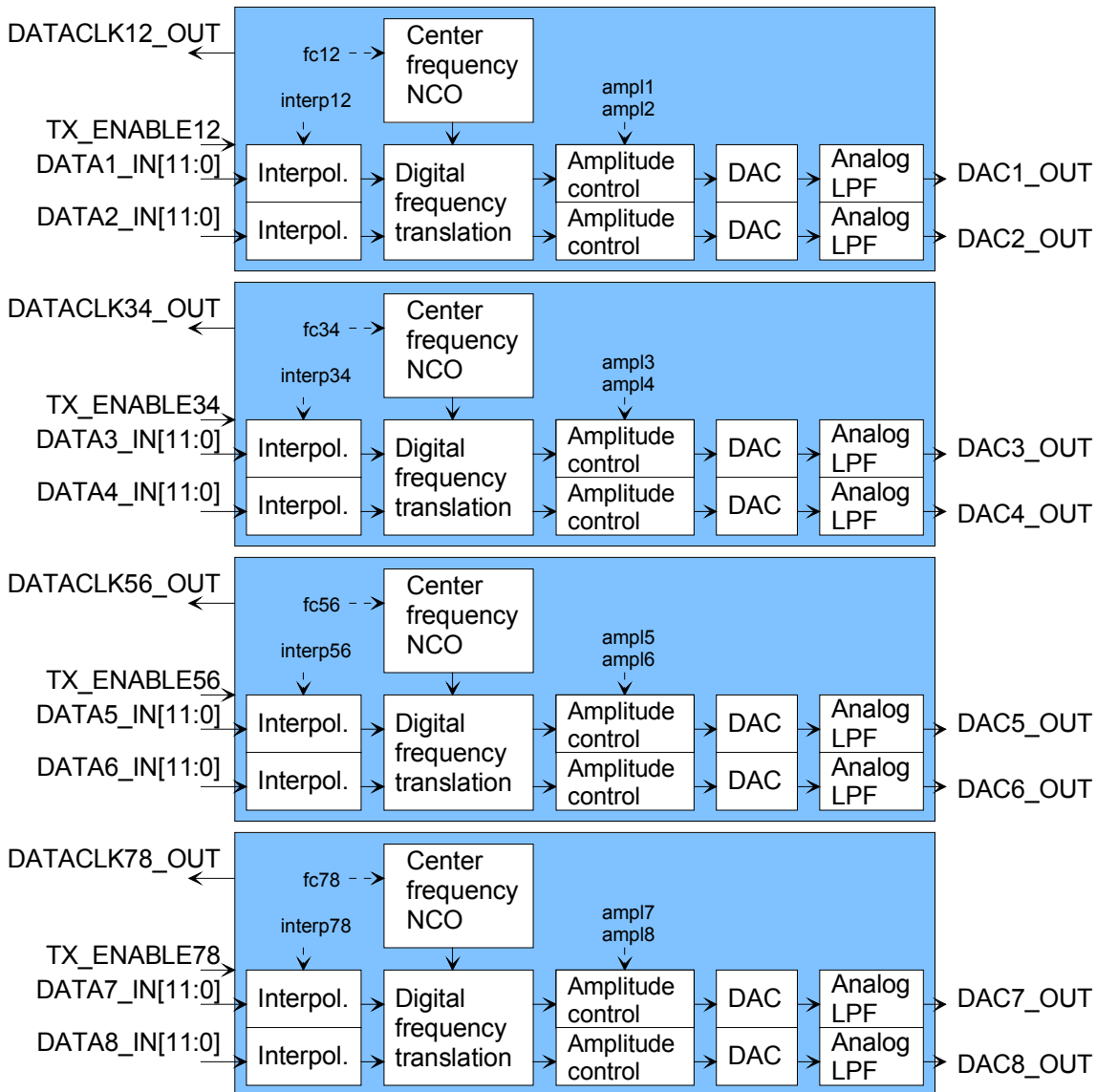
Keywords: MIMO, synchronized DACs, IF modulator, VHF, UHF, multi-channel, AD9785, ADF4350

# Typical Applications

Designed for MIMO applications



# Block Diagram



## Electrical Interface

### Inputs / Outputs

Digital Interface	Definition
DATA <sub>xy</sub> _IN[11:0]	<p>Multiplexed (interleaved) digital input samples for channel <i>x</i> and channel <i>y</i>.</p> <p>LVTTTL.</p> <p>12-bit unsigned (also known as “offset binary”) format. 0x000: maximum output level 0x3FF: minimum output level 0x1FF or 0x200 ≈ center level</p> <p>The data source must generate these samples synchronously with the supplied clock DATACLK<sub>xy</sub>_OUT. The edge is irrelevant because the internal PLL will adjust the clock phase for best input timing.</p> <p>Note: as large input signals may cause internal modulator saturation, users should include some margin with respect to the 0x000 and 0x3FF boundaries.</p> <p>Index <i>xy</i> is 12,34,56 or 78.</p>
TX_ENABLE <sub>xy</sub>	<p>This signal serves two purposes:</p> <ul style="list-style-type: none"> <li>Enabling the complex channel <i>xy</i></li> <li>Demultiplexing the interleaved I/Q input samples.</li> </ul> <p>LVTTTL.</p> <p>The data source must generate this signal synchronously with the supplied clock DATACLK<sub>xy</sub>_OUT, in alignment with DATA<sub>xy</sub>_IN. See the <a href="#">timing diagram</a>.</p> <p>Index <i>xy</i> is 12,34,56 or 78.</p>
DATACLK <sub>xy</sub> _OUT	<p>Sampling clock output, one for each complex channel. Please note that, even though all four complex channels generally operate at the same sampling rate, the four DATACLK<sub>xy</sub>_OUT clocks have <u>different and continuously adjusting phase</u>, as part of the internal timing tracking loop.</p>

	<p>LVTTTL.</p> <p>Speed: 300 MHz or 225 MHz depending on the selected interpolation factor.</p> <p>Index <i>xy</i> is 12,34,56 or 78.</p>
FREQ_STROBE	<p>Low-voltage (3.3V / 0V) TTL input control.</p> <p>A pulse (at least 62.5ns long) will cause the up-conversion frequency to jump to the next frequency in round-robin manner.</p> <p>Used to increment the modulo-<math>N_{freq}</math> frequency pointer 0 through 7 (where <math>N_{freq}</math> is defined in REG58)</p> <p>For example, if <math>N_{freq} = 3</math>, the frequency sequence is Frequency 0 -&gt; Frequency 1 -&gt; Frequency 2 -&gt; Frequency 0 &gt; etc...</p>
NCO_RESET	<p>LVTTTL input.</p> <p>A pulse (at least 62.5ns long) will cause the up-conversion frequency and phase to be reset in all four complex channels.</p>
EXT_REF_CLK	<p>Optional: External 10 MHz frequency reference, typically an ultra-stable clock. Sine, clipped sine or square wave; J4, SMA female connector, 50 Ω Input is DC-blocked. Minimum level: 2.0V<sub>pp</sub> Maximum level: 3.3V<sub>pp</sub></p>
Analog Interface	Definition
DAC <sub>x</sub> _P/N	<p>Differential Analog output; Peak amplitude: 2.0V<sub>pp</sub> (Diff) DC bias: 0.5V<sub>DC</sub> (each pin) Differential PCIe Connector Channel index <i>x</i> range: 1 to 8</p>
<b>USB Monitoring &amp; Control</b>	<p>Mini-USB connector Type AB Full speed / Low Speed</p>
<b>Power Interface</b>	<p>4.75 – 5.75V<sub>DC</sub>; Terminal block Power consumption is ~1.5A</p>

## Absolute Maximum Ratings

Supply voltage	-8V min, +6.5V max
EXT_REF_CLK	-0.3V min, +3.6V max
DACx_IN	-0.3V min, +3.6V max



## Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB (requires a mini-USB cable) or connections via adjacent ComBlocks:
  - USB
  - TCP-IP/LAN,
  - Asynchronous serial (DB9)
  - PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

## Configuration (Basic)

The easiest way to configure the COM-2802 is to use the **ComBlock Control Center** software supplied with the module on CD. In the ComBlock Control Center window detect the ComBlock module(s) by clicking the  *Detect* button, next click to highlight the COM-2802 module to be configured and click the  *Settings* button to display the *Basic Settings* window shown below.

*Basic Settings Window*

## Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see [www.comblock.com/download/M&C\\_reference.pdf](http://www.comblock.com/download/M&C_reference.pdf))

The module configuration parameters are stored in non-volatile memory. All control registers are read/write. Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Programmers developing custom applications (using the [ComBlock API](#) instead of the supplied ComBlock Control Center graphical user interface) should know that frequency changes are enacted upon (re-)writing to the last control register REG58.

Controls common to all channels	
Parameters	Configuration
Sampling rate $f_s$	Select an output sampling rate common for all channels: Range 70 MHz – 900 MHz by steps of 5 KHz, expressed in Hz. REG0: bits 7:0 (LSB) REG1: bits 15:8 REG2: bits 23:16 REG3: bits 31:24 (MSB)
External controls enabled/disabled	Enable or disable the <code>FREQ_STROBE</code> external control on the J2 connector. 0 = external control disabled 1 = external control enabled REG5(0)
Test modes	00 = normal operation 01 = unmodulated carrier REG5(5:4)
Channels 1-2	
Parameters	Configuration
Channel 1 enable	0 = powered down 1 = enabled Note: re-enabling the circuit may take up to 250ms. REG10(0)
Channel 2 enable	0 = powered down 1 = enabled Note: re-enabling the circuit may take up to 250ms. REG10(1)
Interpolation $N_i$	Interpolation factor (ratio of output sampling frequency to input sampling rate). The resulting input sampling rate is $f_s/N_i$  The maximum input sampling rate is 150 MS/s (or 300 MHz as I and Q input samples are interleaved). 00 = x1 interpolation 01 = x2 interpolation 10 = x4 interpolation 11 = x8 interpolation REG10(3:2)
Frequency up-conversion index	Select the frequency up-conversion value by pointing to one of eight pre-selected


	frequencies stored as Frequency 0 through 7. REG10(6:4)
Amplitude scale factor	9-bit amplitude scale factor. Applies equally to both I and Q channels. Fixed-point format: 2.7 For example, a nominal amplitude of 1.0 is obtained by entering the value 0x080. REG11: bits 7:0 (LSBs) REG12(0): bit 8 (MSb)
Channels 3-4	
Same definitions as for channel 1-2	REG14, REG15, REG16, REG17
Channels 5-6	
Same definitions as for channel 1-2	REG18, REG19, REG20, REG21
Channels 7-8	
Same definitions as for channel 1-2	REG22, REG23, REG24, REG25
Stored up-conversion frequencies	
Frequency 0 $f_0$	Frequency up-conversion (translation) from the digital input samples to the analog output.  Theoretical range: - $f_s/2$ to + $f_s/2$ , expressed as $2^{32} * f_0 / f_s$  In practice, the maximum output frequency is limited to about 40% of the sampling frequency.  Frequency step: $f_s / 2^{32}$  REG26: bits 7:0 (LSB) REG27: bits 15:8 REG28: bits 23:16 REG29: bits 31:24 (MSB)
Frequency 1	Same format as Frequency 0 REG30 (LSB), REG31, REG32, REG33(MSB)
Frequency 2	Same format as Frequency 0 REG34 (LSB), REG35, REG36, REG37(MSB)
Frequency 3	Same format as Frequency 0 REG38 (LSB), REG39, REG40, REG41(MSB)
Frequency 4	Same format as Frequency 0 REG42 (LSB), REG43, REG44, REG45(MSB)
Frequency 5	Same format as Frequency 0 REG46 (LSB), REG47, REG48, REG49(MSB)
Frequency 6	Same format as Frequency 0 REG50 (LSB), REG51, REG52,

	REG53(MSB)
Frequency 7	Same format as Frequency 0 REG54 (LSB), REG55, REG56, REG57(MSB)
Number of RF frequencies $N_{\text{freq}}$ in the scanning list	Each time a <b>FREQ_STROBE</b> pulse is received, the frequency pointer increments modulo $N_{\text{freq}}$ . $N_{\text{freq}}$ is in the range 1 – 8. REG58

Direct access to AD9785 control registers	
AD9785 selection	Select which IC to write to ( <i>see schematics<sup>1</sup> for reference</i> ) Bit 0: to U3 when '1' Bit 1: to U6 when '1' Bit 2: to U16 when '1' Bit 3: to U18 when '1'  If any one of these four bits is high, the user configuration above is ignored. REG59(3:0)
Word size	00 when writing to an 8-bit register 01 when writing to a 16-bit register 10 when writing to a 24-bit register 11 when writing to a 32-bit register REG59(5:4)
Address	AD9785 address. See AD9785 SPI register map section for details. REG60
Data[7:0]	REG61
Data[15:8]	REG62
Data[23:16]	REG63
Data[31:24]	Writing to REG64 triggers a word write to the selected AD9785 IC.

Board-specific fine calibration	
Phase correction ch12	TBD
Phase correction ch34	TBD
Phase correction ch56	TBD
Phase correction ch78	TBD
Amplitude balance offset ch12	TBD
Amplitude balance offset ch34	TBD
Amplitude balance offset ch56	TBD
Amplitude balance offset ch78	TBD
DC bias correction ch1	TBD
DC bias correction ch2	TBD
DC bias correction ch3	TBD
DC bias correction ch4	TBD
DC bias correction ch5	TBD
DC bias correction ch6	TBD
DC bias correction ch7	TBD
DC bias correction ch8	TBD

## Monitoring

Monitoring the status of the COM-2802 is performed by viewing the  *Status* window in ComBlock Control Center. All register values are displayed in hexadecimal, but other formats are displayed by hovering over the hex value with the cursor.

Custom applications can monitor module status again, by using the [ComBlock API](#).

Parameters	Monitoring
PLL Lock	The PLL generating the sampling clock is nominally locked onto the internal or external 10 MHz frequency reference. 0 = Not Locked 1 = Locked SREG0 bit 7
Timing alert	There are two types of timing errors: data timing errors and multi-DAC synchronization timing error. 0 = Normal timing. 1 = Timing error. SREG0 Bit 0: DAC1 SREG0 Bit 1: DAC2 SREG0 Bit 2: DAC3 SREG0 Bit 3: DAC4
Internal Power Supply Fault  <i>(see schematics for reference)</i>	0 = Normal Operation 1 = Fault Condition SREG0 Bit 4: DAC_+1.9V SREG1 Bit 0: D_+4.5V SREG1 Bit 1: DAC_+3.3V SREG1 Bit 2: CLK_+3.3V SREG1 Bit 3: DAC1A_+3.3V SREG1 Bit 4: DAC2A_+3.3V SREG1 Bit 5: DAC3A_+3.3V SREG1 Bit 6: DAC4A_+3.3V SREG1 Bit 7: DACA_+1.8V

## Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
DAC_REF	Internal / External 10 MHz reference clock.
PLL_LOCK $x$	DAC PLL lock status. Active high: '1' when locked. This information is also available in status register SREG0

<sup>1</sup> All ComBlocks schematics are located on the supplied CD-ROM

## Operations

### Input / Output Sampling Rates

The output sampling rate and the interpolation factor are user-defined parameters. This allows the user to trade-off maximum bandwidth versus maximum output frequency. The maximum settings are as follows:

#### Maximum bandwidth configuration

- 150 MS/s input,
- x4 interpolation,
- $f_s=600$  MS/s output,
- 240 MHz maximum output frequency,
- 120 MHz maximum (two-sided) usable modulation bandwidth.

#### Maximum frequency configuration:

- 112.5 MS/s input,
- x8 interpolation,
- $f_s=900$  MS/s output,
- 360 MHz maximum output frequency,
- 90 MHz maximum (two-sided) usable modulation bandwidth.

### Synchronization

All eight channels are synchronized (when identically configured) in terms of:

- Sampling clock
- Up-conversion frequency and phase.

Four Numerically Controlled Oscillators (NCOs) control the up-conversion frequencies when transmitting complex signals. In order to synchronize all NCOs, the user must generate an NCO reset pulse.

### IF Modulator

Each complex channel can be translated in frequency between  $\pm 0.4 f_s$  using an independent 32-bit NCO.

The COM-2802 can therefore be used as an IF modulator for frequencies up to 360 MHz.

### Frequency Hopping

Frequency Strobe allows for quick jumps of up-conversion frequencies among 8 pre-selected values. Switching is in a “round robin” fashion sequentially through up to 8 frequencies (the actual number of frequencies in the round robin pool is set by  $N_{\text{freq}}$ . For example, when  $N_{\text{freq}} = 3$ , the up-conversion frequencies will be selected in the following index sequence: 0,1,2,0,1,2,0,1,2...

FREQ\_STROBE is an edge-triggered signal. FREQ\_STROBE pulse width should be at least 62.5nS long. Switching time using the FREQ\_STROBE signal is  $< 500\mu\text{s}$ .

### Internal vs. External Frequency Reference for Frequency Synthesizer

An external 10 MHz frequency reference can be used when precise frequency stability is required. In this case, simply connect a 10 MHz sine, clipped sine or square wave to the J1 EXTERNAL\_FREQ\_REF female SMA connector. Detection is automatic, thus no configuration change is needed. Upon removal of the external frequency reference signal, the module reverts to the internal frequency reference.

### DACs detailed configuration registers

The COM-2802 comprises four Analog Devices AD9785 dual DACs.

The user interface was designed to simplify the task of configuring the COM-2802 for the most common applications. However, many more features are accessible by directly programming the Analog Devices AD9785 dual DACs.

The AD9785 detailed registers are listed in the specifications in the “SPI Register Map” section: [http://www.analog.com/static/imported-files/data\\_sheets/AD9785\\_9787\\_9788.pdf](http://www.analog.com/static/imported-files/data_sheets/AD9785_9787_9788.pdf)

By setting one or multiple 1's in control register REG47, the user can enable writing to one, two, three or all four AD9785 ICs simultaneously.

To avoid any conflict, the configuration stored in REG0 through 45 is unchanged while performing a direct write to the AD9785 control registers.

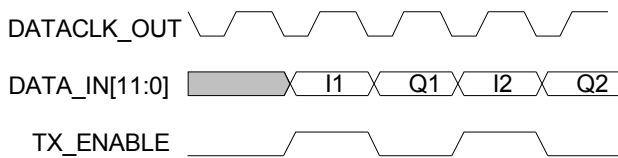
## DACs default configurations

- Inverse sinc ( $x/\sin(x)$ ) enabled
- PN code synchronization mode
- Single port mode

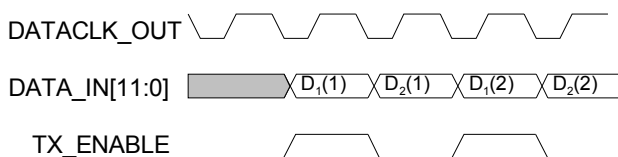
## Timing

### Input Samples

Adjacent odd and even (1 and 2, 3 and 4, etc.) input channel samples are multiplexed over the same 12-bit interface. TX\_ENABLE indicates which channel, '1' for the odd channel and '0' for even. TX\_ENABLE must be aligned with the data samples, within 2.4nS. From the user's perspective, there is no timing offset requirement between incoming DATACLK\_OUT and the outgoing data. Any offset is automatically compensated for internally. All four DATACLK\_OUTs have the same frequency but the phase may be different. All four data clocks must be used for their respective pair of input channels. The maximum sampling clock frequency is 300 MHz.



### Complex input, interleaved I/Q samples



### Interleaved input samples for channels 1 and 2

## Performance

### Internal Clock Reference

The internal crystal performance is as follows:

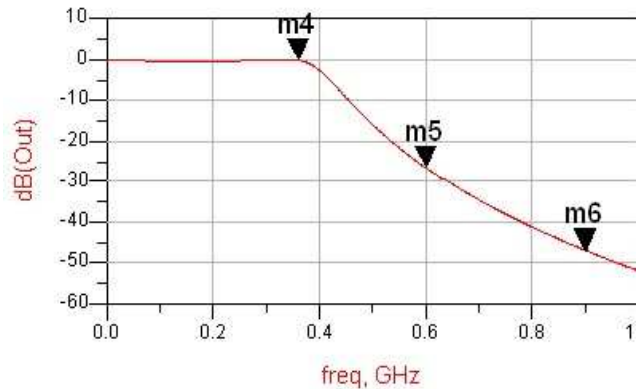
- Tolerance: [-5 to 0] ppm max @25C
- Temperature stability (-10C to +60C): ± 50 ppm max
- Aging: ±5ppm/year max (1<sup>st</sup> year) @25C

## Sampling Clock Phase Noise

TBD

### Low Pass Filter

Each D/A Converter is followed by a 5-pole Chebychev low-pass filter to suppress clock spectral spurious lines and aliasing. The filter response is as follows:



Passband: 0 – 360 MHz

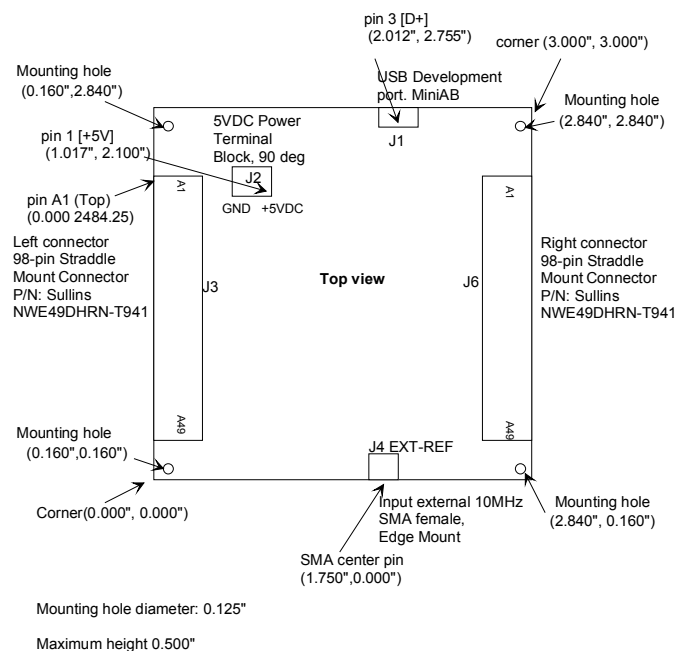
Passband gain flatness: better than ±0.3 dB in any 100 MHz sub-band.

Rejection at 600 MHz: 27 dB

Rejection at 900 MHz: 46 dB

Out of band spectral spurious lines: < -84dBc in any 3 KHz band.

### Mechanical Interface

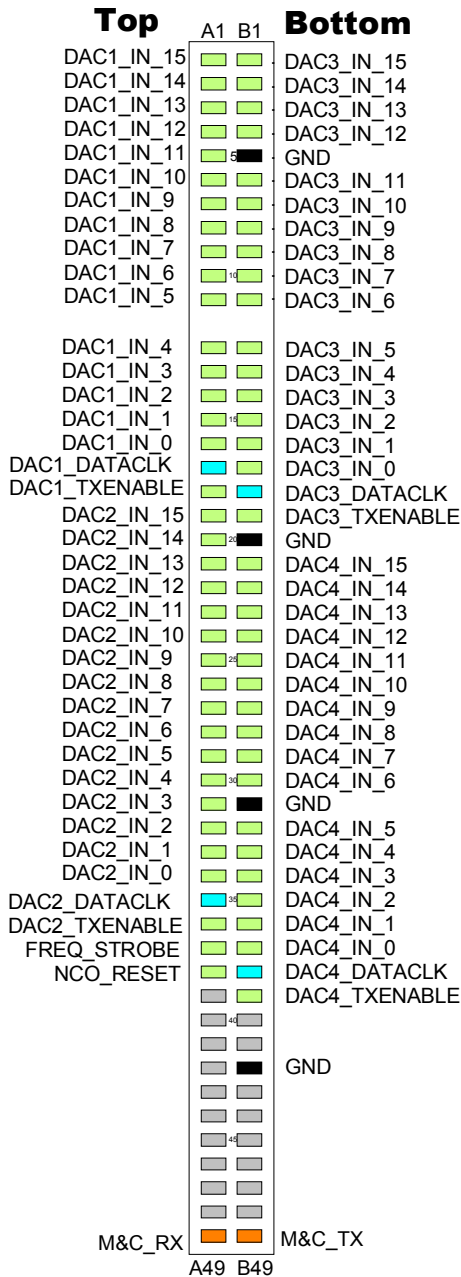


# Pinout

## Digital Input Connector, J3

98-pin Female Connector

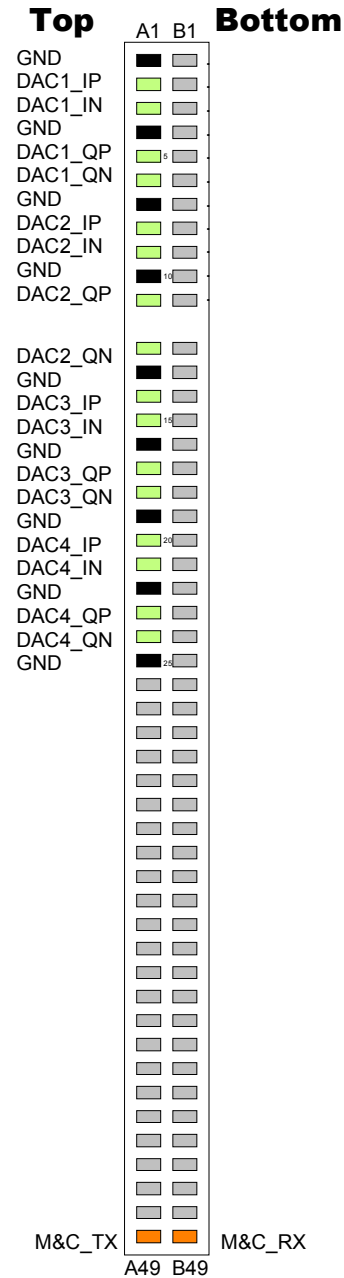
This connector is designed for a direct connection to FPGA-based ComBlocks (COM-160x, COM-170x)



## Analog Output Connector, J6

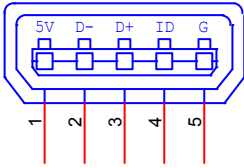
98-pin Female Connector

This connector is designed for a direct connection to the COM-4410 [70 MHz – 2.2 GHz] 4-CHANNEL QUADRATURE RF MODULATORS.



## Mini USB Connector, J1

The COM-2802 is a USB device with a mini type AB connector. (G = GND)



## I/O Compatibility List

(not an exhaustive list)

Input	Output
<a href="#">COM-1600</a> FPGA + ARM + USB2 + DDR2 + NAND development platform. Spartan-6 LX16	<a href="#">COM-4410</a> [70 MHz – 2.2 GHz] 4-channel quadrature RF modulators

## ComBlock Ordering Information

COM-2802  
SYNCHRONIZED 8-CHANNEL 900 MS/s  
DIGITAL-TO-ANALOG CONVERSION

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