COM-1808SOFT_RX DVB-S2 Receiver VHDL source code overview / IP core

Overview

The COM-1808SOFT_RX is a DVB-S2 compliant receiver written in generic VHDL.

The entire **VHDL source code** is deliverable. It is portable to a variety of FPGA targets.

Key features and performance:

- Flexible programmable features:
  - Modulation symbol rate, frequency offset, SRRC filter roll-off.
  - Output type: BBFRAME or stream (transport stream, generic stream packetized, generic bit stream)
- Provided with IP core:
  - VHDL source code
  - GNU radio project and Matlab conversion .m program for generating DVB-S2 waveforms.
  - VHDL testbench
  - PRBS11 test sequence generator, AWGN noise generator

Supported features

Feature	Supported
Inputs	two DDR complex (I,Q) baseband samples, 16-bit precision. ADC sampling rate is twice the clock frequency f_{CLK_RXg}
Maximum payload bit rate	> 675 Mbits/s (8-PSK, rate 9/10, Xilinx Ultrascale+ -2)
FEC frame	Automatic detection on a frame-to-frame basis: normal (64800 bits) short (16200 bits)
Modulation type	Automatic detection on a frame-to-frame basis: QPSK, 8-PSK, 16APSK, 32APSK
Error correction encoding	LDPC + BCH
Encoding rate	Automatic detection on a frame-to-frame basis: 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
SRRC filter roll-off	0.35, 0.25 and 0.20, user programmable
Input stream synchronizer	Yes
Null packet deletion	Yes
Maximum modulation symbol rate (ultrascale+ -2 speed grade)	> 250 MS/s
Output	• Single or multiple MPEG Transport Stream. 188-Byte fixed length frames, Byte-wide. • Single or multiple Generic Stream (packetized or continuous). Byte-wide.

MSS • 845 Quince Orchard Boulevard Ste N • Gaithersburg, Maryland 20878-1676 • U.S.A.
Telephone: (240) 631-1111 www.ComBlock.com
 Issued 1/13/2024

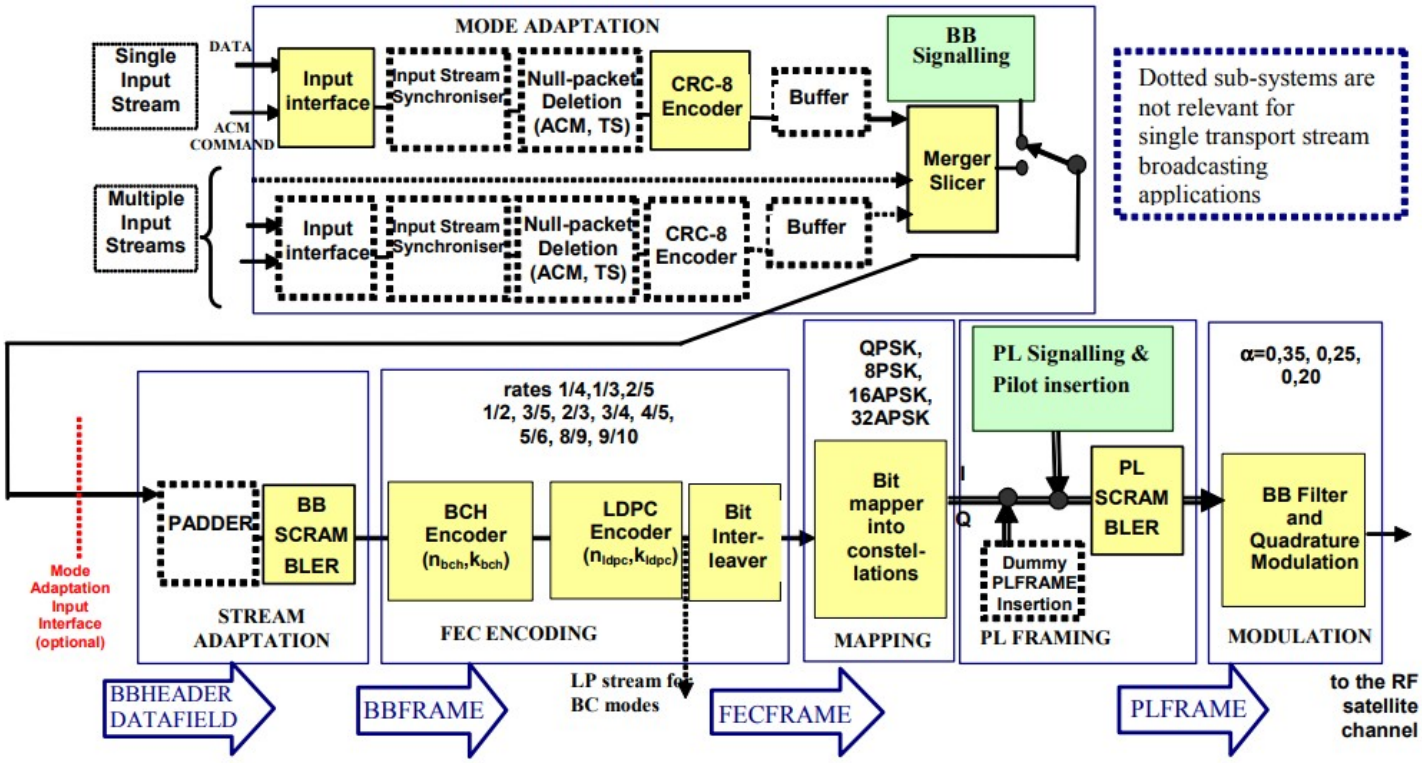


Figure 1: Functional block diagram of the DVB-S2 System

Extract from reference document [1]

Configuration

Synthesis-time configuration parameters

The following constants are user-defined in the *DVBS2_RX.vhd* component generic section and in the *DVB2_RX_PKG* package prior to synthesis. These parameters generally affect the size of the receiver embodiment.

Synthesis-time configuration parameters	Configuration
BBFRAME_OUTPUT_EN	true when the internal TS_DEMUX is bypassed and output consists of BBFRAMEs This is the receiver symmetric equivalent to enabling the mode adaptation input interface at the transmitter. See [1] I.2 Mode Adaptation input interface with in-band signaling (optional)
SIMULATION	True during simulation, false during deployment. Goal is to shorten some long timers during simulation.
RX_N_TS	number of Transport and/or Generic Streams

Run-time configuration parameters

The user can set and modify the following controls at run-time through the top level component interface:

Modulation Parameters	Configuration
AGC RESPONSE TIME	Adjust the AGC response time. approximately log2(NSymbols)
NOMINAL_ SYMBOL_ RATE(31:0)	Nominal (expected) symbol rate expressed as 2^32* symbol rate / ADC sampling rate. Since the input is DDR, the ADC sampling rate is 2* f_{CLK_Rxg} Example: 10 MSymbols/s @ 600 MSamples (300 MHz fclk_rxg) => x"04444444" Note: maximum symbol rate is 0.99*f_{CLK_Rxg} (need 1% margin for symbol tracking loop)
MOD_CENTER_ FREQ 31:0)	modulated signal center frequency. Expressed as fc/modulator processing clock * 2^32
MOD_RO(2:0)	Square root raised cosine filter roll-off factor: 0= 35%, 1 = 25%, 2 = 20%, 4 = 15%, 5 = 10%, 6 = 5%
MOD_CONTROL (7:0)	bit 0: spectrum inversion enabled (1) or not (0)

I/Os

General

Two independent clock domains are used in *DVBS2_RX.vhd*:

CLK_RXg for waveform input, ADC (DDR) sampling rate and demodulation.

CLK for bit de-interleaving, LDPC decoding, BCH decoding, mode adaptation and output. These functions process 8-bit wide data samples.

Of course, each clock timing period must be constrained in the constraint file (.xdc for Xilinx Vivado) associated with the project.

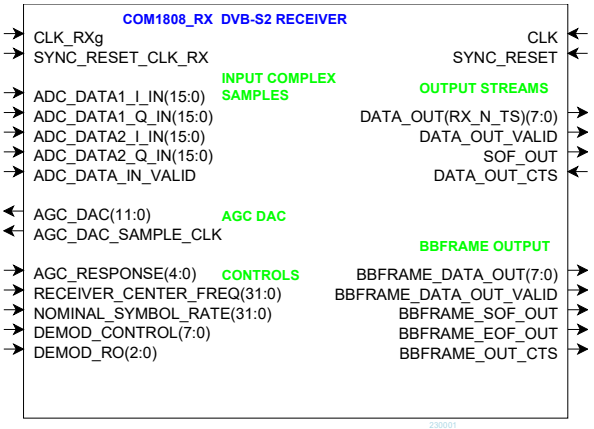
There is no need for inter-clock timing constraints between **CLK_RXg** and **CLK**. (use set_false_path tcl command in the constraint file).

These clocks must be global clocks (i.e. use BUFG before supplying the clock to the transmitter).

Two sync resets (**SYNC_RESET_CLK_RX** and **SYNC_RESET**) must be supplied, one for each clock domain. The recommended use is to keep the resets high until both clocks are stable.

In general, it is recommended to reset the receiver when changing the key configuration parameters (nominal symbol rate, nominal receiver center frequency, RRC filter rolloff).

Receiver



Data Path

Receiver inputs

ADC_DATA1_I_IN(15:0)
ADC_DATA1_Q_IN(15:0)
ADC_DATA2_I_IN(15:0)
ADC_DATA2_Q_IN(15:0)
Two 16-bit precision complex baseband DDR input samples from the ADC. DATA1 is sampled before DATA2. Read at the rising edge of the **CLK_RXg** half-rate sampling clock when **ADC_DATA_IN_VALID** = '1'
In the event of lower precision ADC samples, the LSbs should be set to zero.
Format: 2's complement (signed). Trick: if the samples are in binary offset format, just invert the most significant bit.

AGC_DAC(11:0): output to an external DAC to control an external AGC. Gain control for the external analog/IF/RF front-end. May need to be inverted depending on the analog front-end. 12-bit unsigned. FFF represents the minimum gain, 000 the maximum gain.
Read when **AGC_DAC_SAMPLE_CLK** is '1'

The above signals are clock-synchronous with ADC sampling clock **CLK_RXg**.

Receiver output streams

DATA_OUT is an array of **RX_N_TS** byte-wide output streams. Bit order: MSb first.

DATA_OUT_VALID(RX_N_TS-1:0): 1 CLK-wide pulses indicating that the associated **DATA_OUT** stream output Byte is valid.

SOF_OUT(RX_N_TS-1:0): output Start Of Frame. 1 CLK-wide pulse. The SOF is aligned with **DATA_OUT_VALID**. The first DATA_OUT byte in each user packet is typically the sync byte (x47 for transport stream, any user-value for generic packetized stream)

DATA_OUT_CTS: input. Clear-To-Send flow control. '1' indicates that the data sink is ready to accept another output byte.

Receiver BBFRAME output

When **BBFRAME_OUTPUT_EN** is enabled.

BBFRAME_DATA_OUT(7:0)
Note1: padded bytes are included in the BBFRAME
Note2: BBHEADER is not checked for valid CRC8

BBFRAME_DATA_OUT_VALID: 1 CLK-wide pulses indicating that the associated BBFRAME_DATA_OUT output Byte is valid.

BBFRAME_SOF_OUT
BBFRAME_EOF_OUT: 1 CLK-wide pulses marking the start and end of BBFRAME. Aligned with BBFRAME_DATA_OUT_VALID.

BBFRAME_OUT_CTS: CTS = Clear-To-Send, flow control signal. Data source will stop sending data when BBFRAME_OUT_CTS = '0'

Software Licensing

This software is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bit stream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from
http://www.comblock.com/download/softwarelicense.pdf

Portability

The VHDL source code is written in generic VHDL and thus can be ported FPGAs from various vendors.

Configuration Management

The current software revision is 011324

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code,.pkg packages, .xdc constraint files (Xilinx) One component per file.
/sim	VHDL test benches
/matlab	GNU radio configuration files + Matlab .m file for generating stimulus files for VHDL simulation and for end-to-end BER performance analysis at various signal to noise ratios

Project files:
Xilinx Vivado v2020 project file: project_1.xpr

VHDL development environment

The VHDL software was developed using the following development environment:
Xilinx Vivado 2020 for synthesis, place and route and VHDL simulation

Device Utilization Summary

Receiver device utilization
Device: Xilinx xcku5p-ffvb676-2-i
LDPC parallel decoders: N_PAR_DEC = 45

Resource	Utilization	Available	Utilization...
LUT	39596	216960	18.25
LUTRAM	885	99840	0.89
FF	34219	433920	7.89
BRAM	275	480	57.29
DSP	98	1824	5.37
IO	181	256	70.70
BUFG	3	256	1.17

Clock and decoding speed

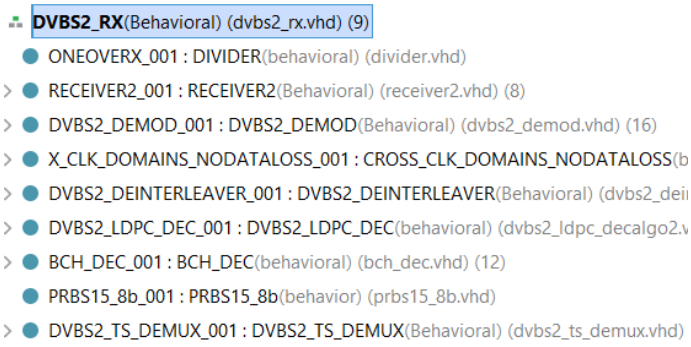
The receiver operates in two clock domains:
global clock CLK_RXg (half the ADC sampling rate) is mostly for demodulation.
Global clock CLK is mostly for error correction and formatting.

Typical maximum clock frequencies for various FPGA families are listed below:

Device family	CLK_Rxg	CLK
Xilinx Kintex7 ultrascale+ -2 speed grade	334 MHz	300 MHz

VHDL components overview

Receiver top level



DVBS2_RX.vhd is the receiver top level component. Inputs consist of two (DDR) baseband complex (I,Q) samples from the A/D converter synchronous with the CLK_RXg clock. The maximum modulation symbol rate is $0.99*f_{clk\_RXg}$ symbols/s.

RECEIVER2.vhd performs non modulation-specific tasks such as AGC, DC bias removal, frequency translation to baseband, anti-aliasing filtering and decimation.

DVBS2_DEMOD.vhd performs the demodulation based on three tracking loops: carrier tracking (for coherent demodulation), symbol timing tracking, and AGC. Each output bit's quality is expressed as Log-Likelihood Ratio (LLR) for use by the follow-on LDPC error correction decoder *DVBS2_LDPC_DEC.vhd*.

BCHDEC.vhd is the BCH error correction decoding (outer coding), as per [1] section 5.3.1.

The *PRBS15_8B.vhd* component generates the BB frame de-scrambling sequence.

Ancillary components

BRAM_DP2.vhd is a generic dual-port memory, used as input and output elastic buffers. Memory is inferred (no Xilinx primitive is used).

INFILE2SIM.vhd reads an input file. This component is used by the testbench to read a modulated samples file generated by GNU radio and follow-on `read_waveform.m` Matlab program for various modulation and coding types.

SIM2OUTFILE.vhd writes three 12-bit data variables to a tab delimited file which can be subsequently read by Matlab (load command) for plotting or analysis.

VHDL simulation

VHDL testbenches are located in the /sim directory.

The `tb_dvbs2_rx.vhd` testbench uses the /sim/input.txt DVBS2 modulated waveform file as input and demodulates and decodes the received bit stream.

The `tb_dvbs2_txrx.vhd` testbench consists of back-to-back DVBS2 transmitter and receiver. The transmitter generate a single DVBS2 generic packetized stream of length STREAMS_UPL with VCM: coding and modulation can change frequently between frames.

Matlab simulation

Matlab programs are located in the /matlab directory.

The `dvbs2_firrcos.m` program helps selecting the minimum size FIR filter to comply with the standard spectral masks for various root raised cosine filter rolloff factors.

The `resample_waveform.m` program resamples waveform files generated by the transmitter with the receiver sampling clock. The resulting input.txt file can be used by `tb_dvbs2_rx.vhd` testbench to assess the receiver performance.

The `read_waveform.m` program opens a *waveform.dat* complex samples file generated by GNU radio, reformats it to 2 columns of signed integers 12-bit precision then saves it to the input.txt file for import by the `tb_dvbs2_rx.vhd` testbench. It can also add white Gaussian noise to the waveform as needed.

GNU radio waveform generation

GNU radio can be used to generate DVB-S2 waveforms. An example GNU configuration is provided in /matlab/dvbs2_tx312MS.grc for the following configuration:
645.16 Msamples/s input sampling rate
8PSK modulation, 39.0625 Msymbols/s, short frame, rate 3/4
(see block diagram further down)

Reference documents

[1] DVB-S2 specifications, ETSI EN 302 307-1 V1.4.1 (2014-11)

[2] DVB-S2 Extensions (DVB-S2X) specifications ETSI EN 302 307-2 V1.1.1 (2015-02)

Acronyms

Acronym	Definition
ACM	Adaptive Coding and Modulation
ADC	Analog to Digital Converter
AWGN	Additive White Gaussian Noise
CCM	Constant Coding and Modulation
CTS	Clear-To-Send flow control flag
DAC	Digital to Analog Converter
DDR	Dual Data Rate
DVB	Digital Video Broadcasting
FPGA	Field Programmable Gate Array
GS	Generic Stream
GbE	Gigabit Ethernet
LLR	Log Likelihood Ratio
LSb	Least Significant bit in a word
MPEG	Moving Pictures Experts Group
MSb	Most Significant bit in a word
RF	Radio Frequency
SRRC	Square Root Raised Cosine (filter)
TS	Transport Stream
tx	Transmit
VCM	Variable Coding and Modulation

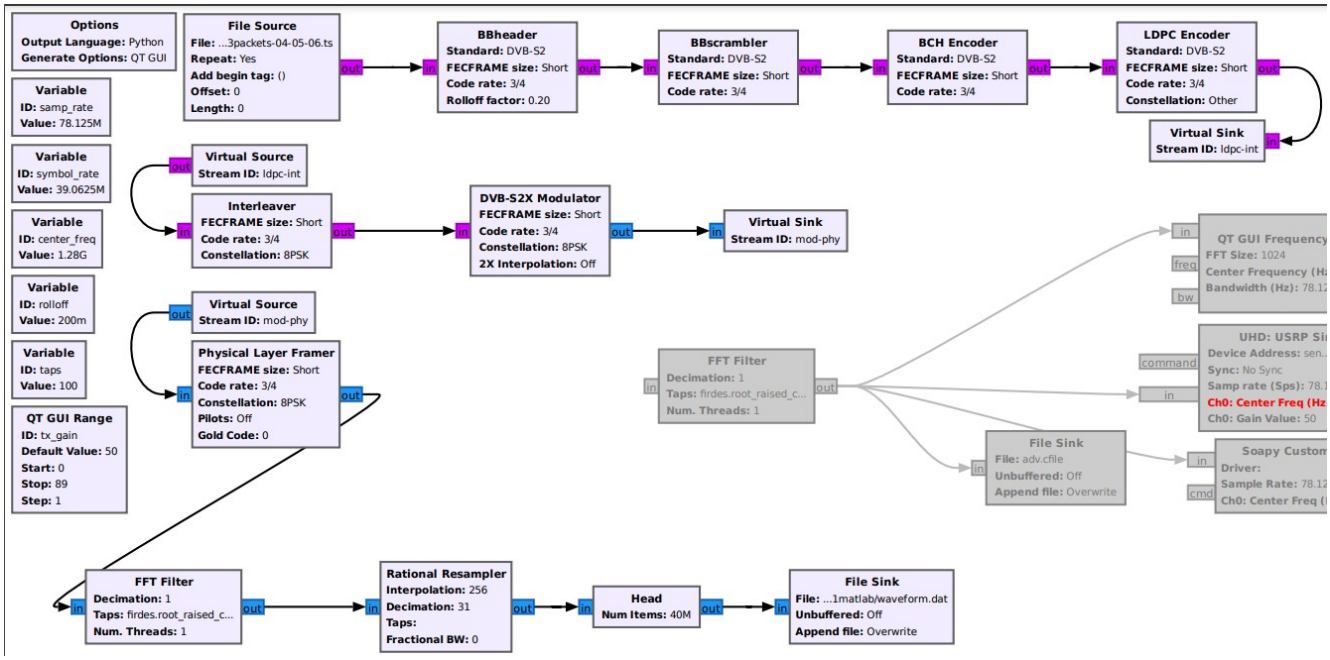
ComBlock Ordering Information

COM-1808SOFT_RX DVB-S2 receiver, VHDL source code / IP core

ECCN: EAR99

Contact Information

MSS • 845-N Quince Orchard Boulevard • Gaithersburg, Maryland 20878-1676 • U.S.A.



GNU radio project for stimulus waveform generation:

645.16 Msamples/s input sampling rate
8PSK modulation, 39.0625 Msymbols/s, short frame, rate 3/4