

COM-1500 FPGA + DDR2 SODIMM socket + ARM + USB2 DEVELOPMENT PLATFORM

Key Features

- Powerful digital signal processing platform comprising:
 - Large Xilinx Spartan-6 FPGA for massive **parallel** computing:
XC6SLX45 (-A option)
XC6SLX150 (-B option)
 - ARM 32-bit co-processor @120MHz (LPC1759) for complementary **sequential** computing¹
 - 200-pin SODIMM socket for an optional DDR2 memory module.
 - 1Gbit NAND for non-volatile storage of numerous FPGA configurations and user data.
- High-speed connectivity:
 - Two USB 2.0 connections:
 - High-speed (480 Mbits/s) connection through FPGA
 - Full-speed (12-Mbits/s) connection through ARM processor
 - differential LVDS connections
82 pairs (-A option)
92 pairs (-B option)
 - RS-232/RS-422
 - Input for an external, higher-stability 10 MHz frequency reference.



- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.

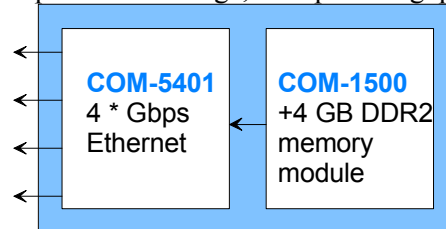
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Typical Applications

The COM-1500 is **interface-compatible** with numerous other ComBlock modules (RF, Analog, Network, modem, error correction). A few examples are illustrated below:

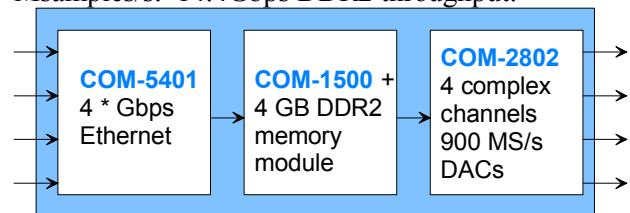
High-throughput IP data server:

Up to 4 GB storage, 4 Gbps throughput.



Arbitrary waveform generator

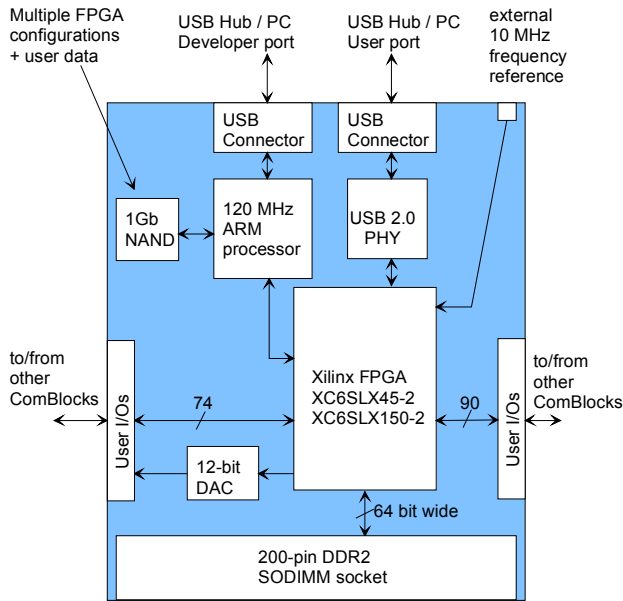
Up to 4GB storage, 4-complex channels, 900 Msamples/s. 14.4Gbps DDR2 throughput.



For the latest data sheet, please refer to the **ComBlock** web site: comblock.com/com1500.html.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer comblock.com/product_list.html.

¹ Use of the ARM processor is at the user's discretion. The ARM processor is pre-programmed with all basic functions.



COM-1500 Hardware Block Diagram

The COM-1500 is compatible with a comprehensive development environment of free industry-standard tools:

- Xilinx ISE WebPACK for development from VHDL or Verilog source code to FPGA binary. [free –A option only]
- Eclipse IDE + GNU ARM toolchain from C/C++ source code to ARM binary. [free]
- ComBlock flashloader to program the FPGA and ARM binaries into the board non-volatile flash memory over USB. [included]
- Optional JTAG USB pod (for ARM in-circuit debugging)

Getting Started with FPGA Development

A detailed tutorial is available at TBD

Developing a custom FPGA-based application requires six key steps:

- 1) The user writes VHDL or Verilog source code.
- 2) The Xilinx synthesis tool (XST), part of the Xilinx Integrated Software Environment (ISE) design suite, converts the source code into hardware primitives (.ngc file).
- 3) The constituent .ngc files are then mapped into the target FPGA and net routing takes place, again under the supervision of the Xilinx ISE. The output is a binary .bit file.
- 4) The Xilinx iMPACT tool reformats the .bit file into a .mcs PROM file.
- 5) The ComBlock Control Center programs the .mcs file into the board non-volatile (flash) memory.
- 6) At power-up, the ARM processor configures the FPGA using the designated .mcs configuration file stored on the flash memory.

Nominal Operation

Supply voltage	+4.9 to +5.5 VDC
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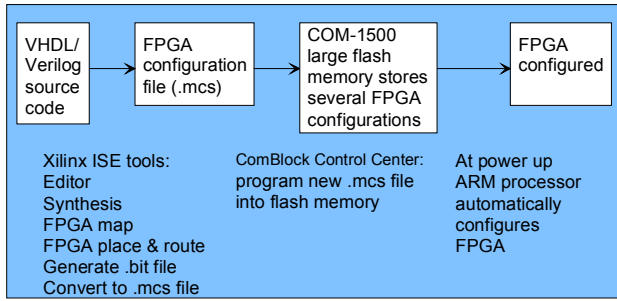
Absolute Maximum Ratings

Supply voltage	-16V min, +16V max
98-pin connector inputs	-0.5V min, +3.6V max

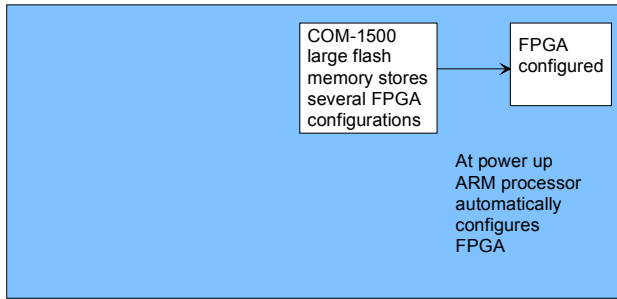
Simple Development Setup

The COM-1500 is designed to simplify the development setup and yet allow unrestricted access to all hardware features.

- Simply connect a USB cable between the COM-1500 USB development port and a PC.
- Connect +5VDC power to the green terminal block.
- Install the ComBlock Control Center software on a PC for monitoring, control and programming.
- Install the industry-standard tools for FPGA and optional ARM development on a PC (see tutorial below)
- Download the source code templates from www.comblock.com/download.html



Development environment



Run-time environment

Getting Started with ARM Development

Writing code for the ARM co-processor is *optional*. The ARM processor is factory programmed with the full set of functions described in this document. In many application cases, the processor could be left as is.

However, since the processor resources are significantly underutilized after the initial configuration, it is made available for developers to implement additional digital signal processing algorithms or customize the power profile.

A detailed tutorial is available at TBD

Operations

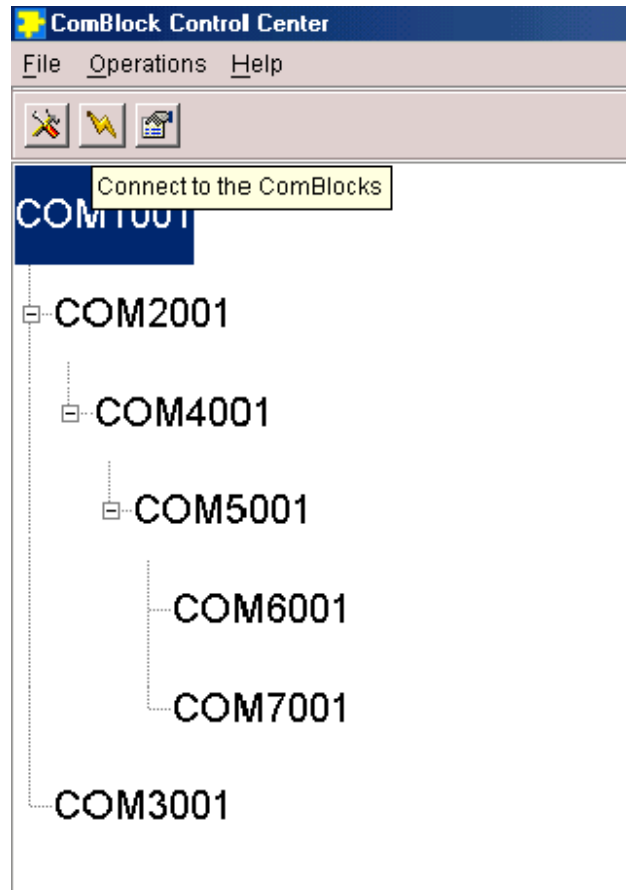
Graphical User Interface

A user-friendly graphical user interface (hereafter named ComBlock Control Center) is supplied with the COM-1500. The ComBlock Control Center runs on any Windows PC. It allows the user to communicate with the COM-1500 over the USB 2.0 interface and when other ComBlocks are connected, via serial link, LAN or PCMCIA/Cardbus.

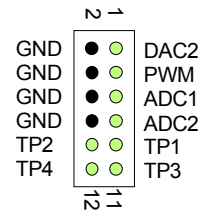
The primary use of the ComBlock Control Center is to:

- (a) Download new FPGA firmware (into non-volatile Flash memory)
- (b) Set control registers
- (c) Monitor status registers
- (d) Capture and display internal signals (ComScope).

When activated, the ComBlock Control Center enumerates the ComBlock modules within the assembly. The modules are identified by their name in a tree-like structure. Each module can be configured and monitored remotely.




The ComBlock Control Center software is provided with all ComBlock modules. The user's manual can be found at www.comblock.com/download/ccchelp.pdf.



Flash Memory

The FPGA configurations are stored in the COM-1500 non-volatile (Flash) memory. The ComBlock Control Center includes the utility to (re)write the FPGA .mcs PROM file into the flash

memory over USB. Click on the  button and follow the instructions.

The COM-1500 Supports [multiple personalities](#) and [dynamic reconfiguration](#):

- Up to 10 FPGA configurations can be stored in non-volatile flash memory.
- The selected configuration is automatically reloaded at power up or upon software command within 2 (TBC) seconds.

The COM-1500 comprises two USB ports labeled DATA and DEVELOP. The development port is the recommended port for flash programming, as it does not depend on the FPGA being properly configured. The USB data port could be inaccessible in the case of an invalid FPGA configuration.

Analog I/Os

The COM-1500 includes multiple ADCs and DACs as listed below:

Function	Precision	Speed	Under control by
DAC1	12-bit	1 MS/s	FPGA
DAC2	10-bit	TBD	ARM
PWM	10-bit	TBD	ARM
ADC1	12-bit	100KS/s	ARM
ADC2	12-bit	100KS/s	ARM

Most of these signals are accessible through a 12-pin header.

ARM Co-processor Test Points

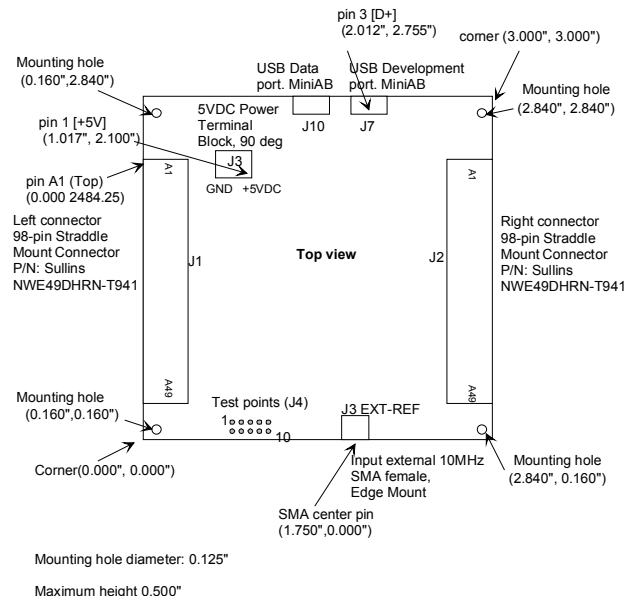
A 12-pin header (Jx) is provided for easy access to several key analog I/Os, digital I/Os and interrupt.

Power Control

The COM-1500 hardware is designed to operate in several low-power modes:

- **Sleep mode 1:**
 - The ARM processor is the only powered circuit. It can be woken up by an external wake-up signal or a USB input pin transition (USB development port).
 - FPGA is off. It will need to be reconfigured upon wake-up.
 - DAC/DDR2 SDRAM/NAND are off.
 - Power consumption is < TBD mA.
- **Sleep mode 2:**
 - ARM processor is active and able to communicate through USB.
 - FPGA is in suspend mode, i.e. keeps state and configuration.
 - DAC/DDR2 SDRAM/NAND are off.
- **Operating:**
 - Individual controls for powering the DAC, DDR2 SDRAM and NAND are accessible through the ARM processor.

Mechanical Interface



Schematics

The board schematics are available on-line at www.comblock.com/download/com_1500schematics.zip

VHDL code template

A VHDL template project is available on the ComBlock CD or on-line at www.comblock.com/download/com1500_000.zip

The template project includes:

- The VHDL source code (.vhd)
- The constraint file (.ucf) listing all pin assignments
- The Xilinx ISE project with the synthesis and implementation settings
- The resulting bit file (.mcs) is ready to be loaded into flash memory.

The sample code describes how the application interfaces with the ComBlock Control Center graphical user interface through control and monitoring registers. Monitoring and control messages and syntax are described in www.comblock.com/download/m&c_reference.pdf.

It also describes how to capture key internal signals in real-time and display on a host computer using the ComScope feature of the ComBlock Control Center. The ComScope user manual is available at www.comblock.com/download/comscope.pdf

Finally, the code template includes the following binary (.ngc) drivers:

- DDR2 driver
- 12-bit auxiliary DAC driver
- USB 2.0 driver
- Tri-mode 10/100/1000 Mbps Ethernet MAC

USB 2.0 Driver

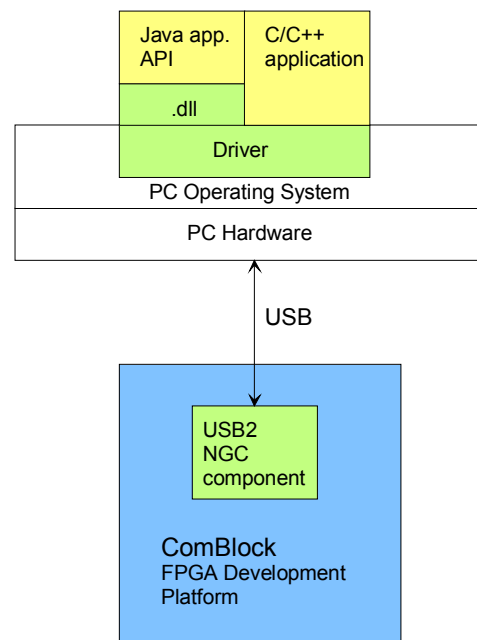
Software to help developers create USB high-speed communications between the COM-1500 platform and a host PC is provided. The **USB 2.0 software package** includes the following:

- USB20 NGC component for integration within the VHDL code.
- VHDL top-level code template
- Windows device driver (.sys, .inf files)

- Java API, .dll and application sample code
- C/C++ application sample code

The **USB 2.0 software package** is available on the ComBlock CD and can also be downloaded from www.comblock.com/download/usb20.zip.

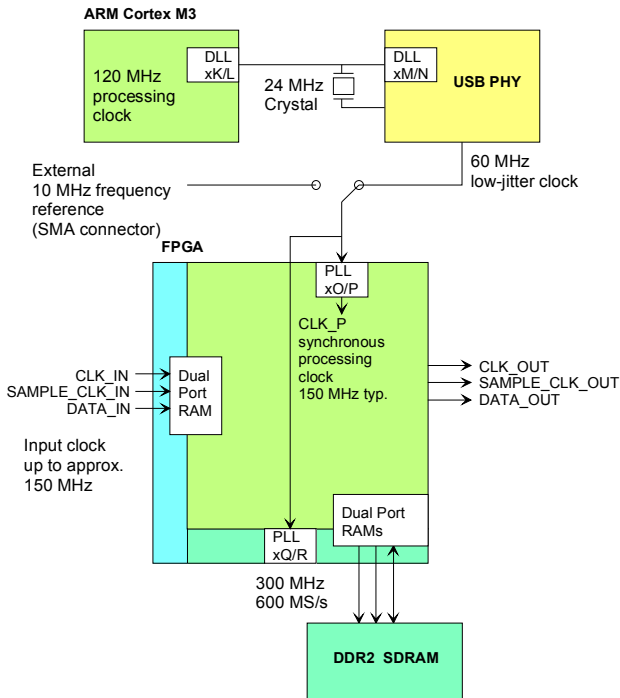
The user manual is available at www.comblock.com/download/USB20_UserManual.pdf



Blue: supplied hardware
Green: supplied ready-to-use software
Yellow: source code examples

Clock Architecture

The clock distribution scheme embodied in the COM-1500 is illustrated below.



Most of the COM-1500 internal frequencies are locked onto a single 24 MHz crystal oscillator. This oscillator (part of the USB PHY) serves as reference for the 100 MHz ARM coprocessor clock, the 60 MHz USB interface clock, and the 150/300/600 MHz FPGA clocks.

The VHDL code template generates the following FPGA clocks:

- 150 MHz processing clock
- 300 MHz DDR2 interface clock

Other clock architectures and frequencies are possible by changing the FPGA source code. For example, in applications requiring a higher frequency accuracy, the FPGA code can be written to select a user-supplied ultra-stable 10 MHz frequency signal as its frequency reference.

I/O Standards

The digital signals on connectors J1 and J2 are LVTTTL (0 – 3.3V) single-ended signals by default. However, the I/O types can be easily changed by software to other types such as differential LVDS_33.

See Xilinx user guide [ug381](#) for details.

Digital to Analog Converter (DAC)

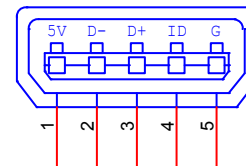
A 12-bit DAC/Analog output is built-in for gain control. The DAC operates under the direct control of the FPGA. The DAC output is connected to pin “B13” of the J1 connector. The DAC can be disabled in software to a high impedance state or physically disabled by removing the 0Ω R3 resistor.

The DAC can typically operate at a 0.5V/μsec slew rate. The output voltage range is from 0 to 3.3 V. The driver provided in the [code template](#) allows for approximate refresh rate of up to 1.765 MHz (slew rate limited.)

Pinout

USB

Both USB ports are equipped with mini type AB connectors. (G = GND). In both cases, the COM-1500 acts as a USB device.



Compatibility List

(Not an exhaustive list)

Input
COM-3002/3/4/5/6/7/8/9/10 RF/IF/Baseband receivers.
COM-5401 4-port 10/100/1000 Mbps Ethernet Transceivers
COM-1600/1500 FPGA + ARM development platforms
Digital Output
COM-2802 Synchronized 8-channel 900 MSamples/s Digital-to-Analog conversion
COM-1600/1500 FPGA + ARM development platforms
Software
COM-5401SOFT Tri-mode 10/100/1000 Mbps Ethernet MAC, VHDL source code

ComBlock Ordering Information

COM-1500-**A** FPGA (Spartan-6 LX45) + DDR2 SODIMM socket + ARM coprocessor development platform

COM-1500-**B** FPGA (Spartan-6 LX150) + DDR2 SODIMM socket + ARM coprocessor development platform

ARM-USB-OCD JTAG debugger (optional)

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