

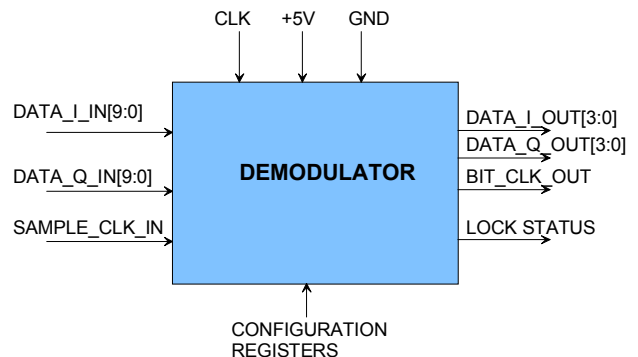
Key Features

- Direct sequence spread-spectrum demodulator.
- Variable chip rate up to 10 Mchips/s.
- Spreading codes:
 - Gold sequences (up to $2^{23}-1$ chips)
 - Maximal length sequences, (max length $2^{23}-1$ chips)
 - Barker codes (length 11, 13)
- BPSK, QPSK selectable.
- Demodulation performances: within 1.5 dB from theory at threshold SNR of 5 dB.
- Sequential code search.
- 4-bit soft-quantized demodulated bits.
- Monitoring:
 - Receiver lock
 - Carrier frequency error
- Connectorized 3" x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Single 5V supply. Interfaces with 5V and 3.3V logic.



Electrical Interface

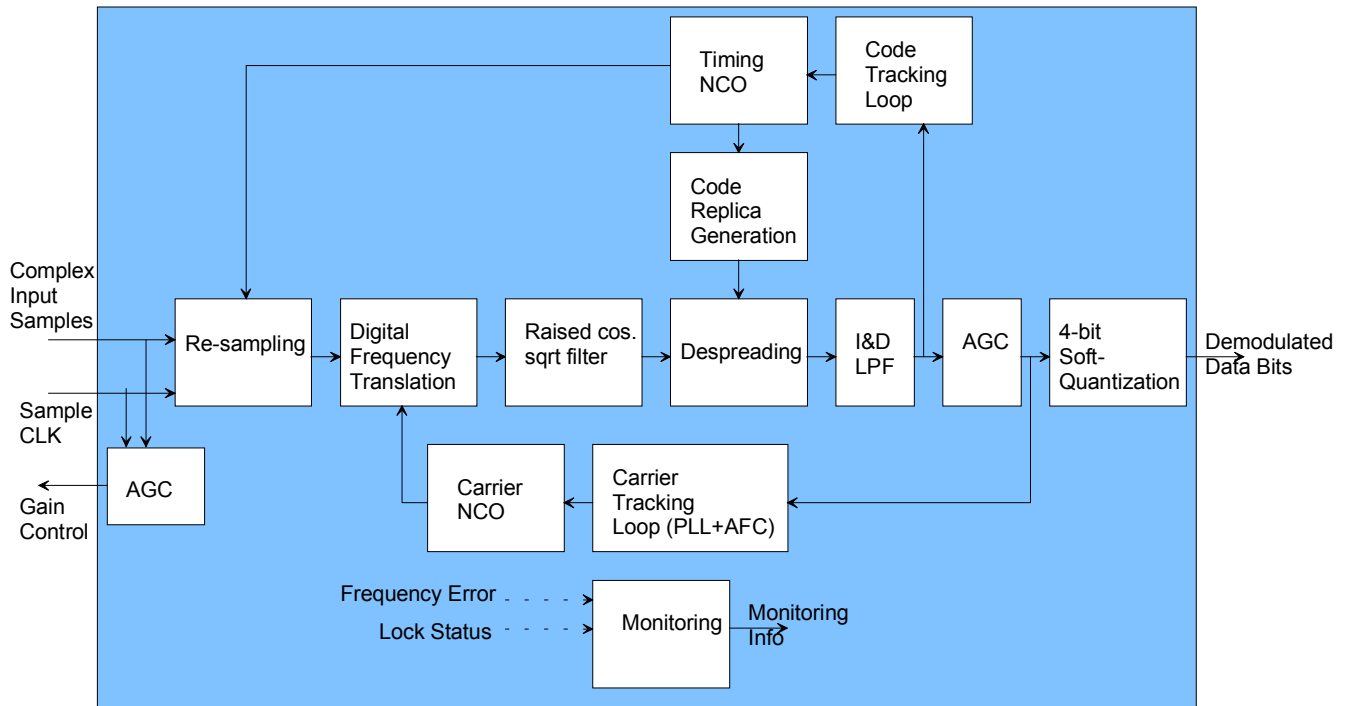
Demodulator Inputs / Outputs



For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1011.pdf
 These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm.

Block Diagram



Input Module Interface	Definition
DATA_I_IN[9:0]	Modulated input signal, real axis. 10-bit precision. Format: 2's complement or unsigned. Unused LSBs are pulled low.
DATA_Q_IN[9:0]	Modulated input signal, imaginary axis. 10-bit precision. Same format as DATA_I_IN. Unused LSBs are pulled low.
SAMPLE_CLK_IN	Input signal sampling clock. One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = '1'. Nominal sampling rate is between 4 and 8 samples per symbol. Samples can be consecutive. Signal is pulled-up.
AGC_OUT	Output. When this demodulator is connected directly to an analog receiver, it generates a pulse-width modulated signal to control the analog gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain.

Output Module Interface	Definition
DATA_I_OUT[3:0]	4-bit soft-quantized demodulated bits, real axis. Unsigned representation: 0000 for maximum amplitude '0', 1111 for maximum amplitude '1'. When the serial output mode is selected, I and Q samples are transmitted one after another on this interface. I is transmitted before Q.
DATA_Q_OUT[3:0]	4-bit soft-quantized demodulated bits, imaginary axis. Same format as DATA_I_OUT. When the serial output mode is selected, this interface is unused.
BIT_CLK_OUT	Demodulated bit clock. One CLK-wide pulse. Read the output signal at the rising edge of CLK when BIT_CLK_OUT = '1'.
RX_LOCK	'1' when the demodulator is locked, '0' otherwise. The lock status is based on the

	code lock.
CLK_OUT	40 MHz output reference clock.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Configuration (via Serial Link / LAN)

Complete assemblies can be monitored and controlled centrally over a single serial, LAN or PCMCIA connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

This module operates at a fixed internal clock rate f_{clk} , determined by CLK_IN (typically 40 MHz).

Most processing is done at the sampling rate / $f_{sample_clk} = 4 * \text{chip rate}$.

Parameters	Configuration
Chip rate	24-bit signed integer (2's complement) expressed as $f_{chip\ rate} * 2^{24} / f_s$, where f_s is the input sampling rate as determined by the SAMPLE_CLK_IN clock. Generally, $f_s = f_{clk} = 40\ MHz$. The maximum practical chip rate is $0.99 * f_s / 4$ to allow for at least 4 samples per chip. The 99% factor is to leave code tracking loop some margin between nominal and actual received chip rates. REG0 = bit 7-0 REG1 = bit 15 – 8 REG2 = bit 23 – 16
Spreading factor (Processing gain)	Spreading code period Range: $1 - 2^{23} - 1$ <ul style="list-style-type: none"> When using Gold codes or maximal length sequences, it is important that this field be consistent with the G1 and G2 generator polynomials below. Length is always in the form $2^n - 1$, where n is an integer. When using Barker codes, the spreading factor must be either 11

	(0x0B) or 13 (0x0D). REG3 bits 7-0 (LSB) REG4 bits 7-0 REG5 bits 7-0 (MSB)
Code selection	001 = Gold code 010 = Maximal length sequences 011 = Barker code REG6 bits 2-0
Gold sequence / Maximal Length Sequence generator polynomial G1	24-bit. Describes the taps in the linear feedback shift register 1: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period $2^n - 1$. Example: $G1 = 1 + x^3 + x^6 + x^7 + x^9 + x^{10} + x^{14} + x^{16} + x^{17}$ is represented as 0x01 A3 64. REG7 = bits 7 – 0 REG8 = bits 15 – 8 REG9 = bits 23 – 16
Gold code generator polynomial G2	24-bit. Describes the taps in the linear feedback shift register 2: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period $2^n - 1$. Example: $G2 = 1 + x^9 + x^{13} + x^{14} + x^{17}$ is represented as 0x01 31 00. REG10 = bit 7 – 0 REG11 = bit 15 – 8 REG12 = bit 23 - 16
Nominal carrier center frequency (f_c)	Nominal center frequency. This value is subtracted from the received signal actual center frequency. 24-bit signed integer (2's complement) expressed as $f_c * 2^{24} / f_{chip\ rate} * 4$. Maximum range to avoid aliasing is $\pm 1.5 * f_{chip\ rate}$. REG13 = bit 7 – 0 REG14 = bit 15 – 8 REG15 = bit 23 - 16
Input sample format	0 = 2's complement 1 = unsigned REG16 bit 1
Carrier frequency loop gain	00 = nominal 01 = 2x loop gain 10 = 4x loop gain 11 = 8x loop gain REG16 bits 3-2
AFC enable	The automatic frequency control circuit extends the frequency acquisition over $\pm 10\%$ of the symbol rate. When disabled, the receiver only means of carrier acquisition is the carrier frequency tracking loop which is

	inherently limited to approximately 1% of the symbol rate. 0 = AFC disabled. Carrier tracking loop only 1 = AFC enabled. REG16 bit 4
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG16 bit 5
Reserved	Always 0 REG16 bit 6
Freeze monitoring data	As the monitoring data is constantly changing, it is important to be able to prevent changes while reading a multi-byte parameter. Write a zero in bit 7 to freeze the monitoring data prior to reading it. Write a one to re-enable the update. REG16 bit 7
Output sample format	00 = I/Q parallel 01 = I/Q serial, I before Q (never use with BPSK as there is no information data on the Q channel) REG17 bits 1-0
BPSK / QPSK decoding	00 = BPSK 01 = QPSK REG17 bits 3-2
Force Acquisition	A one-time write of '1' forces all loops (code, carrier PLL, AFC) back into acquisition mode. This can be used to get out of a false lock condition. There is no need to clear this bit. REG17 bit 7.

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

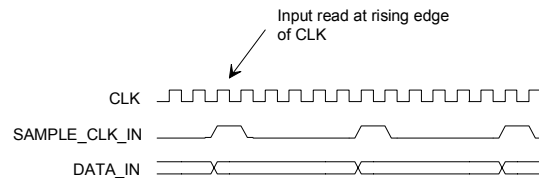
Monitoring (via Serial Link / LAN)

Parameters	Monitoring
Carrier frequency offset	Residual frequency offset with respect to the nominal carrier frequency. 24-bit signed integer (2's complement) expressed as $fdelta * 2^{24} / fchip \text{ rate} \times 4$ REG18 = bit 7 - 0 REG19 = bit 15 - 8 REG20 = bit 23 - 16
AGC gain	Digital AGC gain settings 8 bit unsigned REG21 bit 7-0.
Reserved	REG22: bit 7 - 0
Carrier Lock status	REG23 bit 0 0 = unlocked 1 = locked
Code Lock status	REG23 bit 1 0 = unlocked 1 = locked
Code Acquisition	REG23 bit 2 0 = code tracking mode 1 = code acquisition mode
Option o / Version v	Returns '101ov' when prompted for option o and version v numbers.

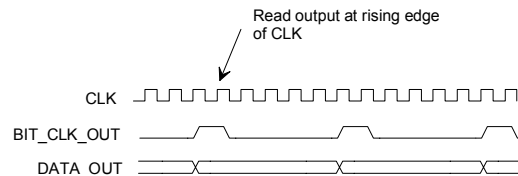
Timing

The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input



Output



Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	Carrier lock
TP2	Code lock (1) or scanning (0)
TP3	Recovered carrier
TP4	Recovered bit timing (i.e. start of code period). Useful to monitor code acquisition and tracking. Compare with modulator bit timing.
TP5	Spreading code replica
TP6	Spread I signal (MSB) (compare with spreading code replica at TP4)
TP7	Spread Q signal (MSB) (compare with spreading code replica at TP4)
TP8	Demodulated bit, I-channel DATA_I_OUT(3)
TP9	Demodulated bit, Q-channel DATA_Q_OUT(3)
TP10	FPGA clock DLL (CLKDLL) lock status. Unlocked when no input clock is present.

Implementation

Spreading codes

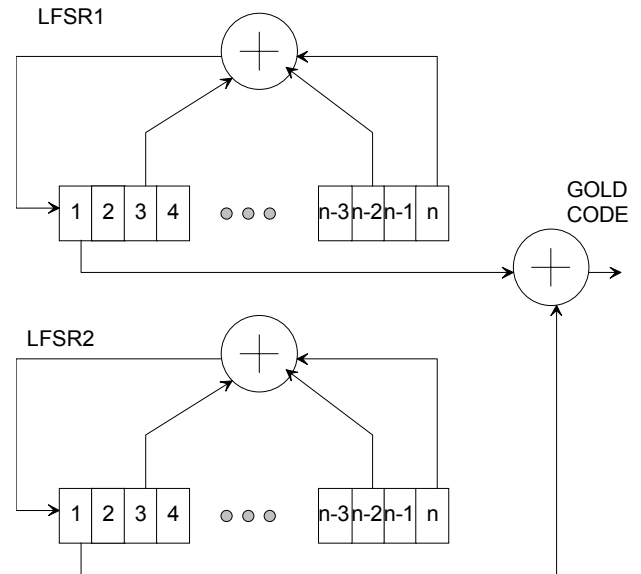
Spreading codes are pseudo random sequences which falls within the following categories:

- Gold sequences, for best autocorrelation properties
- Maximal length sequences
- Barker codes (length 11, 13)

The same spreading code is used on both the in-phase (I) and quadrature (Q) channels.

Gold sequences

Gold sequences are generated using two linear feedback shift registers LFSR1 and LFSR2 as illustrated below:



The code period is $2^n - 1$, where n is the number of taps in the shift register. The LFSRs are initialized to all 1's at the start of each period. The LFSRs will generate all possible n -bit combinations, except the all zeros combination.

Each sequence is uniquely described by its two generator polynomials. The highest order is n . The generator polynomials are user programmable.

A few commonly used Gold sequences are listed below:

$n = 5$ (length 31):

$$G1 = 1 + x^2 + x^5$$

$$G2 = 1 + x + x^2 + x^4 + x^5$$

$n = 6$ (length 63):

$$G1 = 1 + x^5 + x^6$$

$$G2 = 1 + x + x^4 + x^5 + x^6$$

$n = 7$ (length 127):

$$G1 = 1 + x^3 + x^7$$

$$G2 = 1 + x + x^2 + x^3 + x^4 + x^5 + x^7$$

$n = 9$ (length 511):

$$G1 = 1 + x^5 + x^9$$

$$G2 = 1 + x^3 + x^5 + x^6 + x^9$$

$n = 10$ (length 1023):

$$G1 = 1 + x^7 + x^{10}$$

$$G2 = 1 + x^2 + x^7 + x^8 + x^{10}$$

$n = 11$ (length 2047):

$$G1 = 1 + x^9 + x^{11}$$

$$G2 = 1 + x^3 + x^6 + x^9 + x^{11}$$

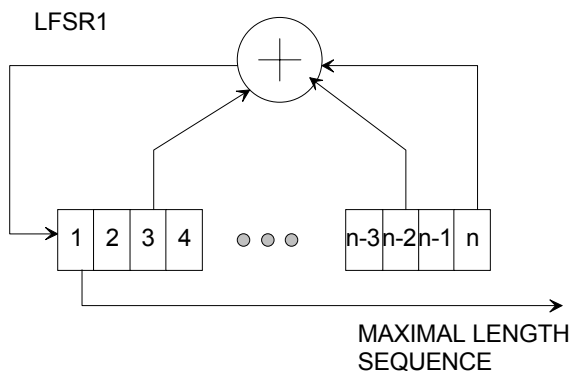
$n = 17$ (length 131071):

$$G1 = 1 + x^3 + x^6 + x^7 + x^9 + x^{10} + x^{14} + x^{16} + x^{17}$$

$$G2 = 1 + x^9 + x^{13} + x^{14} + x^{17}$$

Maximal length sequences

Maximal length sequences are generated using one linear feedback shift register LFSR1 as shown below:



The code period is $2^n - 1$, where n is the number of taps in the shift register. The LFSRs are initialized to all 1's at the start of each period. The LFSRs will generate all possible n -bit combinations, except the all zeros combination.

Each sequence is uniquely described by its generator polynomial. The highest order is n . The generator polynomial is user programmable.

A few commonly used maximal length sequences are listed below:

$$N = 4: G1 = 1 + x + x^4$$

$$N = 5: G1 = 1 + x^2 + x^5$$

$$N = 6: G1 = 1 + x + x^6$$

$$N = 7: G1 = 1 + x + x^7$$

$$N = 8: G1 = 1 + x^2 + x^3 + x^4 + x^8$$

$$N = 9: G1 = 1 + x^4 + x^9$$

$$N = 10: G1 = 1 + x^3 + x^{10}$$

Barker Codes

11 bit Barker code: 101 1011 1000, or 0x5B8

13 bit Barker code: 1 1111 0011 0101, or 0x1F35

Data Rate

The data rate is determined by the chip rate, the processing gain (i.e. the spreading code period) and the modulation (BPSK/QPSK).

For a QPSK modulated signal, the data rate is $2 * \text{fchip rate} / \text{processing gain}$

Filter Response

This module is configured at installation with a 40% rolloff filter. The filter rolloff can be selected among 20%, 25% and 40%. Changing the rolloff selection requires re-loading the firmware using the ComBlock control center.

All firmware versions can be downloaded from

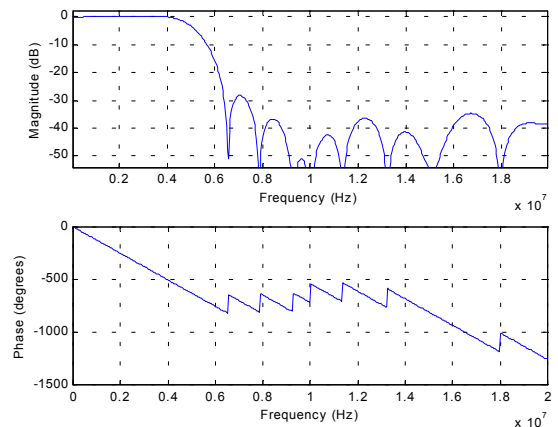
www.comblock.com/download.

COM-1011-A DSSS demodulator 20% rolloff

COM-1011-B DSSS demodulator 25% rolloff

COM-1011-E DSSS demodulator 40% rolloff

Filter Response (25% rolloff)



(filter response normalized for $4 * \text{symbol rate} = 40 \text{ MHz}$)

The raised cosine square root filter with 25% rolloff is a 29-tap FIR filter with the following impulse response:

$$\text{Coeff}(0) = -4/1024$$

$$\text{Coeff}(1) = -12/1024$$

$$\text{Coeff}(2) = -8/1024$$

$$\text{Coeff}(3) = 2/1024$$

$$\text{Coeff}(4) = 16/1024$$

$$\text{Coeff}(5) = 24/1024$$

$$\text{Coeff}(6) = 12/1024$$

$$\text{Coeff}(7) = -16/1024$$

$$\text{Coeff}(8) = -48/1024$$

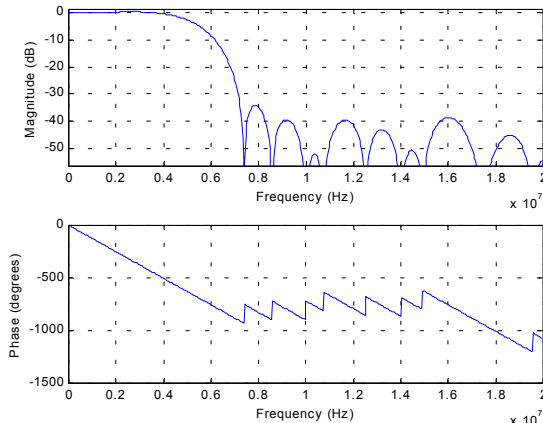
$$\text{Coeff}(9) = -48/1024$$

$$\text{Coeff}(10) = -16/1024$$

$$\text{Coeff}(11) = 64/1024$$

Coeff(12) = 160/1024
 Coeff(13) = 240/1024
 Coeff(14) = 272/1024
 Coeff(j=15:28) = coeff(28-j);

Filter Response (40% rolloff)



(filter response normalized for 4*symbol rate = 40 MHz)

The raised cosine square root filter with 40% rolloff is a 29-tap FIR filter with the following impulse response:

Coeff(0) = 4/1024
 Coeff(1) = 1/1024
 Coeff(2) = -4/1024
 Coeff(3) = -4/1024
 Coeff(4) = 2/1024
 Coeff(5) = 12/1024
 Coeff(6) = 14/1024
 Coeff(7) = -2/1024
 Coeff(8) = -30/1024
 Coeff(9) = -48/1024
 Coeff(10) = -24/1024
 Coeff(11) = 48/1024
 Coeff(12) = 152/1024
 Coeff(13) = 248/1024
 Coeff(14) = 284/1024
 Coeff(j=15:28) = coeff(28-j);

Frequency Tracking

The demodulator comprises both a phase locked loop (PLL) and an Automatic Frequency Control (AFC) loop. The AFC is to quickly detect and compensate for carrier frequency offsets, generally around the time of the code acquisition. The PLL is to detect and compensate for carrier phase errors.

The PLL is a second order loop. It can track the center frequency over a range of +/- 1.5 * symbol

rate. The digital implementation of the Costas PLL has a small frequency acquisition range of about $\pm 1\%$ of the despread symbol rate.

The main purpose of the AFC is to increase the frequency acquisition window to about $\pm 10\%$ of the despread symbol rate (typical). Once acquisition is achieved, the AFC can be disabled (see REG16 bit4).

If the unknown received carrier frequency uncertainty is larger, the user must program some search algorithm using the nominal center frequency control registers (REG13/14/15).

For high data rates (> 100 Kbps), carrier phase noise is generally negligible. For lower data rates, it may be necessary to adjust the carrier tracking loop gain as a tradeoff between carrier phase noise (originating at the modulator, up-converter, down-converter, etc) and thermal noise. To this effect, the user is given control of the loop gain over a range of x1, x2, x4 and x8.

The higher loop gain can also be used temporarily during acquisition to increase the frequency acquisition window from approximately 1% to 3% of the symbol rate. However, use of the AFC is preferred because of the faster acquisition time and larger acquisition range.

In some conditions, such as no input signal, the AFC and PLL loops can drift out and inhibit (re-)acquisition. It is possible for the user to reset the accumulators within the AFC and PLL loops by writing a '1' in REG17 bit7.

Code Tracking Loop

The code tracking loop is a coherent delay lock loop (DLL) of the 1st order.

Code Acquisition

When code lock is not detected for 7 consecutive bits, the receiver goes into code acquisition mode. The code replica is swept until code lock is detected (sequential code search). The rate at which the code replica is scanned is one chip every 8 bits. The search stops as soon as code lock is detected.

Input Interpolation

This module provides fine selection of symbol rates, as long as the input sampling rate is between x4 and x8 the symbol rate. For higher ratios between input sampling rate / symbol rate, the COM-1008 variable decimation filter is recommended to prevent aliasing.

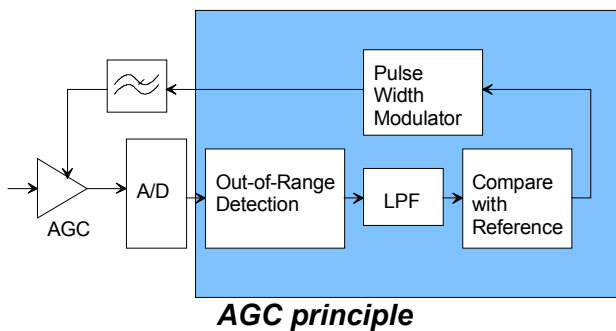
AGC

The COM-1011 comprises two AGC circuits, one at the front-end operating jointly with a front-end analog receiver, the other fully digital after channel filtering.

Front-End AGC

The purpose of this front-end AGC is to prevent saturation at the external A/D converter(s) while making full use of the 10-bit A/D converter dynamic range. The principle of operations is outlined below:

- out-of-range at the A/D converter is detected. An out-of-range condition occurs if the quantized A/D samples are equal to either "111111111" or "000000000".
- The AGC will adjust the analog circuitry gain so that out-of-range conditions do not occur more than 1 in 64 samples in the average.
- The resulting gain control signal is a pulse-width modulated (PWM) signal with 10-bit precision.



The analog circuit shall filter this 3.3V low-voltage TTL PWM signal with a low-pass filter prior to controlling the analog gain. The PWM is randomized and its spectral distribution shifted to the higher frequencies so as facilitate the analog low-pass filter design.

The AGC loop bandwidth is typically 1 Hz when used in conjunction with COM-30xx receivers and a 40 MHz input clock. The loop response time is asymmetrical: it responds faster to a saturation condition than to a 'low signal' condition.

The gain control signal will increase if too many out-of-range conditions occur.

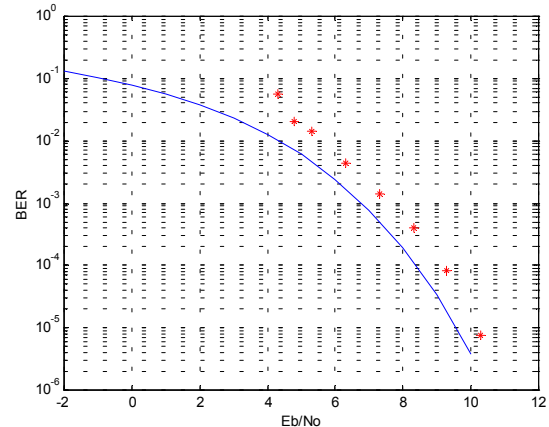
Digital AGC

A digital AGC provides 18 dB (3 bits) of dynamic range for signals following the raised cosine filter.

Performances

Bit Error Rate

The demodulation losses are typically less than 1.5 dB at threshold. The operating threshold E_b/N_o is 2dB (measured in fully digital test setup). The operating threshold is defined as the minimum E_b/N_o for which no loss of lock occurs for at least 10 minutes.



Actual BER vs E_b/N_o measurement.

Test conditions: COM-1012 modulator, COM-4004 70 MHz IF, up conversion to 1 GHz, COM-3002 L-band receiver, COM-1011 DSSS demodulator, COM-1005 BER Measurement.

10 Mchips/s. Maximal length sequence. Processing gain 127. Data rate 78.74 Kbps. BPSK. Raised cosine square root filters with 40% rolloff. SNR is 3 dB lower than the E_b/N_o .

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-300x receivers	COM-1005 Bit Error Rate Measurement
COM-1012/1019 spread spectrum modulators	COM-7001 Turbo code decoder
COM-1008 variable decimation	COM-1009 Convolutional decoder K=7, 5
COM-1023 BER generator, AWGN generator	
COM-1024 Multipath simulator.	

ComBlock Ordering Information

COM-1011 Direct sequence spread-spectrum demodulator.

MSS • 18221 Flower Hill Way #A •
Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111
Facsimile: (240) 631-1676
E-mail: sales@comblock.com